Performance Improvement of GFCAL Circuits

Shipra Upadhyay
Department of Electronics & Communication Engineering, Motilal Nehru National Institute of Technology, Allahabad-211004, India

R.K. Nagaria
Department of Electronics & Communication Engineering, Motilal Nehru National Institute of Technology, Allahabad-211004, India

R.A. Mishra
Department of Electronics & Communication Engineering, Motilal Nehru National Institute of Technology, Allahabad-211004, India

ABSTRACT
In this paper authors have presented a new approach to improve the performance of the glitch free cascadable adiabatic logic (GFCAL) circuit by replacing the triangular power supply with sinusoidal and trapezoidal power supplies (that control the charging and discharging of the capacitive load) and by sizing of transistors. A simulative investigation and performance analysis of proposed approach based 3 bit GFCAL counter, GFCAL JK flip flop and GFCAL 6T-SRAM circuit have also been done. The triangular power supply produces very large delay at the outputs of GFCAL circuits thus it will be very difficult to cascade larger circuits. A solution to provide cascadability is optimization of the delay. In the proposed approach the delay of GFCAL counter for triangular supply has been improved about 40% and 60% whereas for JK flip flop it is 46% and 49% and for 6T SRAM it is 17% and 91% with sinusoidal and trapezoidal power clocks respectively.

Keywords
Adiabatic circuit, MOS-Diode, Switching activity.

1. INTRODUCTION
Many methodologies have been proposed so far to reduce power dissipation [1]-[4], among them adiabatic logic technique [5] is promising alternative. Energy dissipated in a circuit depends on how fast the circuit switches or charges and discharges. Lower the rate of charging, the lesser amount of power is drawn from the source that means efficiency of charging depends on how slowly the capacitance is charged. Adiabatic circuit is based on the same principle; the clock transient time T is kept much larger than intrinsic time constant RC_L of the device [6] and due to this one can reduce power dissipation in a switching transition. Adiabatic circuits are also based on recovering the energy stored in nodal capacitances [7]. Most of the energy that was used for charging the load capacitances is recovered during discharging and stored for further use, while some amount is dissipated as a resistive drop. In adiabatic logic families time varying ramp voltage supply is use to charge the load capacitance, whereas in CMOS logic we use constant voltage source to charge the capacitive nodes. 'Adiabatic' term has been taken from a thermodynamic process which is reversible in nature, where after transformation no gain or loss of heat or energy occurs. Ideally it is assumed that the heat or energy loss can be made almost zero by making the transformation process sufficiently slow. Large number of adiabatic logic architectures proposed over the years work on the same principle but differ in the structure and complexity. The quasi-static energy recovery logic (QSERL) circuit [8] overcomes the drawbacks of the previous reported ERL families but it suffers from in-robustness and output floating. Complementary energy path adiabatic logic (CEPAL) have better performance in terms of improvement in robustness and throughput to the QSERL circuit [9] but it have some drawbacks also, i.e. one extra MOSFET diodes in charging and one in discharging path produces a little bit larger power dissipation. In GFCAL circuit [10] for a logic gate of M inputs, it requires 2M transistors and 2 diodes and is operated by a single triangular power source and does not need multi-phase clocks. The triangular power supply causes lowest power dissipation than the other types of power clocks (sinusoidal and trapezoidal). The drawback is that the triangular power supply causes large delay at the output this can be tolerated in small circuits but in larger circuits like counters, multipliers etc this delay prevents the cascadability.

In this paper, authors propose a solution to improve the performances of GFCAL based circuits along with their simulation results and performance evaluations. All these circuits have been found to save approximately 50% or above power compared with CMOS circuits. The paper is organized into eight sections. Section 1 deals the introduction part. Section 2 describes the CMOS circuit and adiabatic circuits. In section 3 & 4 authors have review of reported adiabatic circuits & problems in existing GFCAL circuit respectively. Section 5 includes proposed approach for performance improvement and 6 and 7 gives performance analysis & discussion and conclusion respectively. In section 8 relevant references are shown.

2. CMOS CIRCUIT VERSUS ADIABATIC LOGIC CIRCUIT

2.1 CMOS Circuits
In CMOS circuit dominant source of power dissipation is due to the switching operation. During the switching operation power is dissipated in charging or discharging the parasitic capacitances during the voltage transition of the nodes. A node capacitance C_L is charged from 0 to V_{dd}, and an amount of $V_{dd}Q$ ($=C_LV_{dd}^2$) energy drawn from the supply. In charge up phase one half of this energy i.e. ½ $C_LV_{dd}^2$ is dissipated as heat in conducting pMOS transistor, and other half energy i.e. ½ $C_LV_{dd}^2$ is stored in load capacitances. The energy which was stored in output load capacitance is dissipated in nMOS transistor in charge down phase. One can reduce this switching energy dissipation by reducing the supply voltage and physical capacitance. But there is a limitation, while reducing $V_{dd,}$ sub threshold leakage current increases. Physical capacitances may be decreased by reducing the sizes of devices but this affects the driving capability and speed.

2.2 Adiabatic Logic Circuits

In adiabatic switching for charge up phase, the output load is charged very slowly compared to its' time constant such that the voltage drop across the switching pMOS transistor is very small. In this way the energy dissipation which occurs due to the finite rate of change of driving voltage is decreased.

In charge down phase instead of ejecting the charge to ground in each clock cycle, circuit is designed so that the charge can flow back to the power clock. In the circuit of Fig. l(b), the supply V_{Φ}, swings gradually from 0 to V_{dd} . The peak current can be significantly reduced by ensuring uniform charge transfers over the entire available time. Due to this there will be very little voltage drop across the channel of pMOS transistor, and hence very small amount of energy is dissipated. A simple method to estimate the power dissipation in this case is:

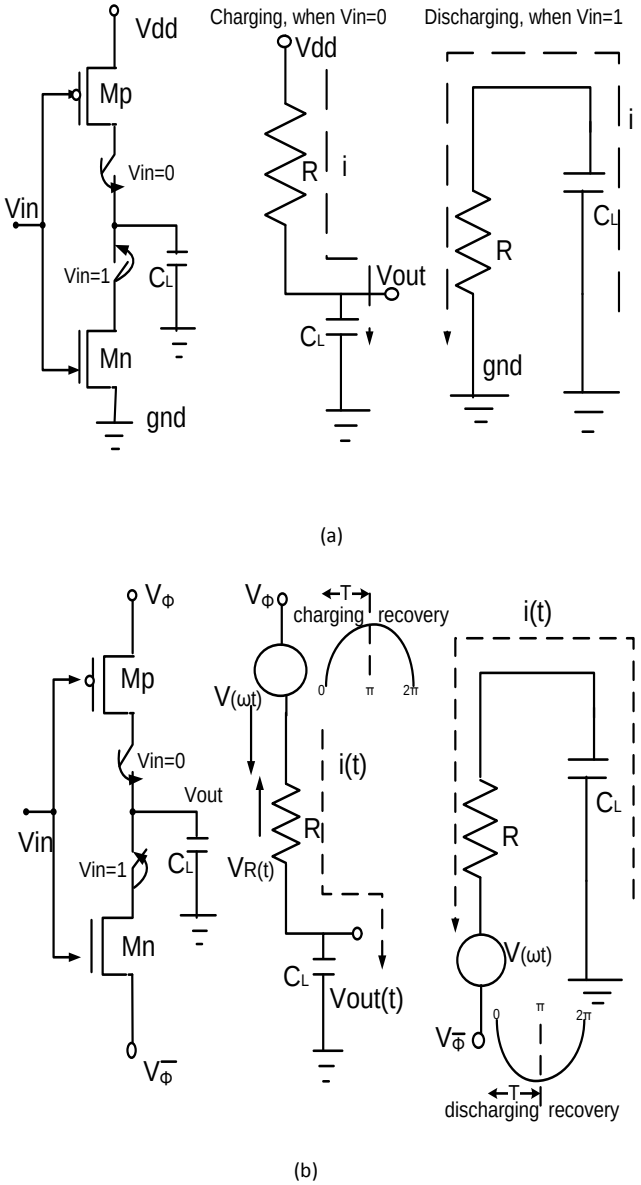


Fig. 1. A model showing charging and discharging (a) CMOS circuit, (b) Adiabatic logic circuit

$$E_{diss} = i^2 RT = \left(\frac{RC_L}{T}\right) C_L V_{dd}^2 \quad (1)$$

Where R is the channel resistance and T is the input transition time. It is well known that RC< 1 ns for a moderate fan out, and T =l/f, thus Ediss will be very small when the operating frequency f =10 MHz.

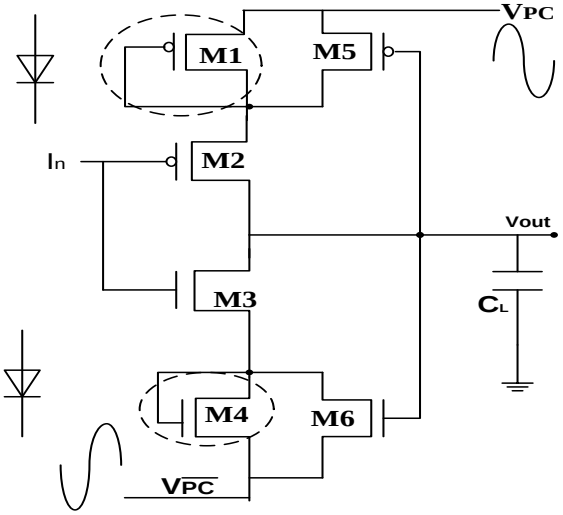
3. REVIEW OF REPORTED ADIABATIC LOGIC CIRCUITS

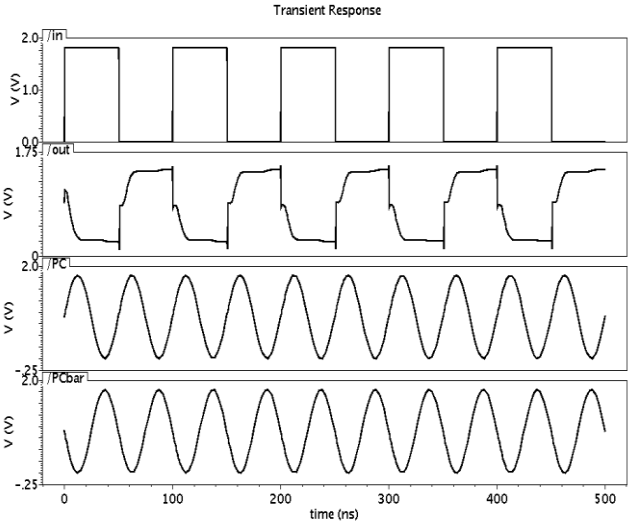
In this section authors will review some quasi adiabatic logic circuits, QSERL, CEPAL, 2PASCL, and GFCAL. The quasi-static energy recovery logic (QSERL) and complementary energy path adiabatic logic (CEPAL) circuits are shown in Fig.2(a) and Fig.2(b) respectively, QSERL circuit has two complementary sinusoidal power clocks with two phases (evaluate and hold). Due to the alternate hold phases it have drawback of floating output. Although the floating output may be eliminated by connecting a clocked feedback keeper to each logic circuit, unwanted losses still occurs.

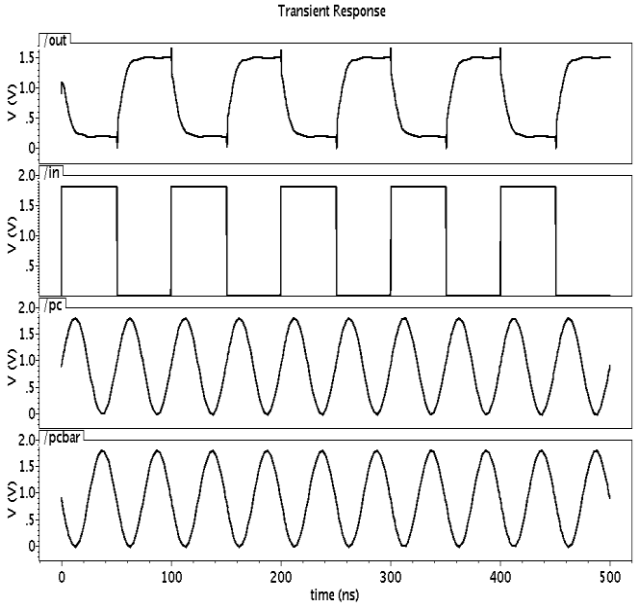
By using CEPAL circuit, one can achieve improved driving ability and robustness than QSERL circuit. Its' throughput does not depend on the frequency ratio and is better (twice) than QSERL circuit. It has some problems like having extra diodes in its charging and discharging path, which causes larger area and a bit larger power dissipation than QSERL circuits [11].

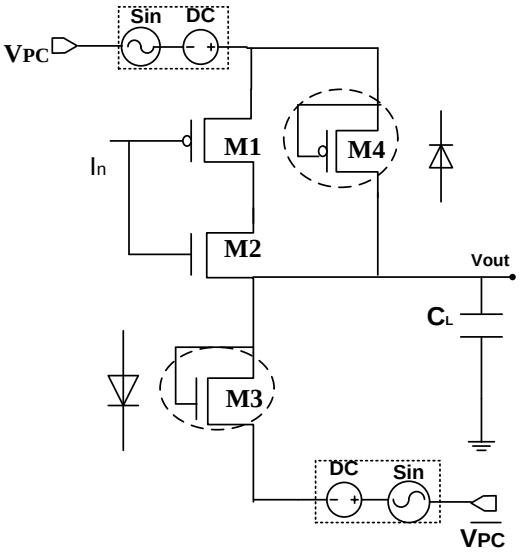
In 2PASCL [12] circuit as shown in Fig.2(c), during charging, the current flows only through the pMOS transistor because it does not have diode in the charging path. This will reduce the non adiabatic losses due to the cut in voltage of diodes. Different from the other discussed quasi adiabatic logic circuits where ramp or sinusoidal power clocks were used here two split level sinusoidal power clocks are used, which have reduced voltage difference between the electrodes hence reduced power dissipation may be achieved. It lacks in performance because of diodes in pull up (connected in parallel with pMOS) and pull down (connected in series below the nMOS) network for recycling the charges stored in the load capacitances.

The GFCAL circuit has a triangular power clock and diodes in the charging and discharging path as shown in Fig.2 (d). Triangular power clocks have lesser power dissipation than the sinusoidal and split level sinusoidal power clocks. But this type of power clock causes comparatively a large delay at the output node. Also due to the voltage drop across the diode, power dissipation (non adiabatic losses) occurs when current flow across it. Since it is well known that, diode based circuits suffers from output amplitude downgrading, thus performance becomes poor. It may be said that GFCAL have very less power dissipation in comparison to other adiabatic logic families but it suffers from very large delay and amplitude degradation at its output.

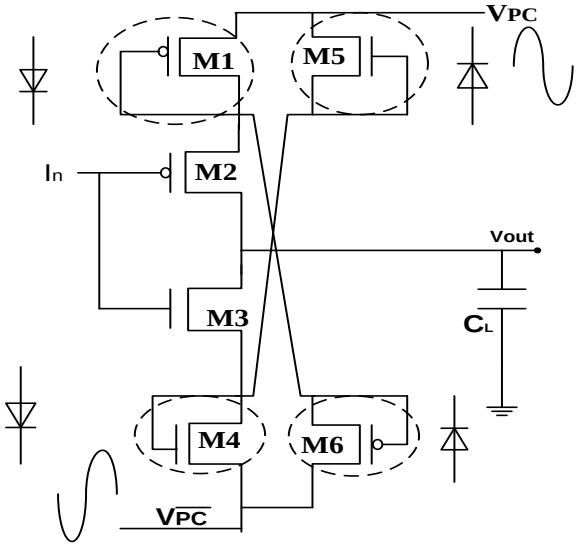

VPC
M1
M5
In
M2
Vout
M3
CL
M4
M6
VPC

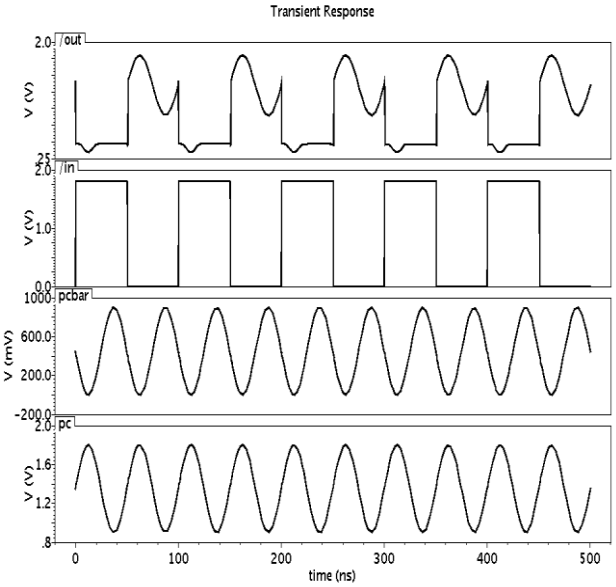

Transient Response
/in
/out
/PC
/PCbar
V (V)
time (ns)


Transient Response
/out
/in
/pc
/pcbar
V (V)
time (ns)

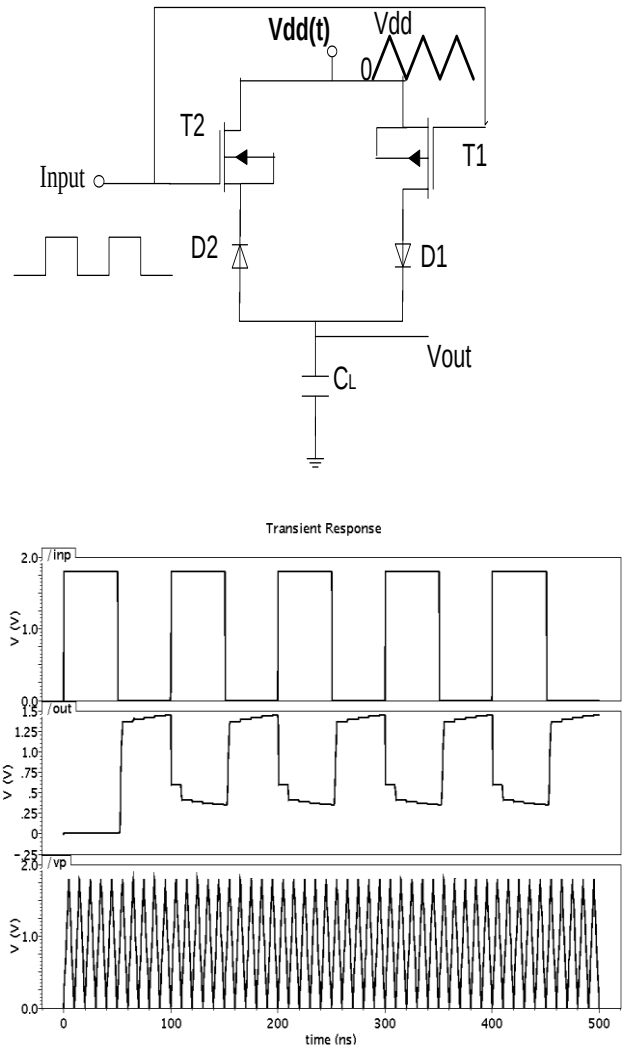

Sin
DC
VPC
In
M1
M4
M2
Vout
CL
M3
DC
Sin
VPC

(a)


VPC
M1
M5
In
M2
Vout
M3
CL
M4
M6
VPC


Transient Response
/out
/in
/pcbar
/pc
V (V)
V (mV)
time (ns)

(c)



(d)

Fig. 2. Adiabatic logic inverter circuits and their simulation waveforms (a) QSERL, (b)CEPAL, (c)2PASCL, (d)GFCAL

4. PROBLEMS IN EXISTING GFCAL CIRCUITS

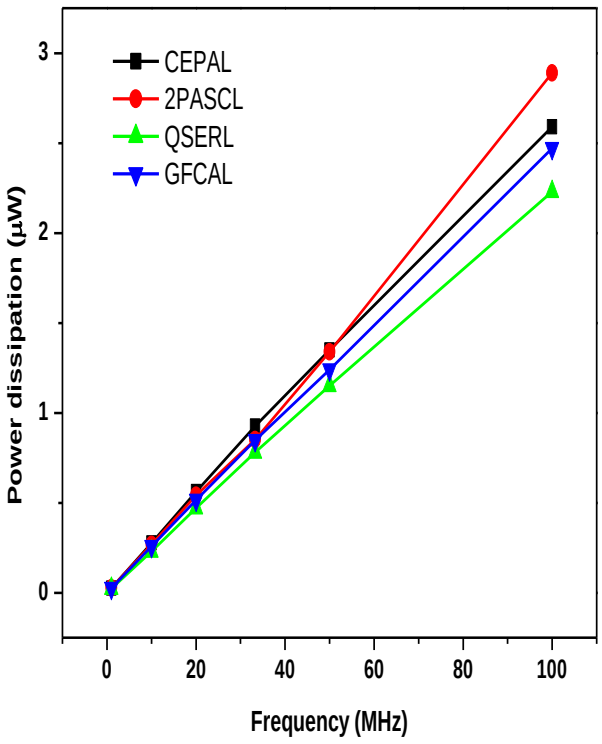
4.1 GFCAL Inverter Circuit Description & Operation

The circuit consists of one p channel MOSFET (T1) followed by a diode (D1) in same path, and one n channel MOSFET (T2) with a diode (D2) in parallel as shown in Fig. 2(d). The supply voltage $V_{dd}(t)$ is a slowly varying triangular waveform. When $V_{dd}(t)$ is rising and input is LOW, T1 ON and T2 OFF. The path T1 D1 allows the capacitor to charge upto the peak value V_{dd} producing logic HIGH. When $V_{dd}(t)$ falling and input LOW, capacitor remains charged due to the diode (reverse biased) and output logic retains its state. When $V_{dd}(t)$ rising and input is HIGH,T2 ON and path T2 D2 allows discharging when the output is higher than V_{dd} (t). This discharge happens only for a small duration. When $V_{dd}(t)$ falling and input is HIGH, the output capacitor gets discharged in case it was previously charged.

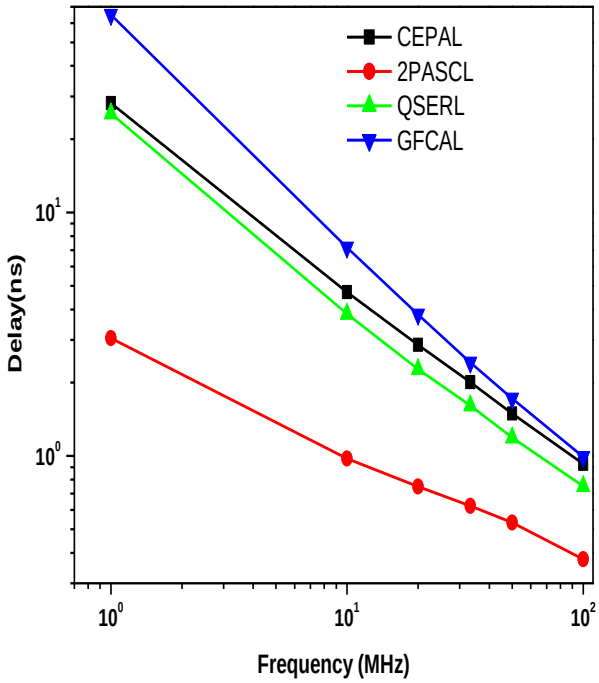
4.2 Comparison of Performances of GFCAL Inverter to the Reported Adiabatic Inverters & Problem Formation

To compare the performance of GFCAL inverter with other reported adiabatic inverters all the inverters are simulated with same W/L ratio (240nm/180nm) using VIRTUOSO SPECTRE SPICE simulator of cadence. The MOS model used is BSIM3v3.2. Performances of these inverters have been evaluated in terms of power and delay with variation in input frequency and load capacitances. For frequency analysis load capacitance is set to 20fF and for load analysis, frequency of power clock and input is set to 80 MHz and 40MHz respectively.

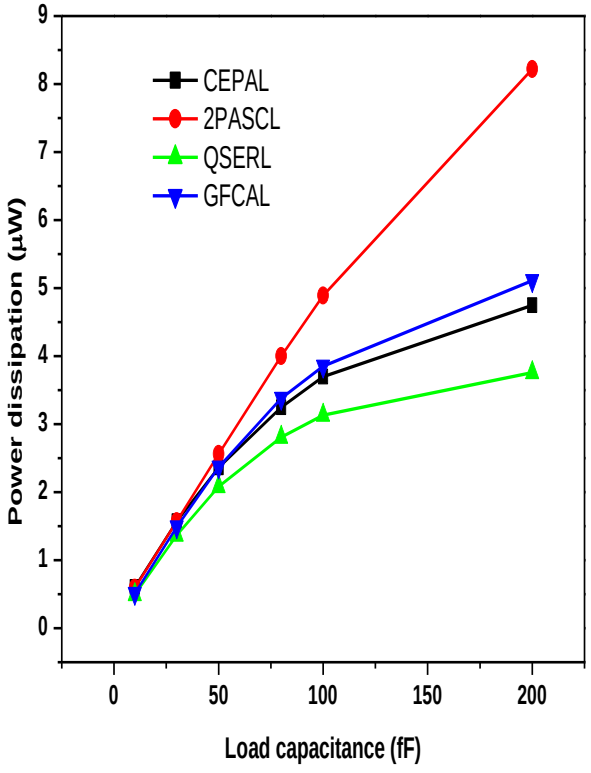
It may be observed from the Fig.3 (a) that as frequency increases power dissipation in all the adiabatic inverters increases, whereas QSERL and GFCAL inverters have lower power dissipation up to 100MHz than others. However QSERL has lowest power dissipation among all but it has output floating related problem, so GFCAL is a good choice as far as power efficiency is concerned. In Fig.3 (b) we may observe that GFCAL has largest delay throughout the whole observed frequency, so it may be concluded that it cannot be used in high speed devices. From the Fig.3(c) and Fig.3 (d) it is observed that GFCAL have poor performance with the load capacitance so there is a scope of performance improvement in terms of delay with load capacitance and frequency in GFCAL by some design modifications.



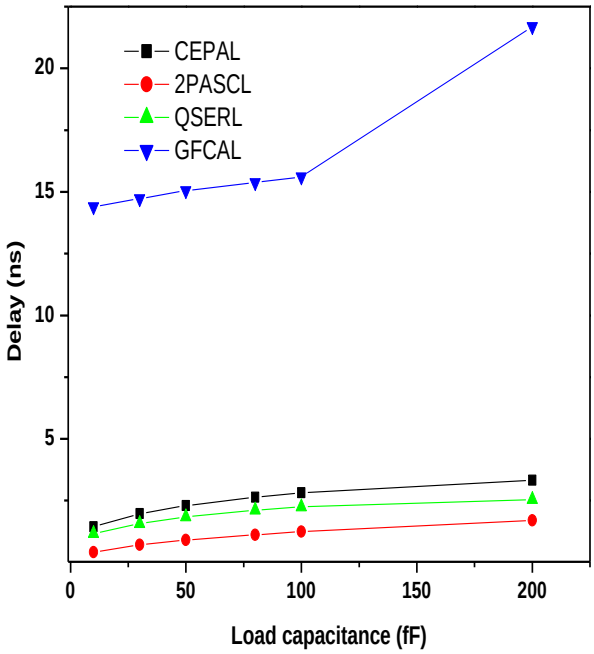
(a)



(b)



(c)



(d)

Fig. 3. Comparison of performances of reported adiabatic inverters to the GFCAL inverter with variation in frequency and load capacitance.

5. PROPOSED APPROACH FOR PERFORMANCE IMPROVEMENT

Based on the discussions of previous sections we know that the major drawback of GFCAL circuits is the large delay at its output. The approach to delay reduction attempts to ensure that the supply voltage is a sinusoidal or trapezoidal instead of triangular power clock. Also by sizing of charging/discharging transistors and by increasing the frequency ratio (power clock frequency to the input frequency) delay is reduced further. In the following section authors will observe and improve the performance of reported GFCAL circuit by the proposed approach.

In recent years various adiabatic logic styles have been proposed which emphasis on combinational circuits like CLA, ALU and multipliers etc. [12]-[26]. Since it is known that sequential circuits like flip-flops, counters and memory circuits are also very important in digital circuit design and it is not possible to design adiabatic sequential circuits [27]-[29] using conventional method, so the proposed approach is based on these circuits and their performance improvement.

5.1 Negative Edge Triggered GFCAL JK Flip Flop

The latches are generally designed by connecting two inverters or two NAND/NOR gates in a cross coupled manner. The GFCAL master slave JK flip flop had been implemented using GFCAL NAND gates (two 3 input and six 2 input) and a GFCAL inverter as shown in Fig. 4(a). The structure of GFCAL NAND gate is already shown in [10]. The inputs are J and K along with the clock signal CLK. Q and Qbar are the outputs where Qbar is the complement of Q.

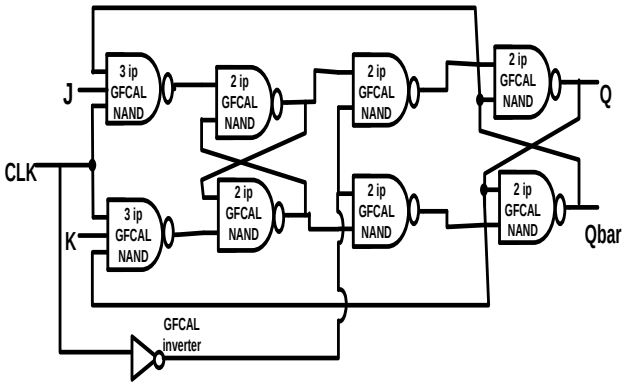
Simulated timing waveforms are shown in Fig.4(b). The combination of inputs at each negative edge of clock pulse '10, 11, 01' are given in the form of strings. The output Q and

Qbar changes according to the inputs at each negative edge of clock pulse. Q= '1' and Qbar= '0' when J='1' and K= '0'. Similarly Q= '0' and Qbar= '1' when J= '0' and K= '1'. Output Q will be complemented when J= '1' and K= '1'. Further the outputs Q and Qbar are latched to their corresponding values other than the negative edges of clock pulses. It may be observed that the waveforms of outputs Q and Qbar have ripples that are due to the continuous charging and discharging through the time varying triangular power clock.

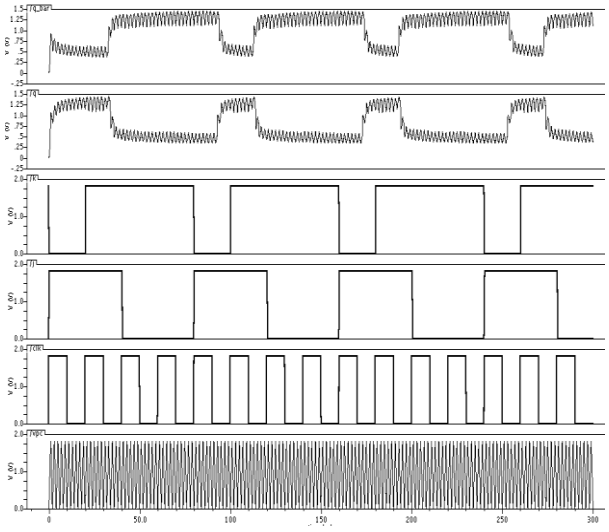
5.2 GFCAL based 3 bit UP Counter

The 3 bit binary up counter has been implemented using 3 GFCAL negative edge triggered master slave JK flip flop for each binary bit as shown in Fig. 5(a). This counter will increment once for every clock cycle and count from zero to seven before it overflows.

Simulated timing waveforms of 3 bit up-counter are shown in Fig. 5(b). Q2 is always toggle at each negative edge of clock pulse (J and K are HIGH). Q1 is toggle at negative edge of Q2. Similarly Q0 is toggle at negative edge of Q1. Supply clock is triangular waveform. The combination of outputs (Q2Q1Q0) at different negative edge of clock pulse is '000,001,010,011,100,101,110,111'.



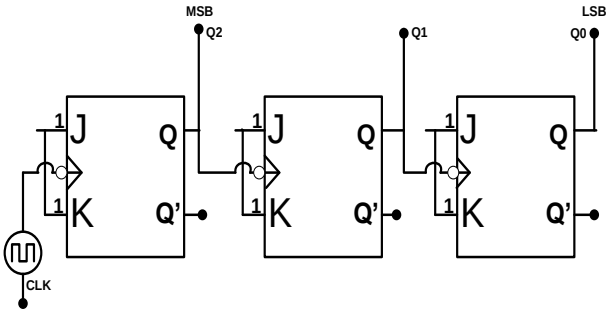
(a)



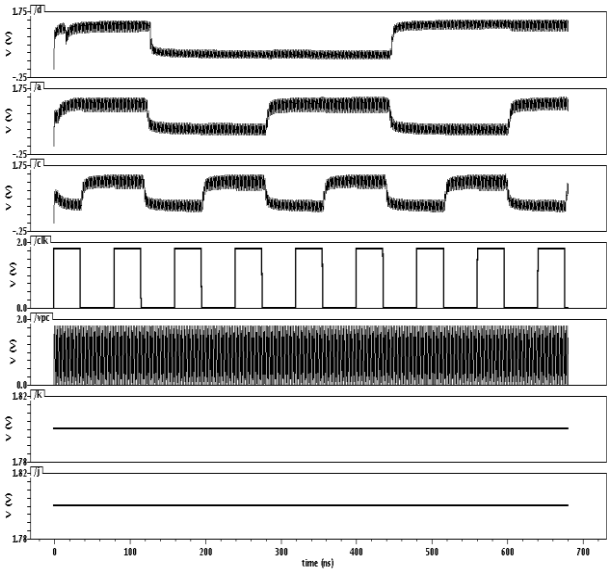
Time (ns)

(b)

Fig. 4. GFCAL JK flip flop (a) circuit diagram, (b) its simulation waveforms



(a)



Time (ns)

(b)

Fig. 5. GFCAL based 3 bit counter (a) circuit diagram, (b) its simulation waveforms

5.3 GFCAL based 6T-SRAM

Read write memory circuits are designed to access modification of the data bits to be stored in the memory array. The GFCAL 6T-SRAM may be implemented using two GFCAL inverters connected in a cross coupled manner where the output potential of each inverter V2 and V1 is fed as input into the other. This feedback loop stabilizes the inverters to their respective state. Two active nMOS pass transistors are used to pass the bits. To access read and write (the data contained/to be contained in the memory cell) two bit lines (BL and $\overline{BL}$) are used. The nMOS pass transistors are controlled by word line (WL) as shown in Fig. 6(a).

When word line is low, turning the access transistors off. In this state the inverters are in complementary state. When the p-channel MOSFET of the left inverter is turned on, the potential V2 is high and the p-channel MOSFET of inverter 2nd is turned off, V1 is low. To write information the data is imposed on the bit line BL and the inverse data on the inverse bit line, $\overline{BL}$ then the access transistors are turned on by setting the word line to high. As soon as the information is stored in

the inverters, the access transistors can be turned off and the information in the inverter is preserved. Simulated timing waveforms of 6T SRAM are shown in Fig.6 (b).

6. PERFORMANCE ANALYSIS & DISCUSSIONS

The presented 3 bit counter is asynchronous counter thus its delay will be large but due to its simplicity it have been frequently used in literature. As authors observed in the JK flip flop circuit (shown in fig. 4) that triangular power clock produces such a large delay at the output that one cannot get proper output of larger circuits. So authors used sinusoidal and trapezoidal power clocks one by one keeping other parameters same as before. It is observed that delay with sinusoidal and trapezoidal power clocks reduced in a significant amount and result is a proper correct output.

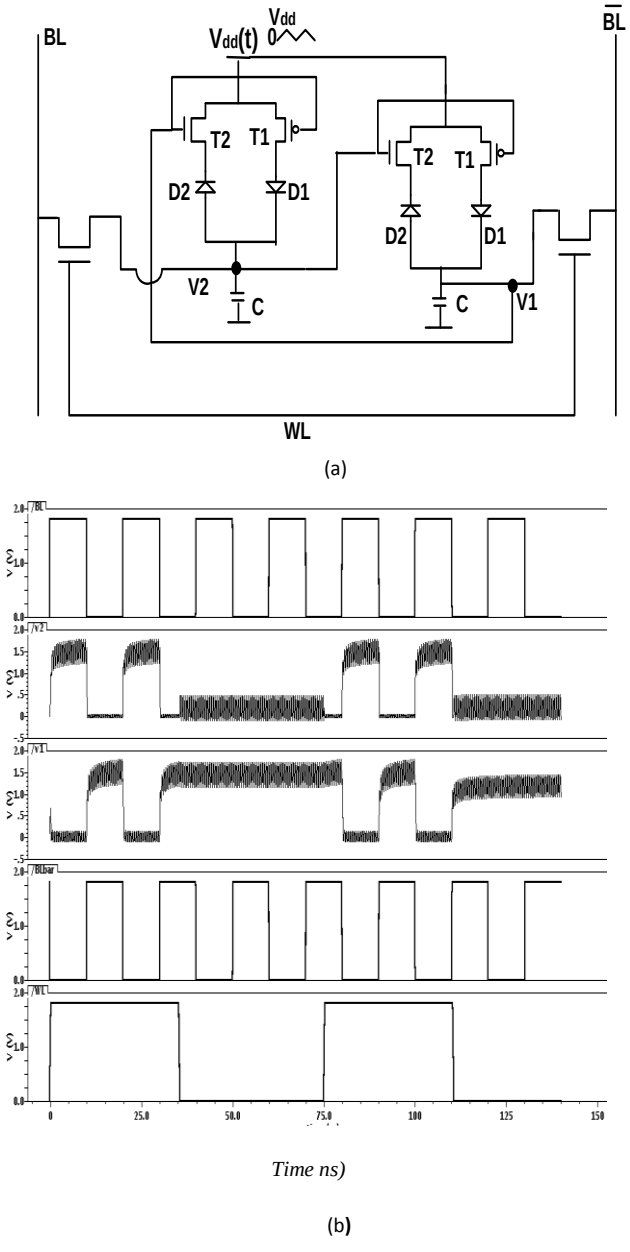


Fig. 6. GFCAL based 6T SRAM (a) circuit diagram, (b) its simulation waveforms

For performance analysis authors have taken the supply voltages as slowly varying triangular, sinusoidal and trapezoidal waveforms. Frequency of power clock is set to 40 times to the frequency of input signal also the sizes of nMOS transistors (W/L=0.72/0.18 nm) is kept larger than the sizes of pMOS transistors (0.24/0.18 nm) to reduce such a large delay at the flip flop output. The simulations have been done in 0.18µm CMOS/BSIM3v3.2 process in VIRTUOSO SPECTRE SPICE simulator of CADENCE.

The comparison of a GFCAL based JK flip-flop, 3 bit counter and 6T SRAM circuits with similar circuit parameters (f_{in}=12.5 MHz, f_{pc}=500MHz and V_{DD}=1.8V) and different shapes of power clocks has been shown in Table 1. Here it should be noted that since CMOS circuits are operated by DC power supply so authors used a 1.8V DC source for all the CMOS based circuits.

It is observed that GFCAL based counter, JK flip flop and 6T SRAM cell exhibits a power saving of up to 73%, 54.7% and 66% respectively with an increase in delay to their respective CMOS circuits but this increased delay has been reduced by proposed remedies like by using sinusoidal and trapezoidal power clocks and by transistor sizing (Width of transistors is increased). The delay of GFCAL based JK flip flop for triangular power clock have been reduced to 46%, 49% respectively for sinusoidal and trapezoidal power clocks. However the delays of GFCAL based counter for triangular power clock have been reduced to 40%, 60% sinusoidal and trapezoidal power clocks respectively and for GFCAL based 6T-SRAM it is reduced to 17% and 91% over sinusoidal and trapezoidal power clocks respectively.

Table 1. Comparison of GFCAL based sequential circuits

	Adiabatic Power supply			**DC power supply**
	Triangular	**Sinusoidal**	**Trapezoid**	
GFCAL JK flip flop				**CMOS JK flip flop**
Power dissipation in 8 cycles(µW)	4.2	4.64	7.01	15.6
Delay (ns)	7.89	4.2	4	0.38
GFCAL 3 bit counter				**CMOS 3 bit counter**
Power dissipation in 8 cycles(µW)	8.33	10.5	17.5	18.4
Delay (ns)	14	8.4	5.6	1.36
GFCAL 6T SRAM				**CMOS 6T SRAM**
Power dissipation in 8 cycles(µW)	0.4	1.02	1.3	1.2
Delay (ns)	0.12	0.1	0.01	0.13

7. CONCLUSION

In this paper authors have presented a GFCAL based JK flip flop, 3 bit up counter and 6T SRAM circuit and its performance with different type of power clocks have been evaluated in terms of power dissipation and delay. It is concluded that GFCAL based circuit with sinusoidal and trapezoidal power clocks have very less delay than the triangular power clock based circuits with a very small incremented power dissipation however overall PDP is very less compared to conventional CMOS circuits.

8. REFERENCES

[1] Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwati,"New Design Methodologies for High Speed Mixed- Mode Full Adder Circuit", International Journal of VLSI and Communication Systems (VLSICS), AIRCC Publication, 2(2), 2011, 78-98,2011.

[2] Adarsh Kumar Agarwal, S. Wairya, R.K. Nagaria and S. Tiwari, "A New Mixed Gate Diffusion Input Full Adder Topology for High Speed Low Power Digital Circuits", World Applied Science Journal (WASJ),Special Issue of Computer & IT, 7, 2009, 138-144.

[3] D. A. Hodges, H. G. Jackson, and R. A. Saleh, Analysis and Design of Digital Integrated Circuits, 3rd ed. New York: McGraw-Hill, 2003.

[4] N. H. E.Weste and D. Harris, CMOS VLSI Design–A Circuits and Systems Perspective, 3rd ed. Reading, MA: Addison-Wesley, 2004.

[5] Vivek K. De and James D. Meindl, "Opportunities for non-Dissipative Computation", in, *IEEE Conf., 1995*, 297–300.

[6] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. Y.-C. Chou, "Low-power digital systems based on adiabatic-switching principles," IEEE Trans. VLSI Syst., 2, Dec. 1994, 398–407.

[7] Y. Moon and D.-K. Jeong, "An efficient charge recovery logic circuit," IEEE J. Solid-State Circuits, 31(4), Apr. 1996, 514–522.

[8] Yibin Ye, And Kaushik Roy , "QSERL: Quasi-static Energy Recovery Logic", IEEE Journal Of Solid-state Circuits,36(2), Feb 2001, 239-248.

[9] Cihun-siyong Alex Gong, Muh- Tihan Shiue, Ci-Tong Hong, And Kai- Wen Yao, "Analysis and Design of an Efficient Irreversible Energy Recovery Logic in 0.18-µm CMOS", IEEE Transactions On Circuits and Systms- I: Regular Papers, 55(9),Oct 2008, 2595-2607.

[10] N.S.S. Reddy, M. Satyam,and K.L. Kishore, "Cascadable Adiabatic Logic Circuits for Low-Power Applications", IET Circuits Devices Syst., 2(6), Jun 2008, 518–526.

[11] Nazarul Anuar, yashuhiro Takahashi, and Toshikazu Sekine, "LSI implementation of a low-power 4x4-bit array two-phase clocked adiabatic static CMOS logic multiplier",Microelectronics Journal, Elsevier, 43, 2012, 244-249.

[12] Shipra Upadhyay, R.A. Mishra, R.K. Nagaria and S.P. Singh, "DFAL: Diode Free Adiabatic Logic Circuits", International Scholarly Research Network: ISRN Electronics, Hindawi, 2013, 1-12.

[13] Sompong Wisetphanichkij, Kobchai Dejhan, "The Combinational and Sequential Adiabatic Circuit Design and Its Applications", Circuits Syst Signal Process , 28,2009, 523–534.

[14] Conrad H. Ziesler, and Marios C. Papaefthymiou, "A True Single-Phase Energy-Recovery Multiplier",Suhwan Kim, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 11(2),Apr 2003,.52-63.

[15] Mehrdad Khatir, Alireza Ejlali, Amir Moradi,"Improving The Energy Efficiency of Reversible Logic Circuits by The Combined Use of Adiabatic Styles", Integration the VLSI Journal, Elsevier, 44, 2011, 12-21.

[16] Visvesh S. Sathe, Juang-ying Chueh, and Marios C. Papefthymiou,"Energy Efficient GHz-Class Charge Recovery Logic", IEEE Journal of Solid-state Circuits, 42(1), Jan 2007,38-47.

[17] Myeong-Eun Hwang, Arijit Raychowdhury, and Kaushik Roy,"Energy-Recovery Techniques to Reduce On-Chip Power Density in Molecular Nanotechnologies", IEEE Transactions on Circuits and Systems—i: regular Papers, 52(8), 2005, 1580-1589.

[18] A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," IEEE Journal of Solid-State Circuits, 30(3), 1995,311–314.

[19] K.W. Ng, K.A. Ng, K.T. Lau, "Energy-recovery flip-flop design using improved adiabatic pseudo-domino logic structure", Microelectronics Journal, Elsevier, 30, 1999, 851–854.

[20] Jouko Marjonen and Markku A. Berg, "A Single Clocked Adiabatic Static Logic—A Proposal for Digital Low Power Applications", Journal of VLSI Signal Processing, Kluwer Academic Publishers, 27, 2001, 253–268.

[21] V. I. Starosel'skii, "Adiabatic Logic Circuits: A Review", Russian Microelectronics, vol. 31, no. 1, pp. 37–58, translated from Mikroelektronika, 31(1), 2002, 42–65.

[22] V. V. Losev and V. I. Starosel'skii, "Power Consumption of Asymptotically Adiabatic Static Logic Gates", Russian Microelectronics, vol. 33, no. 3, 2004, pp. 188–194, translated from Mikroelektronika, 33(3),2004, 233–239.

[23] Peng-jun WANG, Jian XU, Shi-yan YING, "Design of adiabatic two's complement multiplier-accumulator based on CTGAL", Journal of Zhejiang University SCIENCE A, Springer, 10(2),2009, 172-178.

[24] Jianping Hu, Dong Zhou, Ling Wang, Huiying Dong, "Low-power interface circuits between adiabatic and standard CMOS circuits", Analog Integrated Circuits and Signal Processing, Springer, 60, 2009,105–115.

[25] Wang Pengjun and Yu Junjun, "Design of Two-Phase Sinusoidal Power Clock and Clocked Transmission Gate Adiabatic Logic Circuit", Journal of Electronics (China), 24(2),2007, 225-231.

[26] A. Blotti, R. Saletti, "Ultralow-power adiabatic circuit semi-custom design", IEEE Transaction on VLSI Systems, 12(11), 2004, 1248–1253.

[27] Y. Wu, H. Dong, Y. Wang, and J. Hu, "Low-power adiabatic sequential circuits using two-phase power-clock supply," in ASIC, 2005. ASICON 2005. 6th International Conference on ASIC proceedings, 1, 2005, 235 –238.

[28] Shipra Upadhyay, R. K. Nagaria and R. A. Mishra,"Complementary Energy Path Adiabatic Logic based Full Adder Circuit",A Journal of World Academy of Science Engineering & Technology, 66, 2012, 161-167.

[29] Shipra Upadhyay, R.K. Nagaria, R.A. Mishra, S.P.Singh and Amit Shukla, Triangular Power Supply Based Adiabatic Logic Circuits, World Applied Sciences Journal (WASJ), (accepted).