An Improved Analog Waveforms Generation Technique using Direct Digital Synthesizer

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ABSTRACT
In many kinds of equipment, it is important to produce readily control accurate waveforms of various frequencies and profiles such as agile frequency sources with low phase noise and low spurious signal content for communications, and simply generated frequency for industrial and biomedical applications. A direct digital synthesizer (DDS) provides many significant advantages over the PLL approaches such as Continuous-phase switching response, fine frequency resolution, Fast settling time, and low phase noise are features easily obtainable in the DDS systems. The aim of this paper starts from the DDS circuit structure and discusses the design method of DDS based on VHDL in detail.

Keywords
NCO, PLL, DAC, ADC, LPF

1. INTRODUCTION
Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. It is a method of producing an analog waveform by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Compared with traditional frequency synthesis technology, DDS' ability to accurate produced control waveform of various frequencies and profile has become a key requirement common to a number of industries [1]. A DDS has many advantages over its analog counterpart, the phase-locked loop (PLL) including much better improved phase noise, precise control of the output phase across frequency switching transitions and frequency agility[4].

The DDS modules basically constitute of three main blocks. These are Numerically Controlled Oscillator (NCO), Sine ROM Look-up Table and Digital to analog Converter (DAC). The NCO comprises the phase accumulator and logic increment register. The increment register stores the binary value of frequency control register. After that phase accumulator adds the phase increment value to its accumulator output. The accumulator output calculated is used to address the look-up table which outputs the digital sample values of sine wave at current phase value. The implementation of DDS is always stable and with finite-length control words. There is no need for gain control. This design method breakthrough the design bottlenecks in the traditional design and greatly improved the performance of the system [4] [6].

2. LITERATURE SURVEY
DDS's key component is the phase accumulator. The frequency control word K controls the rate of phase change. Under the control of the reference clock fs, the phase accumulator accumulates frequency control word K linearly. The summation then adds with the phase control word P, and finally forms the addresses to the ROM table. By address mapping, the waveform amplitude information is output to the digital-to-analog converter (DAC), and then through the Low Pass filter, the corresponding Analog waveform signal is obtained. DDS (Direct Digital Frequency Synthesizer) is a new type of frequency synthesis. It directly generates variable frequency signals by controlling the rate of change in phase. It is a digital technology [1].

A basic Direct Digital Synthesizer consists of a frequency reference (often a crystal or Surface acoustic oscillator), a Numerically Controlled Oscillator (NCO) and a DAC. The reference provides a stable time base for the system and determines the frequency accuracy, stability of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the output waveform (often a sinusoidal) whose period is controlled by the digital word contained in the Frequency Control Register (FCR). The sampled, digital waveform is converted to an analog waveform by DAC. The output reconstruction filter (LPF) rejects the spectral replicas produced by the zero-order hold inherent in the digital to analog conversion mechanism [2][3].

DDS is a powerful technique used in the generation of radio frequency signals for use in a variety of applications from radio receivers to signals generators and many more. The technique has become very popular in recent years with the advances being made in integrated circuit technology that allow much faster speeds to be handled which in turn enable higher frequency DDS chips to be made. Although often used on its own, DDS is often used in conjunction with indirect or phase locked loop synthesizer loops. By combine the both technologies it is possible to take advantage of the best aspects of each. It is used for generating versatile waveforms like sine, cosine, square and saw tooth etc. In accordance of the fact that integrated circuits are now widely available, this makes them easy to use [2] [4].

3. PRINCIPLE OF DDS
As the name suggests this form of synthesis generates the waveform directly using digital techniques. This technique is different to the way in which the more familiar indirect synthesizers that use a phase locked loop as the basis of their operation. Its basic principle is to sample the phase/amplitude of a cycle of continuous sine wave with equal phase interval,

get the discrete phase amplitude sequence of a periodic signal, and quantify its analog amplitude. Thus a periodic sine signal is converted into a series of discrete binary sequence, which is finally stored in a ROM memory. The content of each memory cell is the quantized amplitude of the sine wave [1].

A basic Direct Digital Synthesizer consists of a frequency reference (often a crystal or SAW oscillator), a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC) as shown below in Fig.1.The reference Oscillator provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the reference clock to the NCO which produces at its output a discrete-time, quantized form of output waveform (often a sinusoidal) whose period is controlled by the digital word contained in the FCR. The sampled digital waveform is converted to an analog waveform by the DAC circuit. The output reconstruction filter (LPF) rejects the spectral replicas produced by the zero-order hold inherent in the digital to analog conversion mechanism [2] [3].

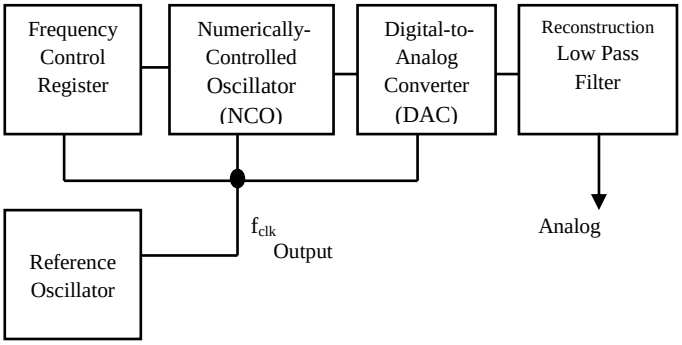

Fig. 1 A basic Direct Digital Synthesizer

In order to generate a periodical waveform at a constant frequency, a constant phase increment value is added to the phase accumulator at each reference clock cycle. A waveform at higher frequency can be generated if the phase increment value is larger. If the phase increment value is smaller, then the phase accumulator steps slower. As a result waveform at low frequency is generated. This situation can be understood as phase accumulator steps the faster through the look-up table (LUT) [7] [8].
The frequency of the waveform depends on the reference clock frequency, the phase increment register value and length of phase accumulator. The waveform frequency is calculated using the formula given below:-

$$F_{out} = \frac{(FCR \times F_{ref})}{2^m}$$

Where
F_{out} = DDS output waveform frequency
FCR = phase increment (frequency control register value)
F_{ref} = reference clock frequency
m = phase accumulator word length

If the desired wave frequency is 500 Hz and the supplied reference clock frequency is 100 MHz, phase increment value (FCR) for 32-bit accumulator is calculated as shown below:

$$FCR = \frac{(F_{out} \times 2^{m})}{F_{ref}} = \frac{(500 \times 2^{32})}{(100 \times 10^{6})} = 21475$$

The frequency resolution of the direct digital synthesizer is a function of the reference clock frequency and number of bits employed in phase accumulator. The frequency resolution is calculated using the formula given below:

$$\Delta f = \frac{F_{ref}}{2^m}$$

Where Δf = frequency resolution.
In order to obtained better frequency resolution, numbers of bits employed in the phase accumulators are increased [7] [8].

1) Signal flow in DDS:

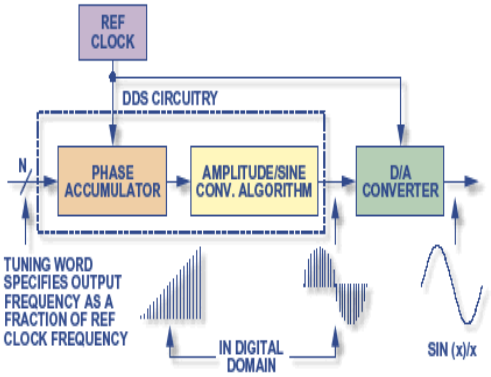

Fig. 2 signal flow in DDS

The phase accumulator is actually a modulus M counter that
Fig. 2 Signal flow through the DDS architecture

The phase accumulator is actually a modulus M counter that increments its stored number each time it receives a clock pulse [7].
The following example based on sine signal is given to explain the principles of DDS. An ideal single-frequency signal can be expressed as:-

$$F(t) = U\sin(2\pi f_o t + \theta_o) \quad (1)$$

As long as the amplitude U and the initial phase θ_0 don't change over time, its frequency can be determined uniquely by the phase.

$$\theta(t) = 2\pi f_0 t \quad (2)$$

Sampling on (2), with the sampling frequency f_s $(T_s = \frac{1}{f_s})$, the corresponding discrete phase sequence is obtained:

$$\theta(n) = 2\pi f_0 n T_s = n.\Delta\theta \quad (3)$$

Where

$$\Delta\theta = 2\pi f_0 T_s = (\frac{2\pi f_0}{f_s})$$

is the phase increment between two consecutive sample. Hence, by controlling, the frequency of synthesized signal is controlled. If the whole phase cycle 2 π is divided into q equal parts, each part δ =2 π /q, is the optional minimum phase increment. If every time the phase increment is taken as, the lowest frequency can be obtained from $\delta = 2f_{0min}T_s$. The frequency resolution is:

$$f_{0min} = \frac{\delta}{(2\pi T_s)} = \frac{f_s}{q} \quad (4)$$

After filtered, analog signal is obtained:

$$f(t) = \sin(\frac{2\pi f_s t}{q})$$

If every time the phase increment is taken as kδ, then the signal frequency is:

$$f_0 = \frac{k\delta}{(2\pi T_s)} = \frac{kf_s}{q} \quad (5)$$

The corresponding analog signal is:

$$f(t) = \sin(\frac{2\pi k f_s t}{q})$$

Where, q and k are positive integers. According to the sampling theorem, the maximum k should be less than q /2. Suppose the length of the frequency control word is N. The whole cycle is divided equally into 2N parts, thus q=2N. Substituting it into (4) and (5), we get:

$$f_{0min} = \frac{f_s}{2^N} \quad (6)$$

$$f_0 = \frac{kf_s}{2^N} \quad (7)$$

f_0 is the output frequency.

Similarly it can analysis the mathematical expression for saw tooth wave, cosine wave and square wave etc. Δθ is the phase increment between two consecutive sample. Hence by controlling, the frequency of synthesized signal is controlled [1].

4. DDS'S VHDL IMPLEMENTATION

The main part of this work is DDS'S VHDL Implementation for doing this it has to follow the following steps:-

1) Sine Wave ROM and Compression Optimization
2) Implementation of Phase Accumulator
3) Implementation of ROM Look-up Table
4) DDS Top File Implementation and Simulation

4.1 Sine Wave Rom and Compression Technique

From above principle of DDS it can see that the greater *N* (length of frequency control word), the larger the space required for lookup table. Therefore, when designing DDS, it should choice a reasonable *N*. And in accordance with waveform characteristics, use the ROM compression technology to further reduce the number of required units. For example, when synthesize a sine signal, according to it symmetry, it can stores only the magnitude value of 0~π/2. Thus the ROM size can be compressed to 1/4 of the original one. Following are the sine wave ROM compression and storage technology. Using the symmetry of the triangle function, it can only use the waveform of 0~π/2 to represent the waveform of 0~2π. The phase's highest bit is used to determine the sign of the output waveform, and the second highest bit is used to control the address of ROM table. The complete waveform can be achieved by appropriately flipping the amplitude and phase [1] [4].

5. CONCLUSION

This design uses VHDL as design language to achieve the modules of DDS, and uses Xilinx ISE 9.2i software to complete simulation. Compared with traditional frequency synthesis technology, the designed DDS has the advantages of the tuning resolution can be made arbitrarily small to satisfy almost any design specification. The phase and the frequency of the waveform can be controlled in one sample period, making phase modulation feasible. The DDS implementation is stable and with finite-length control words. There is no need for gain control. Applications of DDS include: signal generation, used as a local oscillators in communication systems, modulators, function generators, mixers sound synthesizers and as part of a digital phase-locked loop. As VHDL can describe hardware circuits and signal connection relationships; while DDS can synthesize various frequency signals directly by the digitals, their combination can quickly and easily generate a variety of frequency modulation signals, and can be quickly implemented with FPGA. By using this methodology, it can easily generate a versatile waveforms such as square wave with variable duty cycle, sine wave, cosine wave, saw tooth wave etc. This design method breakthrough the design bottlenecks in the traditional design, greatly improved the system performance. At the same time, the DDS designed by this method has high flexibility, can meet user's special requirements.

6. REFERENCES

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