Stable and Low Power 6T SRAM

Mamatha Samson
Alumni of International Institute of Information Technology
Hyderabad

ABSTRACT
In this paper an effort is made to design a stable and energy efficient asymmetrical 6T SRAM cell in 65nm technology generation with one bit line for read and one for write operation along with dual word lines. A simple energy recovery driver is added to enhance the write ability of the SRAM and to recover energy. Sizing the access transistor helps write ability and sizing of the pull down transistor provides better read stability. This circuit saves energy during write operation and also provides good read stability.

General Terms
Design, Experimentation, Performance

Keywords
SRAM, energy, stability, bit line

1. INTRODUCTION
Stable, low leakage and energy efficient SRAMs are essential for mobile applications where on chip memories are employed. But bit line charging and discharging during write operation results in most of the energy loss and is the bone of contention. It is reported that 70% of the total active power is dissipated during read and write operations [1].The power consumption of bit lines represents about 60% of the total dynamic power consumption during a write operation [2].The power consumption by bit lines is proportional to the bit line capacitance, square of the bit line voltage and the frequency of writing.

A Cache built on adiabatic principles is reported by D.Somashekar *et.al* [3] based on slowly changing supply voltages. The authors claim 85% saving for both read and write operations in the adiabatic SRAM designed by them. In this bit-line peripheral circuitry has been eliminated except for the equalization transistor. No pre-charge is used since bit-lines revert to their rest state voltage level at the end of each operation. The sense amplifier has been replaced by the adiabatic voltage level shifter and hence, short circuit current has been minimized. Three phase signal generator is needed for this design.

An energy- recovery latch/driver based on bootstrapping effect in conjunction with two phase resonant clock driver is designed for SRAM by Tzartzanis *et.al* [4]. It is claimed that the energy-recovery SRAM energy recovery resulted in significant energy savings (e.g. 59% to 76%) for the different 0.5µm SRAM parts at 200 MHz. The imbalance in load capacitances will affect the operation of the clock driver.

The design of an energy-recovering (a.k.a. adiabatic) static RAM with a novel driver that reduces power dissipation by recovering energy from the bit/word line capacitors and powered by a single-phase sinusoidal power-clock is reported by Johee Kim *et.al* [5] reported SRAM that delivers read and write operations with single-cycle latency. The driver circuit is complex and large in size. This design uses low bit line pre charge levels. The sense amplifier has to be replaced by a modified sense amplifier. The percentage energy saved is only 37.8% during write cycle.

J.Kim *et.al* [6] reported an energy recovery SRAM which saves energy from bit lines and only during write operation. Non selective pre charging is used after write cycles to maintain the capacitance load fixed. Conventional pre charging is used for read operation. The authors report an energy saving of 79% during write cycle when compared to conventional SRAM.

In [7] J.Kim *et.al* reported an energy recovery SRAM with a constant –load in which a dummy bit line capacitance is provided for each pair of bit lines in order to provide a constant load to the charging source during all the operation cycles including idle cycles. 53% of power saving is reported when compared to its conventional counterpart at 400MHz and 2.5V during write cycle. Non write cycles are reported to be more dissipative than in conventional SRAMs.

Shunji Nakata [8] reported that the energy during writing is saved by the help of high resistivity switches one connected in between SRAM and VDD and the other between SRAM and ground. The switches are operated in such a manner that while writing, the power supply voltage to the SRAM is gradually changed from ground level to VDD level.

The write scheme with differential voltage swing of a bit-line obtained by recycled charge from its adjacent bit-line capacitance instead of the power line is implemented and reported by Keejong Kim *et.al* [9]. Although this reduces the total power dissipation, this scheme employs many power switches and reference generating circuit resulting in additional area over head. Read SNM is found to be degraded by 38% compared to conventional SRAM.

Byung-Do Yang [10] employ the energy recycle method both during reading as well as writing of of 6T SRAM unlike that of [9] in which recycling of the energy is done only during writing. The author claims no degradation of Static Noise Margin, saving of 17% read power and 84% of write power. But the speed of operation is limited to 145MHz. The circuit has an area overhead of pre charge-recycling startup circuit.

The Adiabatic SRAM reported by Jun-Jun Yu *et.al* [11] makes use of Clocked Transmission Gate Adiabatic Logic (CTGAL) Circuit for all the circuits associated with SRAM except the storage cell and two phase power clocks. Hao-I Yang *et.al* [12] have reported the 8T SRAM with floating bit line Read/Write Scheme and write assistant circuit.

Shunji Nakata *et.al* [13] reported an adiabatic SRAM with shared ports for reading and writing. Writing is made easy by changing the ground line voltage gradually to half of VDD and the memory cell ground line is set in a high impedance state. The data is written adiabatically to one of the bit lines. During reading the voltage swing of the global bit line is

reduced to VDD/4 slowly by which the authors claim solving the electro migration problem.

The authors in [14] describes an asymmetric single-ended 6T SRAM bit cell that improves both Read Static Noise Margin (RSNM) and Write Noise Margin (WNM) for the same bit cell area as a conventional symmetric 6T by using single ended writing and differential sensing. An asymmetric 6T SRAM cell was proposed to enhance the static-noise margin (SNM) [15] by selective use of a weak pull down transistor. From the above description it is clear that there is scope of improvement in SRAMs with respect to energy saving keeping and its performance parameters.

2. ENERGY EFFICIENT 6TSRAM – OPERATING PRINCIPLE

The driver circuit consists of an N and a P MOSFET connected to the capacitance load through diodes. When the input signal say 'Din' is low, the capacitance charges to the peak value of the power clock voltage 'Vpc' through D2.When the input signal is low, the charges stored in the capacitance is pumped back to the signal generator through D1 when the capacitor voltage is less than the power clock voltage. Hence there is very less loss of energy as we use the adiabatic principle. In order to make use of the driver to save energy in bit line, one driver is needed for one bit line. The energy saved is proportional to $1/2C_{BL}V^2$ where 'C_{BL}' stands for the bit line capacitance and 'V' stands for bit line voltage. Energy dissipated driving the load is minimum as the voltage drop across the driver is minimum. The bit line capacitance depends on the number of rows and the technology. The

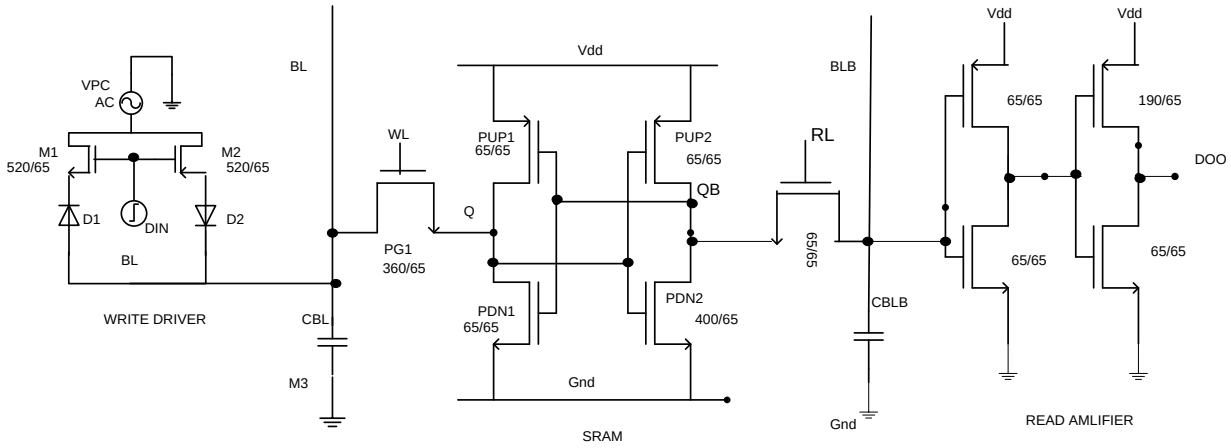

Figure 1. Circuit diagram of Enhanced Asymmetric 6T SRAM with write driver and read amplifier

waveforms of the storage nodes, word line for read, bit line read amplifier output during write, hold and read are as shown in the Fig. 2 and those for adiabatic SRAM are shown in the Fig. 3. The buffered data in complement form is applied to the write driver and then the word line signal is activated. As the resistance of the access transistor and the driver resistance is small, writing is made easier and the cell changes state. Prior to reading pre charging is not used and the charge on the bit line is used during reading operation. If no level change is needed during read

In view of this, investigations have been carried out to arrive at memory cell structure which is stable, writable and energy efficient. In this paper an effort is made to design a asymmetric 6T SRAM with two word lines and with a simple energy recovery driver for write bit line in 65nm technology using Predictive Technology models[19] to arrive at stable and energy efficient SRAM. JUNCAP1 of level 4 model is used for diodes. All voltage levels are same and are equal to 1.1V. An ideal dc shifted by 0.55V sinusoidal power clock operating with frequency equal to 100MHz is assumed.

Section2 explain briefly working of energy efficient SRAM .Section3 discusses performance of the energy saving SRAM and section 4 compares with the non adiabatic type followed by conclusion in the last section.

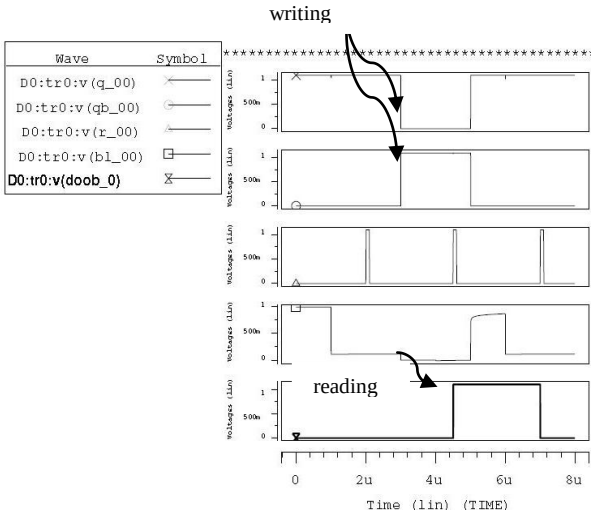

Figure 2. Waveforms during write, hold and read operation of non adiabatic SRAM with single ended read amplifier

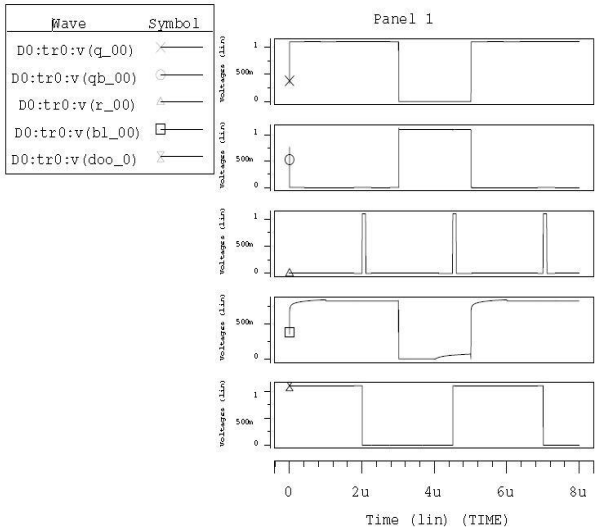

Figure 3. Waveforms during write, hold and read operation of energy efficient SRAM with single ended read amplifier

operation the bit line charges are retained on the line.

Reading is done by single ended double stage amplifier. The inverters are sized keeping in mind the read delay. Hence the input stage is sized smaller than the second stage. The width of the second stage pull up transistor is made large to drive the large output load capacitance. The size is generally chosen considering the ratio of the load capacitance to the input capacitance.

Load capacitance of first inverter:

$$CL1 = (Cdp1 + Cdn1) + (Cgp2 + Cgn2) + Cw \quad (1)$$

Where C_{dp1}, C_{dn1} are diffusion capacitances of first inverter devices

C_{gp2}, C_{gn2} are gate capacitances of second inverter devices

C_w is the wiring capacitance

The size of each inverter in a chain of inverters is the geometric mean of its neighbors' sizes.

The sizing factor 'f' is derived to be

$$f = \sqrt[N]{CL/Cg1} = \sqrt[N]{F} \quad (2)$$

F is the effective fan out of the circuit and equals $CL/Cg1$

N is the number of stages. In this case N=2, f=3, C_{g1} is the input capacitance of the input or first stage, CL is load capacitance of the second stage

3. PERFORMANCE OF ENERGY SAVING SRAM

Although the working principle is similar to 6T SRAM performance parameters are altered due to asymmetric nature. The design is done to enhance the read stability during reading '1' and also to write '0'.Writability has been increased by using bigger access transistor. The SNM is improved compared to a symmetric6T SRAM by increasing the width of the pull down N transistor connected to the read bit line. The performance parameter values are measured and illustrated as shown in the figures. Static noise margin is higher than symmetrical 6T SRAM as the single ended reading operation does not change the voltage levels of the latch. No pre charging is used before read operation and the activity on the read bit line has been reduced because of this. In addition to this only one bit line takes part in the write /read operation and hence results in lesser energy consumption.

4. COMPARISON OF PERFORMANCE OF NON ADIABATIC ASYMMETRIC 6T SRAM CELL AND ADIABATIC ASYMMETRIC 6T SRAM CELL

The performance of the energy saving SRAM was compared with the non adiabatic 6T Asymmetric SRAM with the help of bar graphs. The performance parameters considered are total energy, write delay, read delay, static noise margin and write margin.

4.1 Total energy of the SRAM system

The total energy consumed by the system includes the energy drawn by the SRAM, reading and writing circuitry. But the difference arises because of active power which is due to writing and reading. Energy consumed during reading is similar in both the non adiabatic and the adiabatic SRAM because the charges flow from the bit line connected to the node storing '0' through the pull down transistor into the ground. The quantity of energy lost during reading however is controllable by restricting the time of discharge. The energy lost during writing is around 60% of the total dynamic energy. This energy is pumped back and is saved in the proposed adiabatic SRAMs. It is seen in the Fig.3 that the energy consumed in the adiabatic 6T SRAM with single ended read amplifier is comparatively lesser. It is found that 50.6% of the total energy is saved by the adiabatic SRAM.

Energy relations in non adiabatic 5TSRAM are as follows.

Energy during read time

$$= \int f\,change \times (Cbl + Cdl + Cin) \times Vdd^2 dt \quad (3)$$

Energy during write time

$$= \int fchange \times (Cbl + Cdl) \times Vdd^2 dt \quad (4)$$

Where fchange is the frequency of change in the bit line voltage. Cbl, Cdl, Cin are the capacitances of a bit line, Data line and the input capacitance of the read amplifier.

The energy relations in adiabatic 5T SRAM are as follows.

$$\text{Energy during read time} = \int fchange \times (Cbl + Cdl + Cin) \times Vpc^2 dt \quad (5)$$

$$\text{Energy during write time} = \int fchange \times (Cbl + Cwrite + Cdl) \times Vpc^2 dt \quad (6)$$

Where fchange is frequency of change in the bit line voltage. Cbl, Cdl, Cin are capacitances of a bit line, data line and input capacitance of the read amplifier. Vpc is time varying power clock voltage.

$$\text{Energy during hold time is} = \int I\,leak \times Vdd \quad (7)$$

$$Ileak = Isubthreshold + Igateleak \quad (8)$$

Where I leak is total leakage current, I sub threshold is sub threshold leakage current and I gate leak is gate leakage current.

I leak is reduced in adiabatic 6T SRAM by a small amount of current which flows into the write driver circuit. Hence the leakage of energy is reduced during hold period.

4.2 Read delay

The read delay is defined as time delay between 50% level change in the word line signal to 50% level change in the output of the sense amplifier. Generally the differential type of sense amplifier results in less delay compared to single ended buffer. However the delay in the single ended buffer is improved by choosing inverters with sizes in the increasing order. The comparison of read delays is shown in the Fig. 4. The read delay is found to be reduced by more than half times in case of adiabatic SRAM.

4.3 Write delay

The write delay is the difference in time between 50% level change in the word line signal and the 90% level of the storage node. As it is seen in the Fig. 5, the write delay is found to be increased in the Adiabatic SRAM when compared to the non adiabatic SRAM due to increased resistance of the write driver circuit. The rise is 10 times in case of adiabatic SRAM with single ended reading amplifier at 25^{o}C.

4.4 Static noise margin

The static noise margin is defined as the maximum noise that can be tolerated at the input of the SRAM without changing its status [16]. It is given by the size of the smallest square that can be inscribed in the butter fly curve of the SRAM. The SNM of both SRAMs is found to be 0.357V. Fig.6 shows the similarity of SNM of both SRAMs.

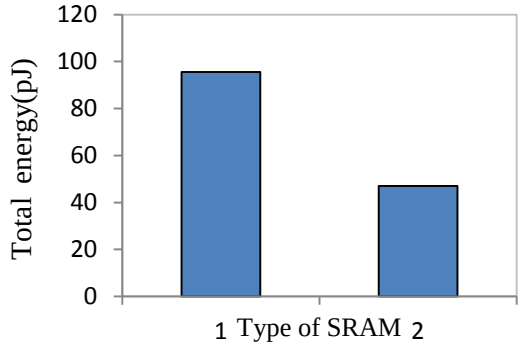

Figure 4. Total energy (pJ) of SRAM cell for both the types of SRAM cells

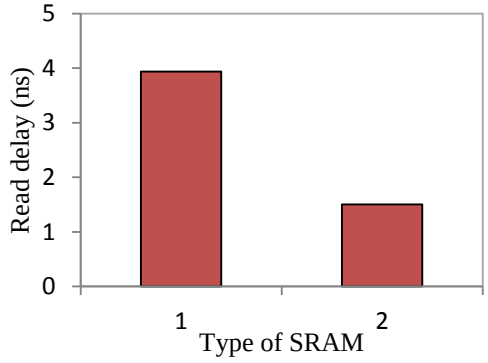

Figure 5. Read delay(ns) of SRAM for both the types of SRAM cells

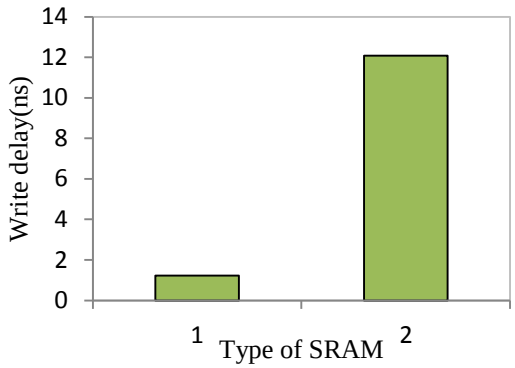

Figure 6. Write delay (ns) of SRAM for both the types of SRAMs

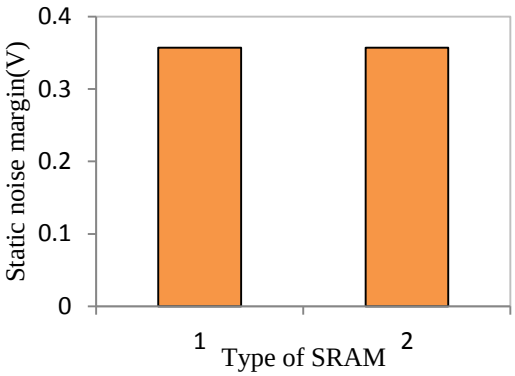

Figure 7. Static noise margin of SRAM for both the types of SRAMs

4.5 Write margin

Write margin is found as the maximum bit line voltage at which the write operation is obtained when the bit line voltage is changed from VDD to 0V. It is found to be same for both SRAMs and is equal to 0.769V for '0' to '1' change and 0.822V for '1' to '0' change. The similarity is shown in the Fig. 7. The storage node voltages during writing is shown in Fig. 8.

5. CONCLUSION

With an intension of arriving at a stable and energy efficient SRAM, effort has been put to design an asymmetrical 6T SRAM cell with one bit line for read and one bit line for write along with dual word lines. A simple energy recovery driver along with a larger access transistor connected to the write bit line helps in enhancing the write ability, in addition to saving energy during writing. Read stability has been improved by sizing the pull down transistor connected to the single ended read amplifier. Read delay has been found to reduce in adiabatic SRAM. Although write delay is greater when compared to non adiabatic similar SRAM the power delay product has improved by 22%.

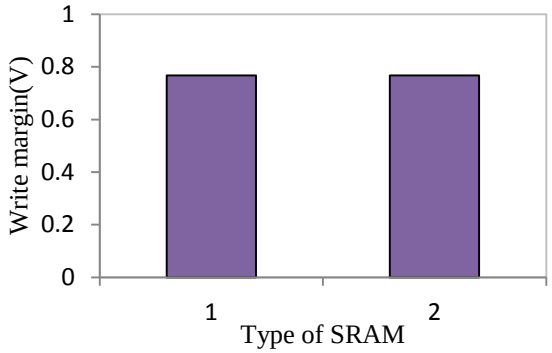

Figure 8. Write margin (V) of SRAM for both types of SRAMs

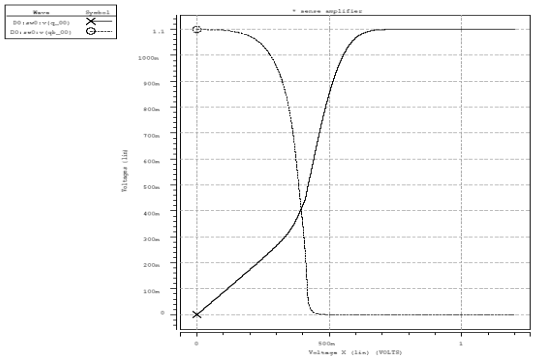

Figure 9. Storage node voltages of SRAM during writing

6. ACKNOWLEDGMENTS

My thanks to the Prof. Satyam Mandavalli for his guidance.

7. REFERENCES

[1] L. Villa, M. Zhang, and K. Asanovic.2000. of International Symposium on Microarchitecture, Dynamic zero compression for cache energy reduction, proceedings 2000, pp. 214–220.

[2] B. Yang and L. Kim. 2005. A low-power SRAM using hierarchical bit line and local sense amplifiers IEEE J. Solid-State Circuits, vol. 40, no. 6, Jun. 2005, pp. 1366–1376

[3] D. Somasekhar, Yibin Ye, Kaushik Roy, "An Energy Recovery Static RAM Memory Core, In Proc. 1995 Symposium on Low Power Electronics", San Jose, CA, October 9-1, 1995

[4] N. Tzartzanis and W.C. Athas, "Energy recovery for the design of high-speed, low power static RAMs," In Proc. IEEE International Symposium on Low Power Electronics and Design pp. 55–60, 1996

[5] Joohee Kim, Conrad H. Ziesler, Marios C. Papaefthymiou "Energy Recovering Static Memory" In Proc. ISLPED'02, Monterey, California, USA, August 12–14, 2002

[6] J.Kim,M.C Papaefthymiou, In Proc. "Constant –Load Energy Recovery Memory For Low Power, International Symposium on Low power Electronics and Design,pp.240-243. 2004

[7] J. *Kim*, C.H.Ziesler, " *Fixed-Load* Energy Recovery Memory for Low Power", In Proc.International Symposium on Very Large Scale Integration. Systems, pp. 145. 6.,2004

[8] Shunji Nakata in "Recent Patents on Electrical Engineering,2009,Vol.2,No.1

[9] Keejong Kim, Hamid Mahmoodi and Kaushik Roy "A Low Power SRAM Using Bit- Line Charge-Recycling" IEEE Journal of Solid State Circuits, vol.43, no.2, pp. 446-458, 2008

[10] Byung-Do Yang "A Low Power SRAM Using Bit- Line Charge –Recycling for Read and Write Operations in IEEE Journal of Solid-State Circuits, Vol.45, No. 10, October 2010

[11] Jun-Jun Yu,Peng-Jun Wang "Design of Adiabatic SRAM Based on CTGAL Circuit". In Proc. The 8th International Conference on Solid –State and Integrated-Circuit Technology, October 23-26, 2006

[12] Hao-I Yang,Ssu-Yun Lai,and Wei Hwang "Low-Power Floating Bit line 8-T SRAM Design with Write Assistant Circuits" In Proc. IEEE International SOC Conference, October, 2008

[13] Shunji Nakata,Hirotsugu Suzuki,Ryota Honda,Takahito Kusumoto,Shinjchiro Mutoh, Hiroshi Makino, Masayuki Makino, Masayuki Miyama and Yoshio Matsuda " Adiabatic SRAM with a shared Access Port using a Controlled Ground Line and Step-Voltage Circuit" In Proc. IEEE International Symposium on Circuits and Systems, ISCAS 2010, pp.2474-2477, 2010.

[14] Nalam, S,Chandra, V.Pietrzyk, C. Aitken, R.C.Calhoun, B.H. 2010.Asymmetric 6T SRAM with two-phase write and split bitline differential sensing for low voltage operation. Proceeding of 11TH International symposium on Quality electronic design 2010 pp.139-146

[15] Keunwoo, K.Jae-Joon.K and Ching –Te, Asymmetrical SRAM cells with enhanced read and write margins'. International. Symposium VLSI Technology, Systems and Applications, 2007, (VLSI-TSA 2007), Hinchey, Taiwan,2007

[16] E.Seevinck,F.J.List and J.Lohstroh.1987 Static-noise margin analysis of MOS SRAM cells. IEEE Journal of Solid-State Circuits, vol. 22, 1987 pp. 748-754

[17] PTM models derived from http://ptm.asu.edu/