Analysis and Testing of VME (Versa Modular European) Bus Cards

Sk. Fahiya[1], V. Vittal Reddy[2] N. Nageswara Rao[3],

[1]Student,
[1]Gudlavalleru Engineering College,
[1]Gudlavalleru, Krishna District, Andhra Pradesh, India.

[2]Assistant Professor
[2]Gudlavalleru Engineering College
[2]Gudlavalleru, Krishna District, Andhra Pradesh, India.

[3]Addl. general manager,
[3]CAD department,
[3]Electronic corporation of India limited (E.C.I.L), India.

Abstract
Abstract: To provide high Reliability, safety and security in PFBR (prototype fast breeder reactor) & also to detect the problems immediately in order to initiate safety actions in fast reactors, VME bus usage in Real Time computers becomes inevitable. In this paper, we do analysis and testing of VME bus cards.

Keywords
VME bus, PFBR, Analog I/O cards, Digital I/O cards.

1. INTRODUCTION
In PFBR Fast reactors have a higher power density in order of 500kw/liter in the reactor core and some of the liquid metal coolant flows through the fuel subassemblies to remove the heat efficiently. By mistakenly Plugging in any one of the fuel assembly can lead to clad hotspot and all the fuels get meltdown. To identify this type of problems immediately in order to take safety actions & also to monitor the o/p temperature of all fuel Subassemblies, mean temperature gradient across core and comparison of actual temperature rise with expected temperature rise for every subassembly & for many derived parameters the usage of VME bus in safety critical system becomes inevitable in PFBR. This type of real time computer based VME bus was designed by the JACK KISTER he is a European engineer.

This VME bus consists of Motorola 68020 processor card, Analog I/O cards ,Digital I/O cards each card has its own functionality. All the cards are get controlled by the motorola68020 processor card. **Analog Input card** was designed to acquire the core inlet & outlet temperature signals. **Digital Input Card** was designed is to check whatever the signals coming from the field are correctly passing or not and also for online testability, status display. **Analog Output Card** was designed to display the total mean temperature of reactor core, which is calculated by the RTC. **Digital Output Card** was designed to display alarm and also SCRAM (shutdown by control rod accelerated movement)signal to shutdown system. The (fig.1) shows the structure of VME bus.

fig.1: VME bus in real time computers

fig.2: internal structure of VME bus.

2. SYSTEM DESIGN MODEL
2.1 VME BASED SYSTEM

CTM(core temperature monitoring) being a safety critical system, RTCs need to be designed to comply with the guidelines specified in AERB Safety Guides D-10 & D-25. It is decided to have Real Time Computer (RTC) system as a **VME based system** since VME bus has longer track record in the market. This system consists of CPU and Analog Input modules, Digital Input modules and Analog Output modules. The Analog Input modules are designed to acquire both the core outlet and the inlet temperature signals. The digital output module is used for display of alarm and also is used to issue

trip signal, which has to be further processed by the 2/3 voting logic in order to issue SCRAM signal to shutdown system. Analog output module is used to display the Mean temperature of reactor core, which is calculated by RTC.

2.2VME BUS BASED ANALOG INPUT CARD

The K-type thermocouple signals from reactor core are signal conditioned and converted to 4-20mA signals and again 4-20mA current signals are converted into 1 to 5V signals by passing these current signals through standard resistors. Hence the Analog Input modules that are part of RTC are designed to accept the 1 to 5V signals and the RTC is used to acquire the temperature signals both from core outlet and core inlets with an accuracy of 0.05% of full scale. RTC should scan all 420 channels (two T/Cs from each of 210 Fuel Sub Assemblies), store the data and transmit the data to the Distributed Digital Control System (DDCS) within 1s. The operational status of the Analog Input module should be available on both the fascia panel through LED display and through addressable registers.

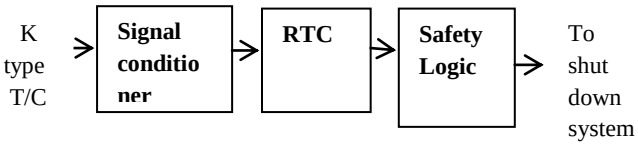


Fig3: signal flow diagram

After receiving the 5V signal it passes inside the analog input card block. The block diagram of analog input card is as shown in fig4. The Analog input Module consists of two level multiplexer, Instrumentation amplifier, low pass filter, analog to digital converter and dual ported memory.

Multiplexer: Multiplexers are the front end devices for this analog input module. They are employed to connect one channel at any point of time to the system out of all the channels. CMOS Multiplexers are used for handling high level signals and also used for fast scanning in contrast with relays which are used for slow scanning. The signals which are coming from field can be connected either as single ended signals or as a differential signals. In single ended multiplexer each signal is ground referenced. The signal referenced to each other is called differential mode signals. By connecting the signal in differential mode, the common mode error in the channel is eliminated considerably. The RTC should scan all 420 channels and transmit the scanned data to the Distributed Digital Control System (DDCS) within 1s, the requirement of scan time for 420 channels is 400ms, after allowing 60% of the time for transmission of data to DDCS. This is approximately 1ms for each sample. For this sampling rate, CMOS Multiplexers are the best choice.

For the implementation of first level multiplexing, ADG406 (Analog Devices) CMOS IC has been identified. This chip is a 16:1 single ended multiplexer. For the implementation of second level multiplexing, ADG409 (Analog Devices) CMOS IC is selected as it meets the requirements. This chip is the 4:1 differential multiplexer. The salient features of these chips are

- Low On-resistance (80 Ohms)
- Fast switching
- Break before switching action
- +15V to –15V input range
- Low power dissipation
- Low leakage current (1nA at V_{DD} =16.5V and V_{SS} = -16.5V)
- Low charge injection
- Low output capacitance (order of 5pf)

Instrumentation Amplifier: The Amplification stage is implemented using the INA114 Instrumentation Amplifier IC. The salient features of this IC are as follows,

- Input impedance of the two inputs = 10^9 Ohms
- CMRR = 115dB
- Input bias current = 2nA
- Settling time = 20μs (0.01%)
- Low offset voltage = 50μV
- Low Drift = 0.25 Vμ/^{o}C
- Gain = 2 for input range (1-5V)
  = 1 for input ranges (0-10V or ±10V)

Low pass filter (LPF): Second order Butter worth Low pass filter is optional block in the analog input module. This filter can be used to suppress the high frequencies components that exist in the output of the Instrumentation amplifier. the scanning time of each of the channels may vary due to the response time of the filter.

Analog to Digital Conversion (ADC): Successive approximation type of ADC is used in this circuit AD976 16bit ADC (Analog Device) is chosen for the Analog input module. The salient features of this IC are

- 16bit Successive Approximation ADC with switched capacitor network
- 200Ksample throughput
- Input range ± 10V

Sequencer: To reduce the load on CPU, a on-board FPGA based Sequencer is proposed. This sequencer is designed to scan all the channels on demand and to store the scanned data in memory. The stored data can be sent to CPU system. During scanning status like busy, healthiness of the ADC, memory clear, scan over, scan incomplete and heartbeat count can be read by CPU. After scanning the stored data and range check status are available to be read by CPU

S/W or H/W Triggering: it Supports software trigger (i.e. Receive command from CPU) Supports Hardware trigger (i.e. On board excitation) Until Sequencer completes the present scan, intermediate triggers are not considered.

Memory: Dual ported RAM is used. In this one external device can write and other device can read synchronously. For each channel, the data is stored in a fixed memory location. Before writing the current scanned data into the memory during each scan into the memory, the previous data will be erased and all the location will be filled with zeros. The CPU read the scanned value from memory. Sequencer writes the 16bit data from ADC into the location allotted for that channel in SRAM after the end of conversion. While writing,

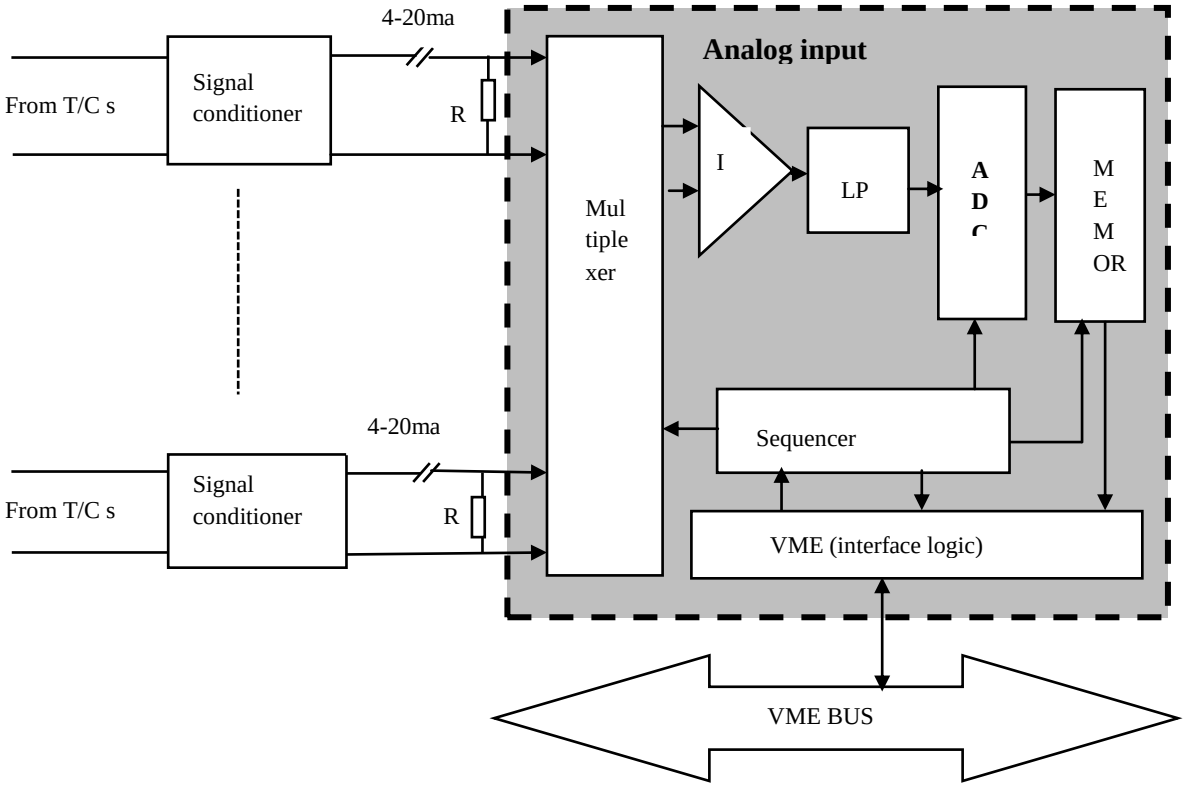


Fig4: block diagram of analog input card

Sequencer will force the signal seq_mem_sel to low and continued to be in low state till all the channels are scanned and stored into the memory. While writing into the memory location, sequencer uses 6 address lines to address one of the 48 locations. This arbitration logic prevents any CPU's read or writes operation while sequencer writing. By default, this logic allows sequencer to write into the memory.

VME Bus interface logic: The interface board is mapped to a single address in the 16-bit address range of the VME bus, and reads commands written to that address by the host processor on the VME bus. VME bus interfacing using Cypress make CY7C960 Slave VME interface chip (SVIC) along with CY7C964s

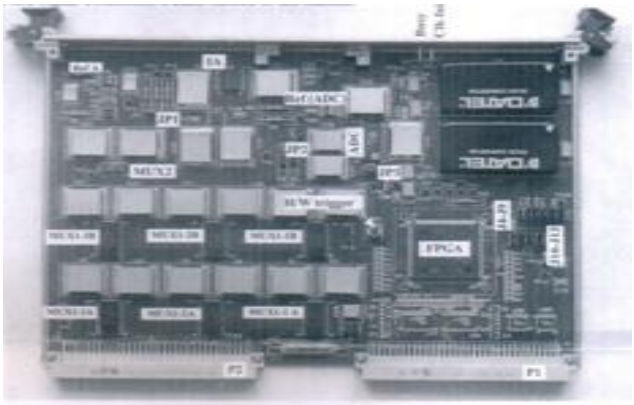


Fig5: VME bus based analog input card

2.3VME BUS BASED DIGITAL INPUT CARD

The digital input block was mainly designed to test the signals Coming from the field are perfect or not. The block diagram of VME bus based 30-channel Digital Input card is shown in Fig.6. Each block has its own functionality. It consists of Two EPLD's named Bus Controller EPLD, Debounce and Force EPLD.

Bus Controller EPLD: EPM7256SRI208-10 type of IC is used it is the family of embedded CPLD with max7000 series it contains 256 macrocells**. The** Bus Controller EPLD block contain Board Select Logic block, Control Logic & DTACK Logic block, The Debounce Clock, Control and Status Register, Change of State Logic block, Interrupter logic, Diagnostics Register block all these blocks are controlled by bus controlled EPLD.

Board Select Logic block: it compares the board's address (set by means of jumpers) to the address on the VME bus address lines and generates a board select signal /BRDSEL when an address match is obtained.

Control Logic & DTACK Logic block: after completion of board selection the control logic block generates the necessary internal read and write signals using this /BRDSEL signal and also gives data transfer acknowledge signal is generated to enable the completion of the current on-going bus cycle.

The Debounce Clock block: the debounce clock divides the system clock of 16 MHz to have 40Hz, 400Hz, 4KHZ and 40 KHz, which is used as a source clock by the Debounce logic block. **Control and Status Register block:** it check the status of all inputs, status of board fail block, and also debounce time

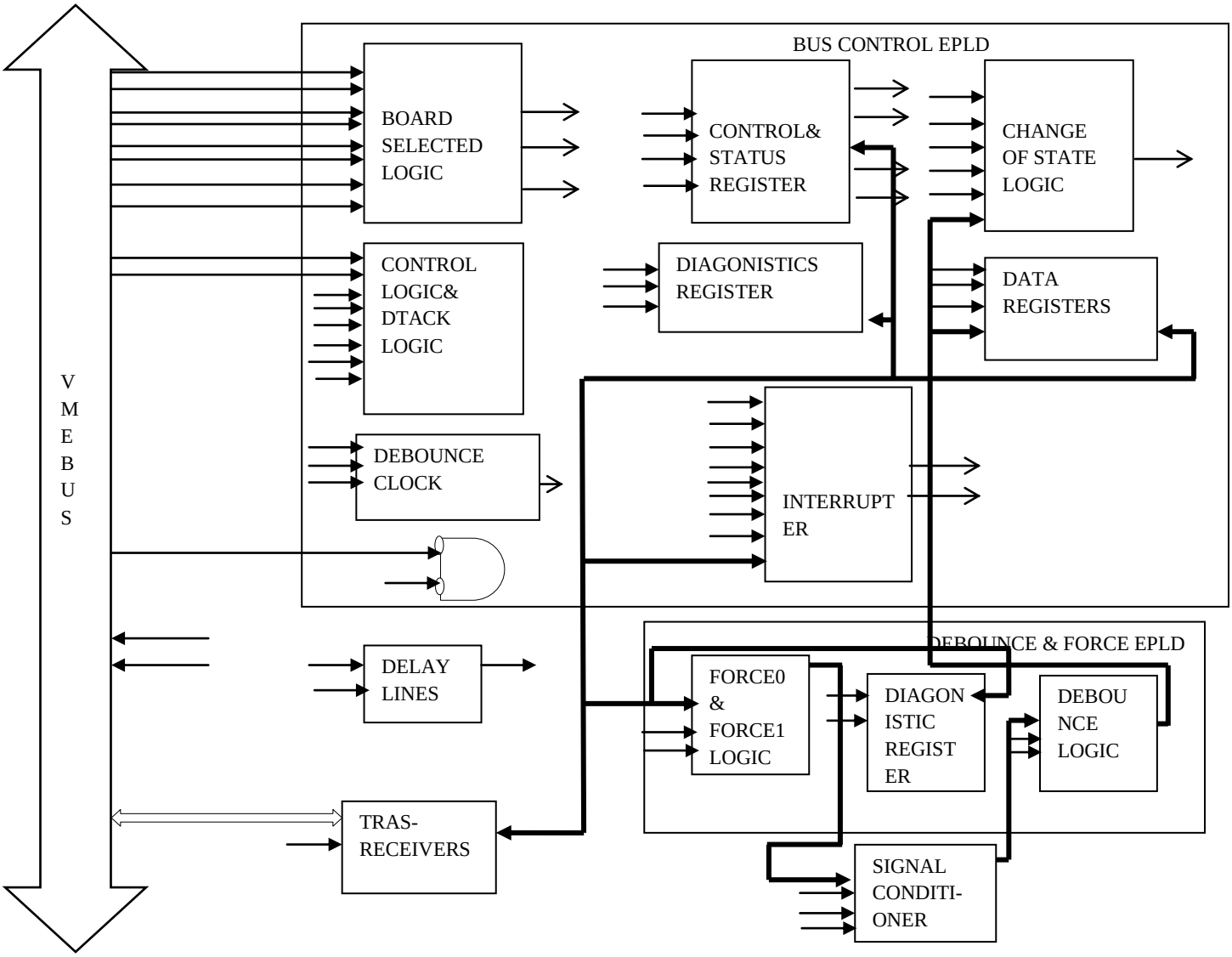


Fig 6: block diagram of digital input card

selection. **Change of State Logic** block: if any one of the input changes its state generate output (COSOUT). **Interrupter logic block:** it places the vector address during interrupt acknowledge cycle and also generates INTA and IACKOUT signal.

The debounce and Force EPLD block: it contains Force'0' and Force'1" logic, Debounce logic and a diagnostic register.

Debounce logic block: for the received signals it performs the debounce logic to eliminate the bounces in the input signal. The default debounce time is 10ms.

Force'1' registers block: it is a two sixteen bit registers to force the input to '1' state. All the input should be in '0' state during force'1' test all the inputs changes its state to '1'.

Force'0' registers: it is a two sixteen bit registers to force the input to 0' state. All the input should be in '1' state during force'0' test all the inputs changes its state to '0'.

Diagnostic registers: to check the health status of force'0' and force'1' test it is used and it also read back the signal to processor.

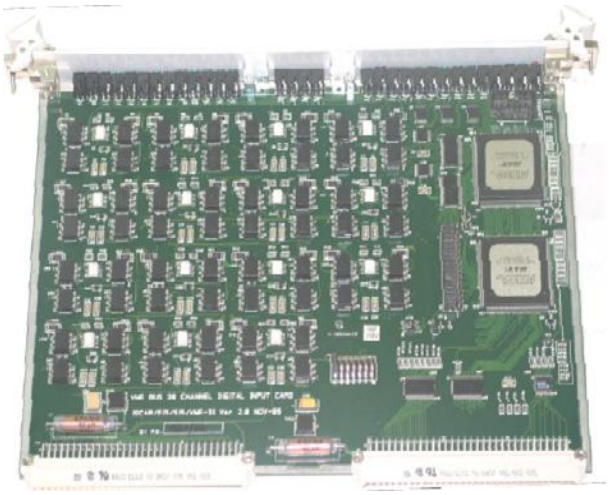


Fig7: VME bus based digital input card

2.4 VME BUS BASED ANALOG OUTPUT CARD

The analog output card is designed to display the total mean temperature of reactor core. The block is as shown in fig9.

Bus buffers / Transceivers: the 74FCT16244 chip of bus buffer and 74FCT245 chip of transceivers are used to interface with VME bus to buffer the Address bus and control signals from VME bus.

Bus Interface / Control CPLD: to interface with the VME **Bus** Interface / Control CPLD is used.

it provide control signals to the DAC for writing or reading back digital Inputs, resetting the outputs, etc.

• It provides control signals to the analog MUX and ADC to implement the conversion of analog data back to digital.

• It provides diagnostic registers for the testing of the bus interface.

• It detects clock failure

DAC: For starting any conversion, the processor must write the 12-bit data into the corresponding DAC register. The data written into the DAC can also be read back by the CPU from the same address. For performing any operation on the DAC, the CPLD must drive the Data lines of the DAC. It also has to drive the address lines that indicate which one of the 4 DACs has been selected for updating. This section has four 12-bit Digital to Analog Converters. The chip used is the Analog Devices AD664. It has four complete 12-bit voltage-output DACs in one monolithic IC chip. It uses an external 10 V reference voltage source.

Isolation: Four voltage-to-current converter isolation chips are used for obtaining current output. The chip used is the Analog Devices. It can take an input of 0 to+10V and can be connected to give an output of 4-20 mA or 0-20 mA. The current range selection is through jumper settings.

Read-back Section (Isolation, Analog MUX, Amplifier and ADC): This section consists of four isolators, an analog MUX, an amplifier and an ADC for conversion of the analog output back to digital, for diagnostic purposes.

Isolation: for the received current loop path, a 100 Ω resistor is provided onboard in the current loop for converting the current to voltage for read-back. The voltage across these four resistors are isolated and fed to an analog MUX.

Multiplexer: The analog multiplexer used It has eight input channels. It switches one out of eight inputs to a common output as determined its 3-bit binary address lines. Other than the four analog output channels, a temperature signal from the reference IC is also connected to one input of the MUX. The other inputs are grounded. Since the input signal is unipolar (0-10V), the device can be operated from a single rail power supply of +15V.

Amplifier: The op-amp chip OP177 is used for the amplification stage prior to the ADC.

ADC: The ADC used is the Analog Devices AD1674. It is a complete 12-bit analog-to-digital converter consisting of a user-transparent onboard sample-and-hold amplifier, 10V reference, clock and three-state output buffers for microprocessor interface. The device is used in stand-alone mode.

Fig8: VME bus based analog output card

2.5 VME BUS BASED DIGITAL OUTPUT CARD

The digital output card is used to display alarm and also is used to issue trip signal, which has to be further processed by the 2/3 voting logic in order to issue SCRAM signal to shutdown system. The block diagram for VME bus based 15-channel Relay output card is shown in Fig. 10.

Transceivers & Transceiver Enable Logic block: it contain drivers which interface with VME bus data lines. Its functionality is to Trans and receives the signal from board to VME bus. **The Board Select Logic & DTACK Generator block: it** compares the board's address (set by means of jumpers) to the address on the VME bus address lines and generates a board select signal /BRDSEL when an address match is obtained.

Control Logic block: it generates the necessary internal read and write signals using this/BRDSEL signal. Further data transfer acknowledge signal is generated to enable the

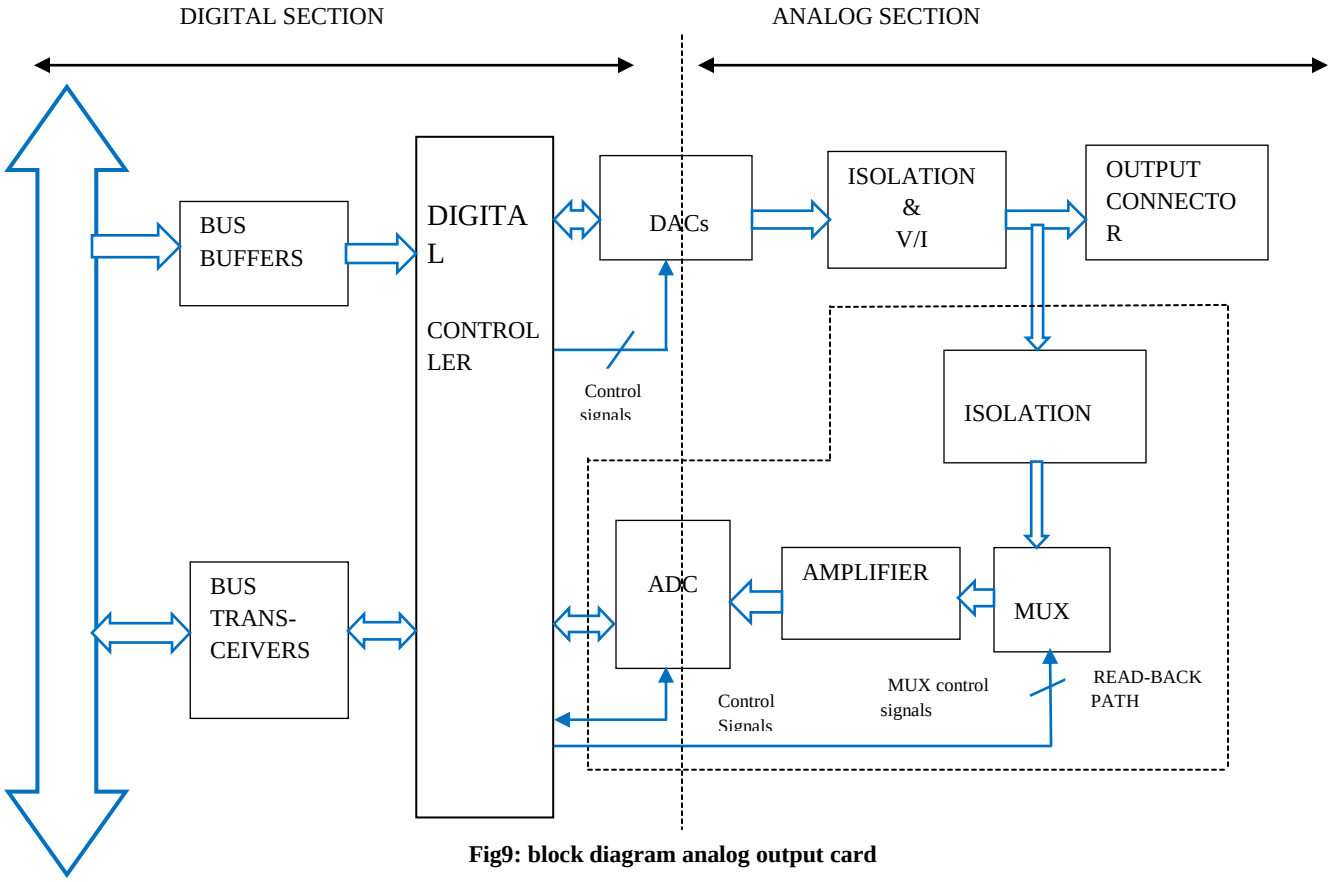


Fig9: block diagram analog output card

completion of the current on-going bus cycle. **Latch block:** latch is a data storage element.it is used to latch the data onthe VME bus data lines and it feeds the Inverters block.Whenever watchdog generates timeout due to CPU failure or when system clock fails all the outputs are instantaneously cleared.

Latch block: latch is a data storage element.it is used to latch the data onthe VME bus data lines and it feeds the Inverters block.Whenever watchdog generates timeout due to CPU failure or when system clock fails all the outputs are instantaneously cleared.

Inverters block : inverter block drives the **Relays, Drivers and Status LED's** block. it contains fifteen inverter gates, which inverts the outputs of the **LATCH** block.

The Clock Divider block: it divides the system clock of 16 MHz to 1000 Hz, is used as a source clock by the **Watchdog Timer.** It also uses counters to divide system clock to get 1 ms pulse, whichis used as a clock to run the watch dog timer circuit. The above logic is implementedusing 7493 and 7490 counters**.**

The Control and Status Register block: it generates signals to enable the watchdog timer for operation and facilitates generation of board fail signal incase of any mismatch between relay contact outputs versus latched data through software.It also reads back the status bit such as Watchdog Timer enable and Timeout.

Watchdog timer, countpatten registers:

The watchdog timer is designed using counters. Load value is set throughsoftware by loading bit patterns into count pattern registers to set the timeout value between 1milliseconds to 65.536 seconds. The counters are loaded with this value periodically by the CPU. Failure of CPU card or software causes the counter to decrement from the load value until it reaches zero and then generate a **time out** signal.This output can be reset by manual reset or through software. Provision has been madeto read back watchdog timer counter on the fly through software to check its healthiness.

Diagonistic register and readback: To check the healthiness of transceivers, board select logic and data bus, a pair of diagnostics register is provided. Data patterns can be latched on to the diagnosticregister and subsequently latched data can be read back on data lines.The above logic is implemented using 74273 latch and 74244 buffers.

Clock fail detection: The clock fail detection circuitry is designed to detect failure of the system clock.

Relays,drivers and status LEDs: which drive the relay coils and indication LEDs. The LEDs are connected in parallel to the relay coils, toensure that failure of LED does not affect the relay operation.On power on- reset, the relays will be in de-energizedcondition. relay operation.On power on- reset, the relays will be in de-energizedcondition.

Connectors: The VME signals are connected to P1 connector and relay contact outputs are terminated in P2 connector. Transient suppressor devices have beenadded on +5V and +24V power line on the card for protection against surges. The no. ofchannels is reduced from 16 (in Ver1.0) to 15 (in Ver 2.0). Further the 24V relay coilvoltage is introduced on the P2

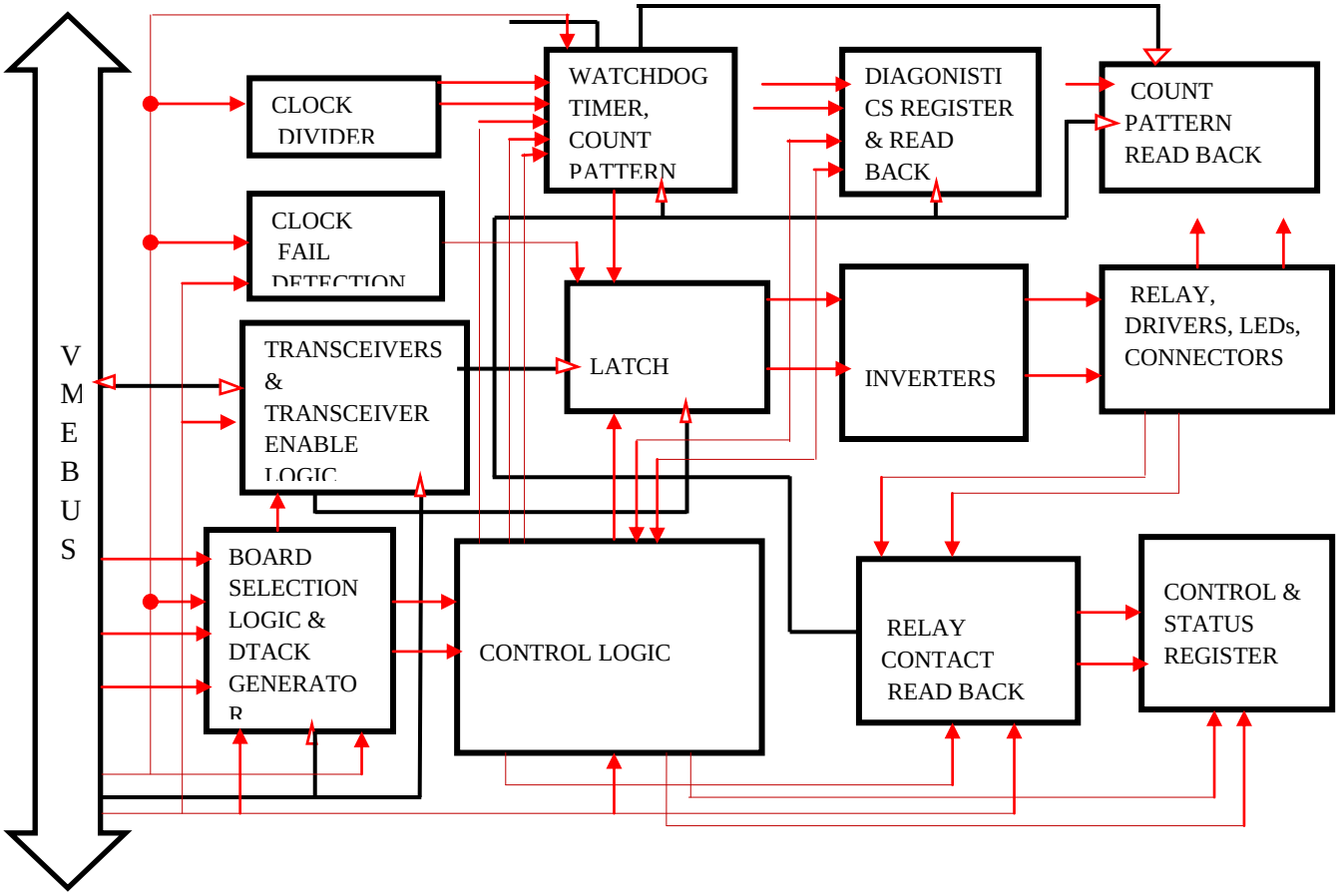


Fig10: block diagram of digital output card

connector.

Count Pattern Read Back block: it reads watchdog count register on data bus lines. The Board select Logic and DTACK Generator block, Control logic block, Latch block, Relay contact read back block, Controland Status register block, Transceiver enable logic block, Clock Divider block, WatchdogTimer and Count pattern register block, Diagnostics read/write register block, Countpattern read back block, Clock Fail Detection block and Inverters block has been implemented in CPLD.

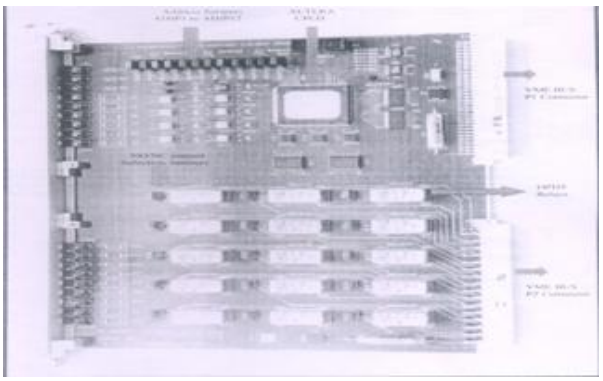


Fig11: VME bus based digital output card

3. SIMULATION AND EXPERIMENTAL RESULTS

3.1 TESTING PROCEDURE OF VME BUS CARDS:

Test setup hardware: all designed analog I/O and digital I/O cards are tested using these hardware components.

- CPU-ED20 as standard board.
- 19’’standard bin with VME20 slot P1 motherboard
- 5V and 24V of power supplies.
- VME based analog I/O and digital I/O cards.
- One RS 232 cable assembly.
- Pentium-IV pc windows2000/ XP.
- One 96 pin flat cable for P1 connector which interfaces the analog I/O and digital I/O cards with VME bus.64 flat ribbon cable for P2 connector which connects all the I/O’s of analog and digital cards.

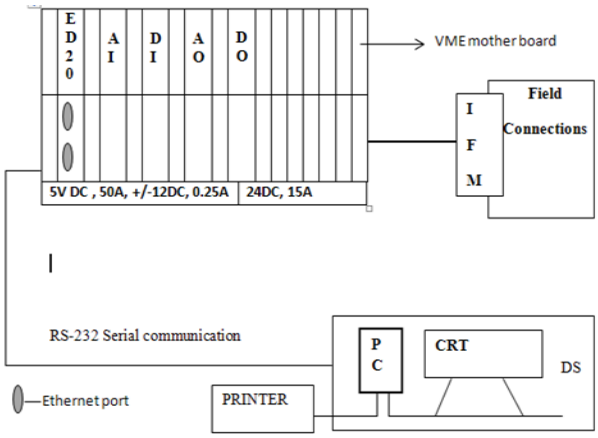
Connectivity

- VME based analog IO and digital IO boards are tested along with CPU-ED20 system.
- One serial RS232 cable is connected between COM1/COM2 port of PC and P2 connector of CPU-ED20 board.
- One of the 96- pin and 64-pin flat cables should be connected to interface module which placed at back side of connector.
- 5Vpower supplier for P1 connector, 24V power supplier for P2 connector.

Test software for PC

Terminal.EXE the test software for PC (hyper terminal) is used to communicate with ED-20 card through RS232. The monitor uses serial port COM1/COM2 for communicating with host PC and operated in 38400-N-8-1 mode with flow control enabled.

Block diagram of testing process



3.2 EXPERIMENTAL RESULTS

For troubleshooting purpose these VME bus cards was used. If there is no failure while testing the cards, the LED's in the front panel of cards will glow.

4. CONCLUSION

In the nuclear reactors if any problem occurs it becomes very difficult to identify and takes more time to repair. In This paper we presented an analysis and testing of VME (versa modular European) bus using this VME bus we can provide safety & security and can also detect the problems immediately in order to take safety actions. using this VME bus overall system design should have high mean time between failures and low mean time to repair.

5. ACKNOWLEDGEMENT

I would like to thank our HOD - Dr. M. Kamaraju, v.vittal reddy -assistant professor, ECE department. I also express my grateful thanks to principal-Dr.P.Nageswar Rao; Gudlavalleru engineering college. I would also thank N.nageswara rao, project manager, E.C.I.L.

6. REFERENCES

[1] Design Specification for Core Temperature Monitoring System (Ref –PFBR/63110/SP/1003)

[2] [1].John A Stankovic "Real Time Computing", University of Massachusett, April 16 1992

[3] Conceptual Design of Core Temperature Monitoring system (Ref. – PFBR/63110/DN/1000)

[4] Cypress - VME bus interfacing Handbook.

[5] B. Ramaswamy Pillai, G. Venkat Kishore, M.A. Sanjith, S. Chandrasekaran and S. Ilango Sambasivan,"core temperature monitoring system" Report No.PFBR/66120/DN/1002

[6] G. Venkat Kishore, N. Sridhar, B. Krishnakumar, S. Chandrasekaran and S. Ilango Sambasivan,"real time computers in PFBR" Report No.PFBR/66120/DN/1000M.

[7] N. Sridhar, J. Selva Solomon, V. Mythili, D. Thirugnanamurthy, B. Krishnakumar and S. Ilango Sambasivan,"core temperature monitoring in nuclear power plant" ReportNo. PFBR/66120/DN/

[8] http://www. Real time computers for instrumentation and control of PFBR.

[9] http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/VMEbus/index.html

[10] VME bus market overview – http://www.vita.com.