High Performance and Function Design on the Transistor Level

Tripti Sharma & K. G. Sharma
Department of ECE
FET-MITS (Deemed University)
Lakshmangarh, Rajasthan, INDIA

ABSTRACT
This paper proposes a new design of pass transistor logic based 2T AND gate. Performance comparison of proposed gate with traditional CMOS, complementary pass-transistor logic design and GDI techniques is presented. Different methods have been compared with respect to the number of devices, power-delay product, temperature sustainability and noise immunity in order to prove the superiority of proposed design over existing ones. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm technology.

Keywords
AND gate, PTL and Power-delay product.

1. INTRODUCTION
With rapid development of portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggered numerous research efforts [1]–[3].Last two decades has seen development of many logic design techniques to improve the performance of logic circuits based on traditional CMOS technology. One form of logic that is popular in low-power digital circuits is pass-transistor logic (PTL). Many PTL circuit implementations have been proposed in the literature [1]-[2], [4]-[8]. Some of the main advantages of PTL over standard CMOS design are 1) high speed, due to the small node capacitances; 2) low power dissipation, as a result of the reduced number of transistors; and 3) lower interconnection effects due to a small area.

However, most of the PTL implementations have two basic problems also. First, the threshold drop across the single-channel pass transistors results in the reduced current drive and hence slower operation at reduced supply voltages. This aspect is particularly important for low-power design since it is desirable to operate at the lowest possible voltage level. The second, since the "high" input voltage level at the regenerative inverters is not, the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant [4].

This paper proposes a new design of AND function using two transistors which shows the better performance in terms of power consumption, power-delay product and it is also area efficient as compared to traditional CMOS and CPL AND

functions. Existing AND gate designs using CMOS, CPL and GDI techniques are briefly described in Section II. Proposed AND cell is discussed in Section III. Results of quantitative comparisons based on simulations of AND gates using different logic techniques with proposed cell are shown in Section IV and conclusions are finally drawn in Section V.

2. PREVIOUS WORK
Fig.1 [1], [2] and [8] shows the design of two input AND gate based on CMOS technology. It consists of six transistors (6T). The advantage of this gate is that it gives full output swing i.e.; no threshold loss but on the other side it has many shortcomings such as more area because of six transistors required to design a gate, large power consumption and less speed. For every input combination it produces the delay of 3T.

Design of AND gate based on CPL technique [1]-[2], [4]-[8] is shown in Fig.2. This design consists of four transistors (4T). This circuit shows better performance than CMOS AND gate in terms of area, power consumption and speed but it shows threshold loss when both the inputs are at logic high.

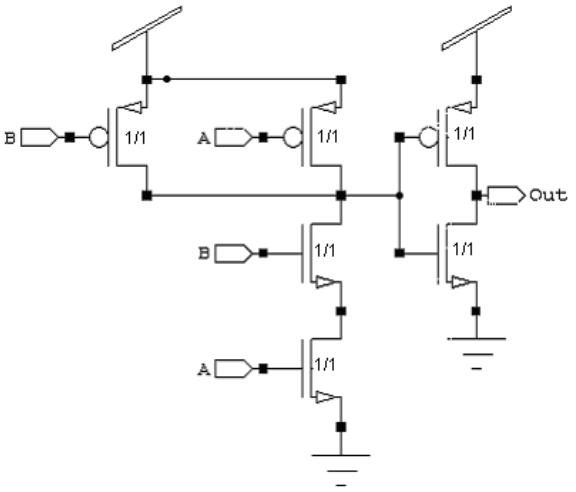

Fig 1: 2-i/p 6T AND gate

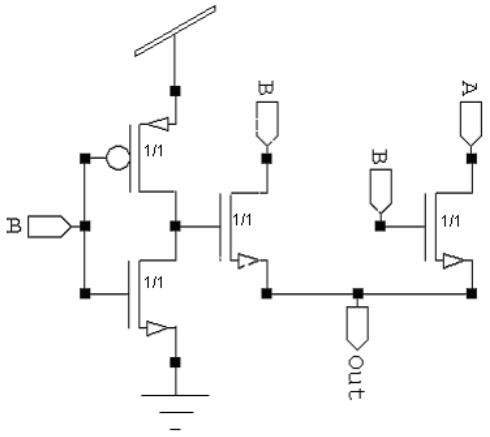

Fig 2: 2-i/p CPL AND gate

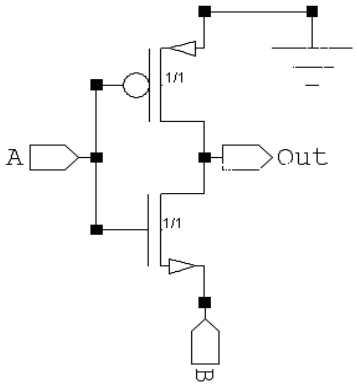

Fig 3: GDI AND gate

Another design of two input AND function is shown in Fig.3 [9]-[12]. It is based on GDI technique. Area wise it is the most efficient and fastest AND cell reported in the literature as it uses only two transistors. It also consumes least power but on the darker side it has nearly 10% more threshold loss than CPL AND gate.

3. PROPOSED PTL BASED 2T AND GATE DESIGN

Some of the main advantages of Pass Transistor Logic (PTL) over standard are high speed due to the small node capacitances, low power dissipation as a result of the reduced number of transistor and lower interconnection effects due to small area[1]-[4] and [7].

PTL are single FETs that pass the signal between the drain and source terminal instead of a fixed power supply value. They required less area and wiring but cannot pass the entire voltage range. NFETs are preferred for this application, since the larger electron mobility implies faster switching than could be obtained with PFETs of the same size. The proposed design is based on the model, where a set of control signals is applied to the gates of NMOS transistors.

The proposed PTL AND gate shown in Fig.4 consists of two NMOS transistors connected in series. The two inputs A and B are connected to the gate of NMOS pass transistors M2 and M1 respectively. Instead of connecting ground and supply voltages to source/drain of transistors inputs A and B are used.

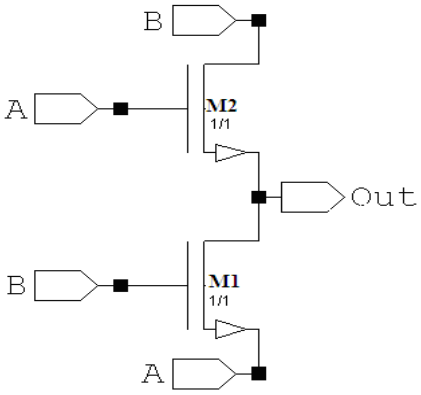

Fig4: Proposed PTL AND Gate

When AB=00, then both transistors will be OFF and output terminal will show some error voltage which is as low as logic '0'. But when AB=01, M1 is ON and M2 is OFF and as NMOS is strong '0' it will pass logic low signal without any degradation at the output. Similarly, for AB=10, M2 is ON and M1 is OFF and as NMOS is strong '0' it will pass complete logic low signal to the output and for AB=11, then M1 and M2 are ON and as NMOS is a weak '1' device it will pass high signal at the output having threshold loss. But on the other side M1 and M2 both are connected in parallel and their equivalent resistance will result into increased transconductance which will lead to an increased output voltage. Hence, as a result very less degradation in the voltage will be shown at the output terminal. Table 1 depicts the obtained output for various input combinations.

Table 1. Truth table of proposed PTL based AND gate

A (Volts)	B (Volts)	Expected Output(Volts)	Obtained Output(Volts)
0	0	0	0.076
0	1	0	0
1	0	0	0
1	1	1	0.917

4. SIMULATION AND PERFORMANCE ANALYSIS

In order to test the performance of proposed AND cell, detailed comparisons are performed. To establish an impartial testing environment, all the circuits are simulated on same input patterns. Also the transistor sizes of the prior designs are properly tuned to have optimal performance.

The existing and proposed 2T AND gate cells are simulated using Tanner EDA Tool at BSIM 3v3 90nm technology with supply voltage ranging from 1v to 1.8v in steps of 0.2v.

Circuits are also simulated on different operating frequencies and increasing temperature at V_{DD}=1v in order to prove that the proposed designs of AND gate have better performance in terms of power consumption and overall PDP over the range of operating frequency and varying temperature. Also the proposed design has better noise immunity than the other existing ones. All the simulation results are shown in Fig.5-Fig.7.

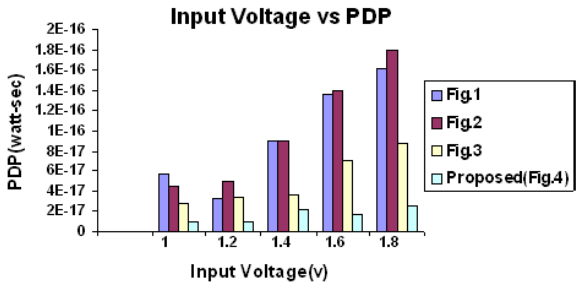

Fig 5: Power-Delay Product comparisons with increasing input voltage

Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heat sinks. An additional benefit of the reduced power consumption is the extended life of the battery

in battery-powered systems. Table 2 shows the parasitic capacitances of various AND gate cells which are extracted on 0.5submicron technology. The parasitic capacitance of proposed AND cell is having minimum value as compared to others which proves that it has least power consumption.

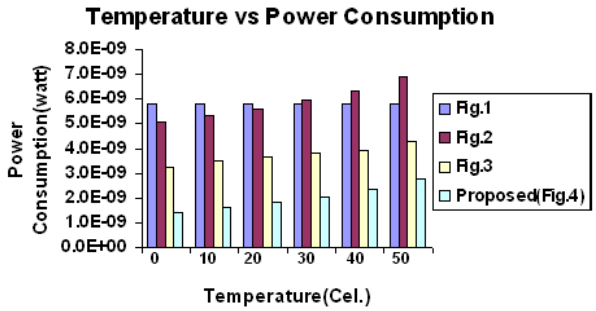

Fig 6: Power Consumption with varying temperature

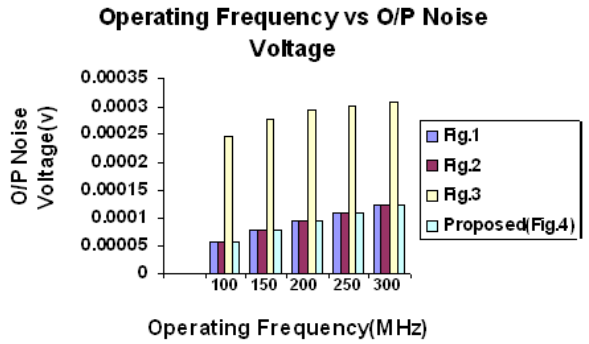

Fig 7: Output Noise voltage at different operating frequencies

Table 2. Parasitic capacitance of all AND gate designs

AND Gate Designs	Parasitic Capacitance (fF)
Fig.1	16.82631
Fig.2	8.88048
Fig.3	8.76447
Proposed(Fig.4)	**5.19561**

5. CONCLUSION

The paper is focused on the design of low power and high performance AND gate design. The proposed design is compared with traditional CMOS, complementary pass transistor (CPL) logic design and GDI technique. As a result the proposed AND cell prove its superiority in terms of power-delay product, threshold loss, temperature sustainability, noise immunity and parasitic capacitance. Hence, this new AND gate can be used for the designing of efficient multiplier and other complex systems.

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