Power Reversible Comparator Circuits 180 nm Technology

Amit Grover
Assistant Professor (ECE)
SBSSTC, Ferozepur
Punjab, India.

Sumit Khurana
Research Scholar (ECE)
SBSSTC, Ferozepur
Punjab, India.

ABSTRACT

This article explains design of reversible comparator circuits using GDI and TG in 180 nm technology, because of number of applications of reversible comparator [8] circuits in different fields. In this article, by combining CMOS-GDI circuit and CMOS-TG Circuits, we have implemented transistor of reversible gates. It has been observed that, usage of these techniques saves power and area as compare to CMOS implementation. GDI circuits provide some measure of enhanced hazard tolerance and are more suitable for low voltage operation [14]. Here transistor implementation of reversible gates is done by using Tanner tools and H-spice tools.

Keywords

Gate Diffusion Input (GDI), Transmission Gate Technology (TG).

1. INTRODUCTION

In 1960s R. Landauer demonstrated that even with high technology circuits and systems constructed using irreversible hardware, results in energy dissipation due to information loss. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping [12]. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Extra inputs or outputs are added so that the number of inputs is made equal to the number of outputs whenever it is necessary. A reversible circuit should be designed using minimum number of reversible gates along with minimum number of inputs [3, 4]. Transmission gate CMOS (TG) uses transmission gate logic to realize complex logic functions using a small number of complementary transistors. A gate diffusion input (GDI) technique [7] was presented which solves most of the problems discussed above. The GDI [5] approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS [13] and existing PTL techniques), while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library[9].

This paper is organized as follows: basic GDI functions and their circuit principles in Section II. In section III some preliminaries and full adders based on GDI- XOR and GDI-XNOR gates are described [8]. In section IV, simulation results are compared.

2. GATE DIFFUSION INPUT CELL

Fig.1. shows a GDI [7] cell which contains three inputs: (common gate input of n MOS and p MOS), P (input to the source/drain of p MOS), and N (input to the source/drain of n MOS).
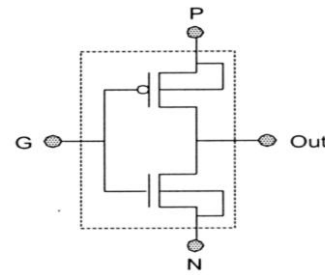

Figure 1 GDI basic cell [7]

It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS [16] or silicon on insulator (SOI) technologies.

3. TRANSMISSION GATE FUNCTIONS

Transmission gates are typically used as building blocks for logic circuitry, such as a D Latch or D Flip-Flop [11]. These can isolate components from live signals during hot insertion or removal. Fig.2. shows schematic Representation of Transmission Gate. Logic 1 voltage on node A applies Logic 0 to active-low node A, that allows to conduct both [2] the transistors whereas Logic 0 performs the reverse function, turning both the transistors off.
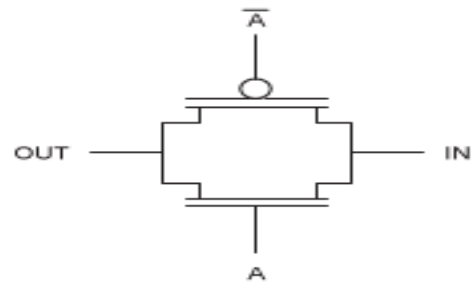
Figure2. Transmission Gate

4. SIMULATION ANALYSIS

4.1 Simulation Environment:

Comparator Circuit based on GDI and TG Technology is simulated in EDA Tanner (Evaluation version). The results are obtained in 180 nm CMOS process technology.

4.2 Comparison:

GDI and TG based Comparator circuits are compared based on the parameters like dynamic power consumption, delay and number of transistors.

4.3 GDI Based Comparator Circuit

Figure3. GDI based comparator circuit

Figure 4 Waveform of GDI based comparator circuit

4.4 TG Based Comparator Circuit

Figure5. TG based comparator circuit

Figure 6 Waveforms of TG based comparator circuit

5. RESULTS

Table 1 shows the comparative analysis of TG & GDI Based Comparators based on Dynamic power, number of transistors and delay.

Table1. Comparative Analysis of TG & GDI Based Comparator

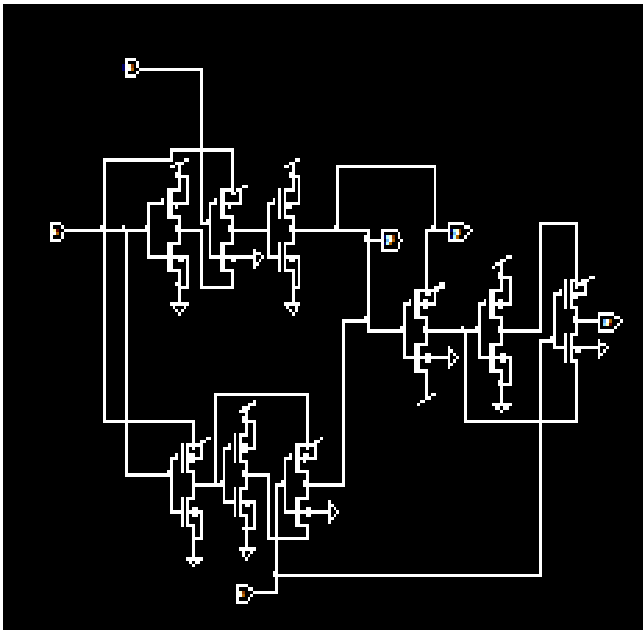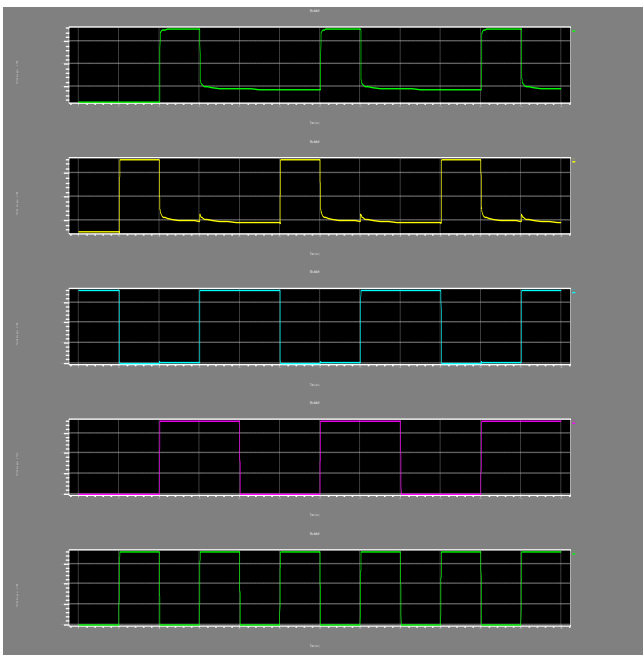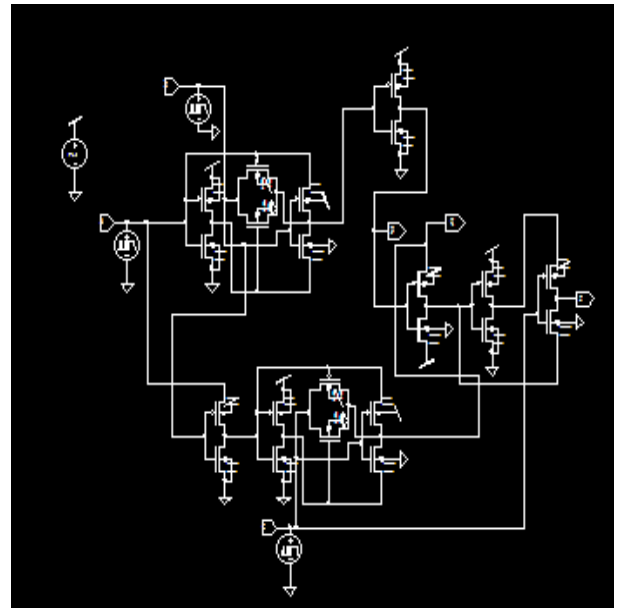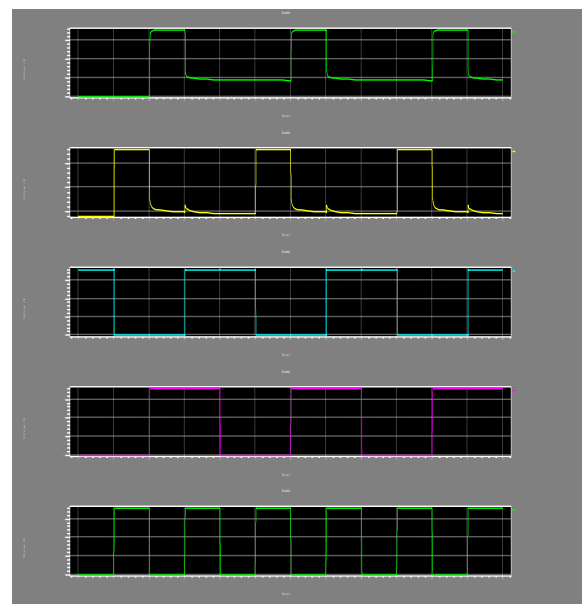| De	No. of transistors	Min Width of...	Width of NMOS (μm)	Length of PMOS (μm)	Average Power Consumption	Propagation Delay at P	Propagation Delay at Q	Propagation Delay at R
G	18	0.1	0.64	1.7	4.62×10^{-5}	2.08×10^{-10}	7.37×10^{-10}	1.27×10^{-9}
T	22	0.1	0.64	1.7	1.91×10^{-4}	2.77×10^{-10}	1.09×10^{-9}	1.65×10^{-9}

6. CONCLUSIONS

An optimized reversible comparator is presented using GDI & TG based Comparators. Based on transistor count, delay and average power consumed, the performance of both the methods has been considered using180 nm technology. It has been concluded that when we use 180nm technology than GDI based comparator consume lesser power.

7. REFERENCES

[1] C.H. Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, pp. 525-532, November 1973.

[2] Y.-C. Hung and B.D. Liu: "1-V CMOS Comparator for Programmable Analog Rank-Order Extractor", IEEE Transactions Circuits and Systems, Vol. 50, No. 5, 2003, pp. 673-677.

[3] Lihui Ni, Zhijin Guan, Xiaoyu Dai, Wenjuan Li, "Using New Designed NLG Gate for the Realization of Four-bit Reversible Numerical Comparator", 2010 International Conference on Educational and Network Technology (ICENT 2010), 5, 978-1-4244-7662, 2010 IEEE.

[4] E. Fredkin and T. Toffoli, "Conservative logic," International Journal of Theoretical Physics, vol. 21, pp. 219–253, 1982.

[5] Arkadiy Morgenshtein, Michael Moreinis and Ran Ginosar," Asynchronous Gate-Diffusion-Input (GDI) Circuits" Very Large Scale Integration (VLSI) Systems, IEEE Journal Transactions, Aug. 2004.

[6] A. Morgenshtein, A. Fish, I. A. Wagner, "Gate-Diffusion Input (GDI) – A Novel Power Efficient Method for Digital Circuits: A Detailed Methodology," 14th IEEE International ASIC/SOC Conference, USA, September 2001.

[7] D. P. Vasudevan, P. K. Lala, J. Di and J. P. Parkerson, "Reversible-logic design with online testability", IEEE Transactions on Instrumentation and Measurement, vol.55, no.2, pp.406- 414, April 2006.

[8] A N Nagamani, H V Jayashree, H R Bhagyalakshmi, "Novel Low Power Comparator Design using Reversible Logic Gates" Indian Journal of computer Science and Engineering , Vol. 2 No. 4 Aug - Sep 2011.

[9] B. Wicht, T. Nirschl and D. Schmitt-Landsiedel: "Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier", IEEE J. Solid-State Circuits, Vol. 39, No. 7, 2004, pp. 1148-1158.

[10] K.-L. J. Wong and C.-K. K. Yang: "Offset Compensation in Comparators with Minimum Input-referred supply Noise", IEEE J. Solid-State Circuits, Vol. 39, No. 5, 2004, pp. 837-840.

[11] H. J. M. Veendrick: "The Behavior of Flip-Flops Used as Synchronizers and Prediction of Their Failure Rate", IEEE J. Solid-State Circuits, Vol. 15, No. 2, 1980, pp. 169-176

[12] H.P. Le, A. Zayegh, and J. Singh, "Performance analysis of optimized CMOS comparator," Electronics Letters, vol. 39, pp. 833-835, May 2003.

[13] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 0.35μm CMOS Comparator Circuit for High-Speed ADC Applications," IEEE International Symposium on Circuits and Systems, pp. 6134-6137, May 2005.

[14] T. W. Matthews, P. L. Heedley, "A Simulation Method for Accurately Determining DC and Dynamic Offset in Comparators," IEEE MWSCAS, pp. 1815-1818, Aug. 2005.

[15] B. Razavi and B .A. Wooley, "Design Techniques for High-Speed High-Resolution Comparators," IEEE Journal of Solid-State Circuits, Vol-27, pp.1916-1926, Dec 1992.

[16] A. Boni, G. Chiorboli and C. Morandi: "Dynamic characterization of high-speed latching comparators", IEEE Electron. Letters Vol. 36, No. 5, 2000, pp. 402-404.

[17] R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11–20, 1985.

[18] K. Uyttenhove, M. S. J. Steyaert: "A 1.8-V 6-Bit 1.3-GHz Flash ADC in 0.25-μm CMOS", IEEE J. Solid-State Circuits, Vol. 38, No. 7, July 2003, pp. 1115-1122.

8. AUTHOR'S PROFILE

Amit Grover (M'06-SM'09-PI'11&12) The author became a Member (M) of Association ISTE in 2006, a Senior Member (SM) of society SELCOME in September 2009, and a Project-In charge (PI) in august 2011 and in September 2012. The author place of birth is Ferozepur, Punjab, India on 27th, September 1980.The author received his M. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthla, Punjab, India in 2008 and received his B. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthala, Punjab, India in 2001. Currently, he is working as an Assistant Professor in Shaheed Bhagat Singh State Technical Campus, Ferozepur, Punjab, India. The author is a Reviewer of many International Reputed Journals. His area of interest includes signal processing, MIMO systems, Wireless mobile communication, High speed digital communications, 4G Wireless Communications and VLSI Design.

Sumit Khurana received his B. Tech degree in ECE from LLRIET, Moga affiliated to PTU, Jallandhar, Punjab, India in 2011. At present he is doing his research work under the guidance of Amit Grover, Assistant Professor, ECE, SBSSTC, Ferozepur, Punjab, India. His place of birth is Ferozepur, Punjab, India on 22nd, May, 1989. His area of interest includes signal processing and VLSI Design.