Design and Analysis of Gain Boosted Recycling Folded Cascode OTA

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ABSTRACT

In this paper, a low Power, Gain Boosted Recycling Folded Cascode Operational Transconductance Amplifier (GB-RFC OTA) is described. The proposed GB-RFC OTA is designed using 130nm CMOS technology and achieves enhanced gain, unity gain bandwidth and slew rate with the low Power budget. The proposed circuit operates on 1V supply voltage and 200 μ A bias current and consumes a power of 798 μ W.The GB-RFC has about 24dB higher gain and 37MHz higher unity Gain Bandwidth (GBW) compare to Double Recycling Folded cascode OTA (DRFC).

General Terms

Unity Gain Bandwidth, Gain, Slew Rate, Phase Margin, Transconductance.

Keywords

Operational Transconductance Amplifier (OTA), Current recycling, Gain Boosting, Folded-cascode, CMOS

1. INTRODUCTION

Because of the growing market of battery operated mobile and portable electronic devices, the low voltage and low power supply is becoming one of the important research area in today's electronics industry. The power consumption is becoming as important as speed, gain and GBW. The OTA is still playing a dominant role in many analog designs. OTA is an amplifier whose differential input voltage produces an output current. So, it is a Voltage Controlled Current Source (VCCS) [1] [7].

$$I_{out} = (V_{in}(+) - V_{in}(-))g_m$$
(1)

The output current is a function of input differential voltage and transconductance of the circuit. The gain is represented by the product of effective transconductance and output impedance of the circuit.

$$A_o = g_{m,eff} R_{out} \tag{2}$$

Although the Folded Cascode (FC) OTA is providing a good optimization in term of different performance parameters like gain, GBW, output voltage swing, slew rate, power consumption as compare to Two stage OTA and Telescopic Cascode OTA. The current recycling has been emerged to improve the performance of conventional Folded Cascode OTA within the same area and power budget.

Previously R.Assad has proposed the Recycling Folded Cascode Operational Transconductance Amplifier (RFC OTA) (Fig. 1) in which the input drivers M1 and M2 has splitted into M1a and M1b and M2a and M2b.Next M3 and M4 are splitted to form the current mirror M3a:M3b and M4a:M4b with a ratio of K:1 to enhance the effective transconductance. Which enhance the other parameters such as Gain bandwidth and speed of the amplifier within same area and power budget. [2]

K.f.Han and Y.L.Li has proposed Improved Recycling folded Cascode (IRFC) in which the extra shunt current source separates the AC and DC path and achieves the enhancement in transconductance within the same area and power budget. [3]

The Zushu yan proposed Double Recycling folded cascode OTA (DRFC) which replaces the input pair by triplet and shunt current sources are replaced by current mirrors. This method again recycles the shunt bias currents to further enhance the performance of OTA. [4]



Fig 1: Recycling Folded Cascode OTA

In this paper a Gain Boosted Recycling Folded Cascode Operational Transconductance Amplifier (GB-RFC OTA) is described in which the Gain is enhanced by increasing the output impedance of the circuit with the addition of extra cascoded gain stage which will further enhance the different parameters within the same area and power budget.

This paper organized as follows: the basics of proposed modifications are discussed in section II. Section III presents the Proposed GB-RFC OTA and the simulation results are presented in section IV. Finally, the Section V presents the conclusions.

2. CIRCUIT DESCRIPTION

In the GB RFC operational transconductance amplifier the gain is enhanced by increasing the output impedance of the circuit by providing the cascoded gain stage. The high gain often causes to instability so to achieve the stability and significant phase margin the miller compensation is used. As we know Dc gain can be expressed as

$$A_o = g_{m,eff} R_{out} \tag{3}$$

Where g_{meff} is the effective transconductance and R_{out} is the output impedance of the circuit.

So in order to increase the gain either the Transconductance or the output impedance can be enhanced but we know that the transconductance increases as square root of increase in bias current which cause to increase in power consumption. The transconductance is given by the expression:

$$g_m = \sqrt{\frac{2\mu c_{ox}(\frac{w}{l})I_D}{1+\lambda V_{Ds}}} \tag{4}$$

Where the symbols have their usual meaning of μ is the surface mobility of channel, C_{ox} is capacitance per unit area of gate oxide, W is effective channel width, L is effective channel length, λ is channel length modulation factor, I_D is drain current and V_{DS} is Drain to Source voltage.

But the output resistance \boldsymbol{r}_{o} is given by the expression:

$$r_{o} = \frac{1}{\frac{1}{2}\mu_{o}c_{ox}W/l(V_{GS} - v_{th})^{2}\lambda}$$
(5)

$$r_o = \frac{1}{I_D \lambda} \tag{6}$$

The output impedance can be enhanced in proportion to decrease in bias current. So in order to lower the power consumption it is better to increase the output impedance by decreasing the bias current.

2.1 Gain Boosting

The cascoded structures as shown in Fig. 2 are widely used to boost the gain [5] [7]. The transfer function of the cascode stage can be written as

$$\frac{\Delta I_o}{\Delta V_1} = \frac{g_{m1}(g_{m2}r_{01} + {}^{I_01}/r_{02})}{(g_{m2}r_{01} + {}^{r_{01}}/r_{02} + 1)} = g_{meff}$$
(7)

Which is approximately equal to g_{meff} , the output voltage V_o is given by

$$\Delta V_{o} = \Delta I_{o} R_{out} \tag{8}$$

Where Rout is the output impedance of the whole circuit and is given by

$$R_{out} = (g_{m2}r_{o2} + 1)r_{o1} + r_{o2}$$
(9)

$$R_{out} \cong g_{m2} r_{o2} r_{o1} \tag{10}$$

It produces the following expression of Dc gain (A_o)

$$A_{o} = g_{m1}r_{o1}(g_{m2}r_{o2} + 1)$$
(11)





2.2 Miller Compensation

Although the multistage amplifiers may be used for high gains but such kind of high gain amplifiers are generally difficult to compensate [7] [20]. So we have to implement some compensation techniques to achieve the stability and significant phase margin. So in this design Single Miller Compensation Nulling Resistor (SMCNR) is used in which we place a compensation capacitor between the input and output nodes of the second inverting stage of the amplifier and the dominant pole is created due to Miller feedback and it will helps us to increase the high midband gap without affecting its dc response.

But as the transistor gain of second stage increases the dominant poles decreases and non dominant pole increases and poles are split apart to stabilize the amplifier but this method also introduces a Right Half Plane (RHP) zero which causes negative phase shift and stability decreases. This zero arises because of the direct feed through of input to output through Miller capacitor. In order to increase the phase margin the RHP should be eliminated and lead compensation technique in which a nulling resistor in series with the compensation capacitor is used to increase the impedance of feed through path.



Fig 3: SMCNR

3. PROPOSED GB-RFC OTA

It is real challenge to design the low power and high gain operational transconductance amplifier and to achieve the optimization among different performance parameters such as Gain, Phase Margin, Unity Gain Bandwidth, input referred noise and slew rate. The different configurations of OTA are discussed like Single stage OTA, Two stage OTA, Telescopic OTA and folded cascoded OTA. The two stage OTA provides high gain and UGB as compare to single stage OTA with increased complexity and low speed. The Telescopic Configuration provides further increase in Gain, UGB and speed but the voltage swing is reduced at the output.

Folded cascode amplifier is a good compromise between the two stage amplifier and telescopic cascode amplifier. It helps us to better optimize the values at low power supply voltages. The inefficiency of folded cascode OTA was overcome by recycling folded cascode OTA in which we are reusing or recycling the existing devices or currents to perform additional task speed but the voltage swing is reduced at the output. In the proposed GB RFC OTA the gain is enhanced by increasing the output impedance because the output resistance increases in proportion to decrease in bias current.

So it makes the circuit power efficient to increase the output impedance by lowering the currents. The cascode gain stage is attached as shown in Fig. 4 to enhance the performance parameters.

The output impedance of the RFC circuit is given by:

$$R_{oRFC} = gm_6 r_{ds6} (r_{ds2a} || r_{ds4a}) || gm_8 r_{ds8} r_{ds10}$$
(12)

The output impedance of GB-RFC is given by:

$$R_{out} = gm_{13}r_{013}r_{014}(R_{oRFC})$$
(13)

The circuit is characterized by performance parameters like Dc gain, UGB, Phase Margin, slew rate, noise and power. The different measures are fixed by various parameters like bias current, supply voltage, transistor size and biasing.



Fig 4: GB-RFC OTA

4. SIMULATION RESULTS

The amplifier is fabricated using 130nm CMOS technology and voltage supply of 1V. The simulations are done with the help of Tanner EDA tool T-Spice and the different performance parameters like gain, UGB, phase margin, Slew rate are analyzed using W Edit. In comparison to previous designs like RFC OTA, IRFC OTA and DRFC OTA the GB RFC OTA has better performance parameters. The number of transistor in the proposed design is less as compare to DRFC OTA.

The DC voltage gain for the circuit is 78.8dB which is 24.3dB more as compare to DRFC and the GBW of DRFC and GB RFC is 203.2 MHz and 240 MHz respectively which reflects the enhancement of 37 MHz as shown in Fig. 5.



Fig 5: Gain

The gain variation of 10 dB and phase margin of 5^0 is observed with the temp variation of -20° C to 100° C. That reflects that there is very little effect of temperature on its performance parameters.

Table 1. Effect of Temperature on different parameters

Parameter	Temp.	Temp.	Temp.	Temp.	Temp.
	(-20°C)	(0°C)	(50°C)	(75°C)	(100°C)
Gain	74.36	75.64	80	82	84
GBW	262	251	212	195	186
Phase Margin	56	57.2	51	51.3	51.3

The phase Margin of 55.09 deg is observed as shown in Fig. 6 with a small reduction of phase Margin as compare to DRFC. The maximum and minimum power consumption of the circuit is 798.8μ W and 602.9μ W respectively as shown in Fig.7. The bias current of 200 μ A is used to make the circuit of GB RFC power efficient as compare to 800 μ A in RFC and DRFC.



Fig 8: Amplifier large signal step response

The spectral density of input referred noise when calculated over a frequency range of 1Hz to 100MHz is found to be 28.4 μ Vrms. In order to measure the slew rate, a large step signal of 1.5V at 5 MHz was applied to amplifiers and results are given in Fig.8.The average slew rate of 102.05V/µs is achieved using a capacitive load of 2.5pF.

Parameters	RFC	IRFC	DRFC	GB RFC
Supply voltage(V)	1	1	1	1
Bias current (µA)	800	260	800	200
Capacitive load (pF)	5.6	7	10	2.5
DC gain (dB)	53.6	70.2	54.5	78.8
GBW (MHz)	134.2	83	203.2	241
Phase margin (deg)	70.6	70	66.2	55.09
SR+/SR-(V/µs)	94.1(avg)	21.2/38. 4	84.1/91. 6	99.25/10 4.8
1% Settling time (Ts+/Ts-) (ns)	11.2	NA	10.7/9.5	10.34/9.8 5
Input referred noise (1 Hz–100 MHz) (µVrms)	48.5	NA	25.8	28.4
Power consumption (µW)	2580	841.48	NA	700
FOM1 (MHz.pF/mA)	939.4	2235	2,540	3012.5
FOM2 [(V/µs)*pF/mA]	658.7	802.30	878.5	1275.31

Table 2. Performance Comparison of different OTA structures

* Average slew rate is used to calculate the FOM2.

5. CONCLUSION

A GB RFC OTA showing significant performance enhancement over the existing configurations like FC, RFC [2], IRFC [3] and DRFC [4] is designed using 130nm CMOS technology .The output impedance of the circuit is enhanced by providing the cascode gain stage at the output and a significant increase in Gain, GBW and slew rate is achieved within the same power budget. The Miller compensation technique is used to increase the phase margin of the circuit.

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