# Design and Synthesis of QPSK: A Subsystem Module of Digital Communication using Reversible Logic

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## ABSTRACT
In this paper we are implemented BPSK modulation technique, a subsystem module of digital communication using reversible logic. Later on we have implemented a QPSK modulation technique using reversible logic and The QPSK modulator unit will be modelled using HDL code and simulation will be done by ModelSim 6.0 simulator to verify their functionality in the system. The digital system of QPSK is designed using a reversible logic gates which yields in low power, less required area and less amount of delay. Reversible logic is mainly used to construct low power circuits and also used in quantum computing, optical computing and DNA computing to produce zero power dissipation. QPSK is widely used modulation technique in satellite radio applications.

## Keywords
Reversible Logic, Reversible Gate, Garbage output, VHDL Code.

## 1. INTRODUCTION
In Quadrature phase shift keying modulation a sinusoidal waveform is varied in phase while keeping the amplitude and frequency are constants. The term Quadrature represents that there are only four possible phases.

The general expression for a QPSK waveform as shown in equation (1),

$si(t) = A\cos[\omega c\, t + \phi 0 + \phi\, i\,(t)]$……(1)

where

$si$ represents the PSK signal waveform for phase $i$

$t$ represents time

$A$ represents the peak amplitude

$\omega c$ represents the carrier frequency in radians/s ( $\omega c = 2\pi fc$ )

$\varphi 0$ represents the reference phase angle

$\varphi i$ represents the phase $i$

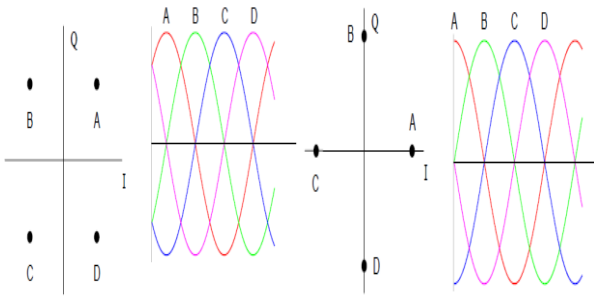
$i$ ranges from 1 to 4

The instantaneous phase having discrete values equal to $\Phi + 2\pi i/4$ where $i$ = 1, 2, 3, or 4.

## 2. QPSK CONSTELLATIONS
In QPSK, therefore, Phase States $M$ = 4 and the phases are separated by 90, Figure 1 shows two common representations of the QPSK constellation. The constellation points are arbitrarily taken as A, B, C and D, each of these represents one of the four possible di-bits 00, 01, 10, and 11. The mapping between the di-bits and the constellation points depends on the modulator circuit which we are going to design.

In the fallowing two representations, the four phases are spaced 90° ($\pi/2$ radians) apart and the difference is the choice of the reference phase angle in both the cases. In Figure 1 (a)

the reference phase angle is $\varphi = \pi/4$ and In Figure 1 (b) the reference phase angle is $\varphi = 0$.




a) QPSK ($\varphi = \pi/4, 3\pi/4, 5\pi/4, 7\pi/4$) b) QPSK ($\varphi = 0, \pi/2, \pi, 3\pi/2$)

**Figure 1: QPSK constellation and waveforms.**

## 3. QPSK MODULATION
The generation of the QPSK signal is usually done by modulating two carriers in Quadrature independently (cos ωt and sin ωt), as shown in Figure 2.

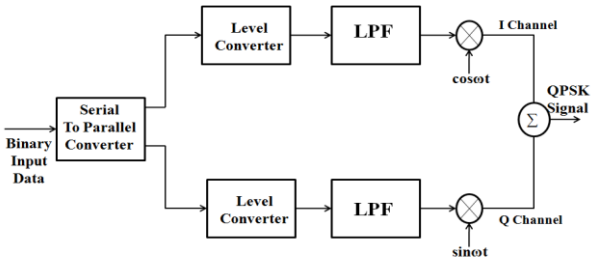



**Figure 2: Simplified block diagram of a QPSK modulator.**

Quadrature Phase Shift Keying is generated by two independent BPSK systems (I and Q), and exhibits the same performance but bandwidth efficiency will be double. The Serial to Parallel Converter groups as di-bits from the binary data input. Two bits have been clocked at a time serially into its buffer, the Serial to Parallel Converter outputs one di-bit in parallel at its two outputs.

From the di-bit, One bit is sent to the I channel of the modulator and the other bit is sent to the Q channel of the modulator and the modulators will be working independently for each channel to processes the stream of bits it receives.

In order to convert the data into a bipolar pulse stream we use Level converter the converted data is applied to one input of the mixer. A Low-Pass Filter (LPF) is usually used before the mixer in each channel of the modulator to restrict the bandwidth of the QPSK signal, in order to provide the desired spectral shaping.

The sinusoidal carriers of I-channel and Q-channel are cosωt and sinωt respectively, and they are in Quadrature. The modulation is performed by each mixer by multiplying the

carrier with the bipolar data signal in order to produce a BPSK signal.

Finally two BPSK signals are summed to produce the QPSK signal. Because these two BPSK signals are generated by considering two carriers in phase Quadrature, the BPSK signals are orthogonal, and the QPSK demodulator will be able to demodulate them separately. Figure 3 shows generation of QPSK signal by two BPSK signals.

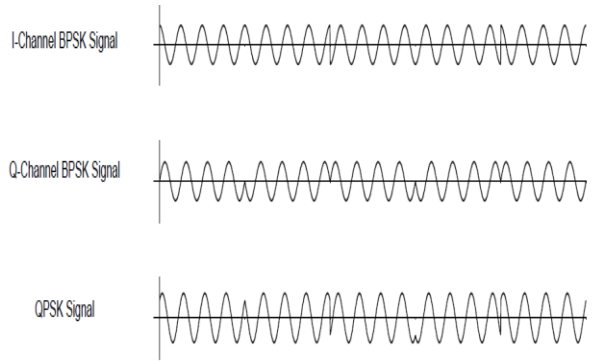



**Figure 3: QPSK signal generation from two BPSK signals.**

## 4. TYPES OF QPSK

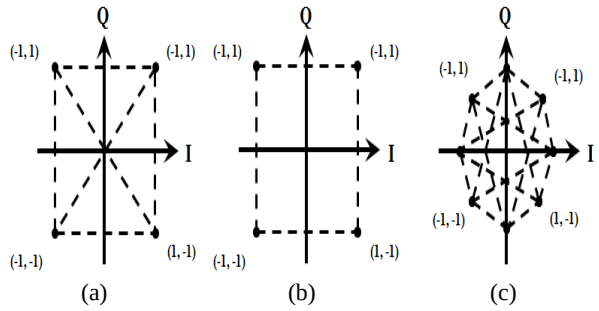



**Figure 4: (a) Conventional QPSK, (b) Offset QPSK and (c) π/4 QPSK**

In QPSK we have following types

(a) Conventional QPSK: In Conventional QPSK have transitions through zero ie. Phase transition is $180^0$ .

(b) Offset QPSK: In Offset QPSK the transitions are straggered on the I and Q channels. Phase transition limited to $90^0$.

(c) π/4-QPSK: In π/4-QPSK the set of constellation points are toggled each symbol, so transitions through zero cannot occur. This scheme produces the lowest envelope variations. Where I = In phase channel, Q = Quadrature channel

## 5. REVERSIBLE LOGIC GATES

Everyday new technology is developing rapidly, The clock frequency also increasing continuously to achieve greater speed and also number of transistors packed onto a chip increases to achieve complexity of a conventional system results in increased power consumption. Hence Reversible logic is the efficient technique in the recent trends due to its less heat dissipating characteristics.

**Moore's law** predicts exponential growth of heat generated due to information loss which will be an intolerable amount in the next decade. This heat dissipation dramatically reduces the performance and lifetime of the circuits. The solution is to use revolutionary technology which enables extremely low power consumption and heat dissipation in computing.

As per Landauer [1], for irreversible logic, each bit of information lost generates kTln2 Joules of heat energy, where k is Boltzmann's constant and T is absolute temperature at which the computation is performed. For room temperature T, the amount of heat dissipated for one bit is small i.e. 2.9×10-21 J.

Bennett [2] showed that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation.

Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. More formally, a **reversible** logic gate is a *k*-input, *k*-output (denoted *k***k*) device that maps each possible input pattern into a unique output pattern. While constructing reversible circuits with the One extra output should be produced to make the circuit reversible and that unwanted output (P=A, marked as *) is known as garbage.

In reversible logic, The Input vector is represented as shown in equation (2),

$I_v=( I_{i,j} , I_{i+1,j} , I_{i+2,j} , \ldots, I_{k-1,j}, I_{k,j} )$……(2) and

The Output vector is represented as shown in equation (3),

$O_v=( O_{i,j} , O_{i+1,j} , O_{i+2,j} ,\ldots, O_{k-1,j}, O_{k,j} )$…...(3) For each particular vector j $I_v \leftrightarrow O_v$.

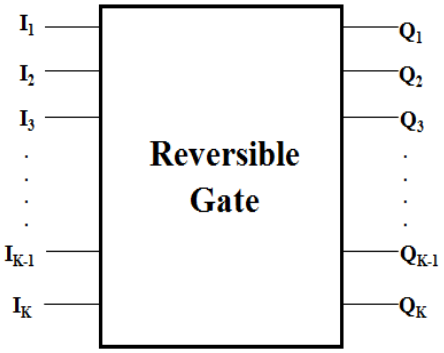



**Figure 5: General Reversible Gate**

A reversible gate which is used to design QPSK in reversible logic is

**4*4 Reversible DKG Gate:**

A 4* 4 reversible DKG gate can work singly as a reversible Full adder and a reversible Full Subtractor is shown in Figure.6. It has A,B,C and D are the input vectors and P=B,Q=AC+AD,R=(A+B)(C+D)+CD and S=B+C+D are the output vectors. The implementation of 4*4 Reversible DKG Gate as a full adder and as a full Subtractor is shown in Figure 7 and Figure 8 respectively. If input A=0, this gate works as a reversible Full adder, and if input A=1, then it works as a reversible Full Subtractor.

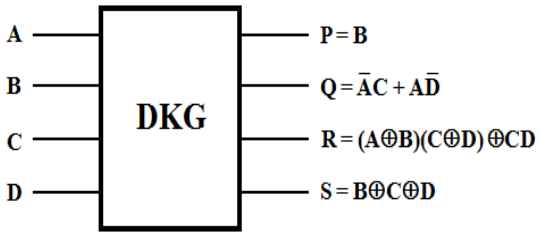



**Figure 6: Reversible DKG gate**

If input A=0, the proposed gate works as a reversible Full adder,

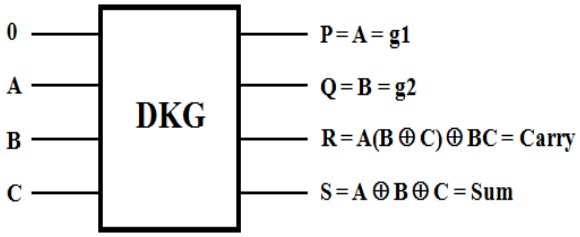



**Figure 7: DKG gate implemented as Full adder**

If input A=1, then it works as a reversible Full Subtractor.

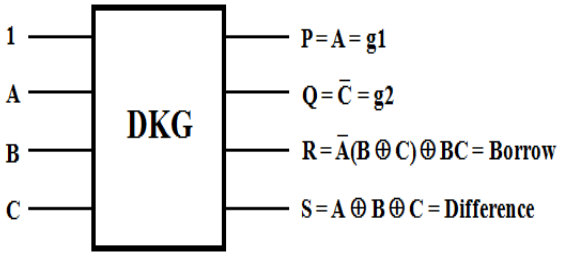



**Figure 8: DKG gate implemented as Full Subtractor**

**Application of Reversible Logic**

The Reversible logic will have several Applications. Some of the potential application areas of reversible logic include the following:

- Nanocomputing
- Bio Molecular Computations
- Laptop/Handheld/Wearable Computers
- Spacecraft
- Implanted Medical Devices
- Wallet "smart cards"
- " Smart tags" on inventory

## 6. BPSK DESIGN USING REVERSIBLE LOGIC

The BPSK (Binary Phase Shift Keying) is one of the basic binary modulation techniques [5]. It has as a result only two phases of the carrier, at the same frequency, but separated by 180º. Binary data are represented by two signals with different phases in BPSK. Typically these two phases are 0 and π.

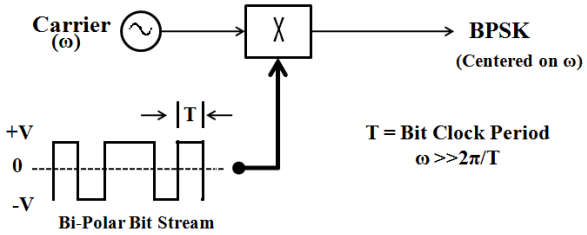



**Figure 9: Generation of BPSK**

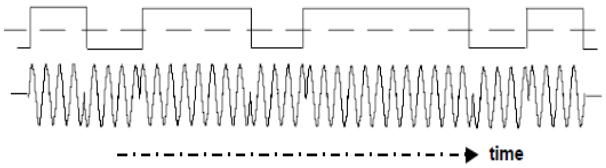



**Figure 10: A BPSK signal in the time domain**

The General expressions for the BPSK signals are as shown in equation (4) and equation (5)

s1 (t) = Acos 2πfct, $0 \le t \le T$, for 1 ……..……. (4)

s2 (t) = −Acos 2πfct, $0 \le t \le T$, for 0 …….. (5)

The sinusoidal carrier is modulated by a bi-polar bit stream according to the scheme illustrated in Figure 9, its polarity will be reversed every time the bit stream changes polarity. This, for a sine wave, is equivalent to a phase reversal (shift). The multiplier output is a BPSK signal shown in Figure 10. The Figure 11 shows the top level RTL schematic for BPSK and Figure 12 shows the inner components of RTL schematic for BPSK.

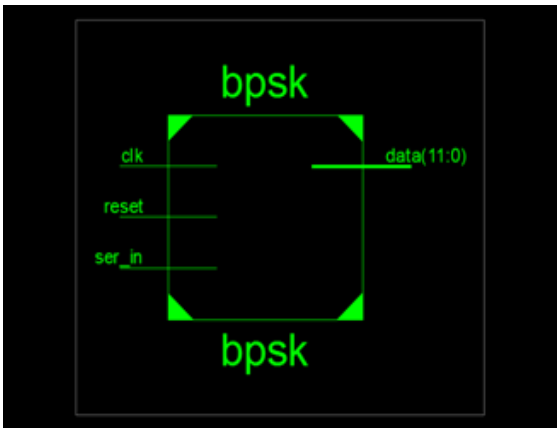



**Figure 11: Top level RTL schematic for BPSK**

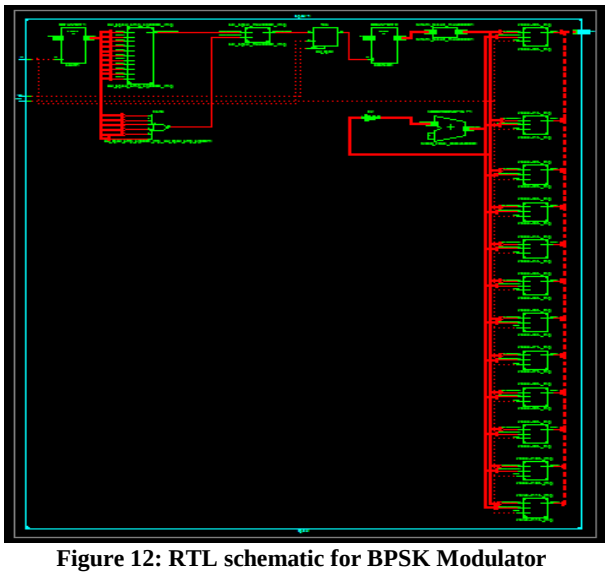


**Figure 12: RTL schematic for BPSK Modulator**

The Figure 13 shows the simulation result for one address bit of I-Channel BPSK signal, Figure 14 shows the simulation result for all 32 address bits of I-Channel BPSK signal. The Figure 15 shows the simulation result for one address bit of Q-Channel BPSK signal, Figure 16 shows the simulation result for all 32 address bits of Q-Channel BPSK signal.

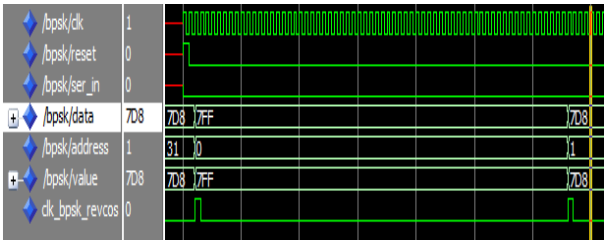



**Figure 13: I-Channel BPSK Signal for one address bit**


**Figure 14: I-Channel BPSK Signal for 32 address bits**

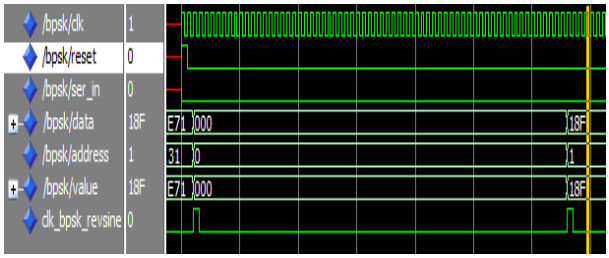



**Figure 15: Q-Channel BPSK Signal for one address bit**


**Figure 16: Q-Channel BPSK Signal for 32 address bits**

## 7. QPSK DESIGN USING REVERSIBLE LOGIC

The modulators are the basic requirement of the communication systems they are designed to reduce the channel distortion & in RF communication many type of carrier modulation techniques has been already proposed according to channel properties & data rate of the system. Here we are proposing QPSK modulator using Reversible logic, the proposed system has many advantages over Conventional QPSK modulators such as low power, less required area and less amount of delay. The simulation of the system proves all the features mention above. The Figure 17 shows the RTL schematic for QPSK Modulator and Figure 18 shows the inner components of RTL schematic for QPSK modulator

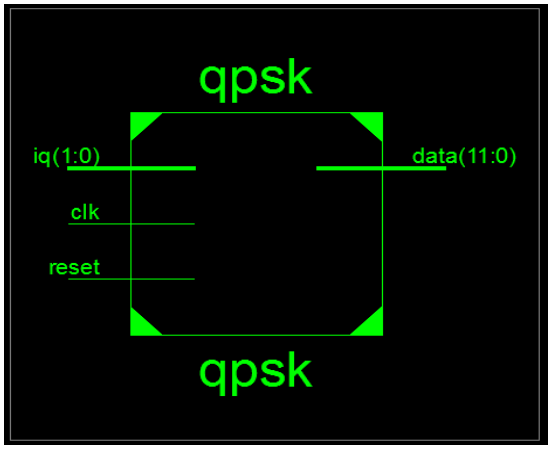



**Figure 17: Top level RTL schematic for QPSK**

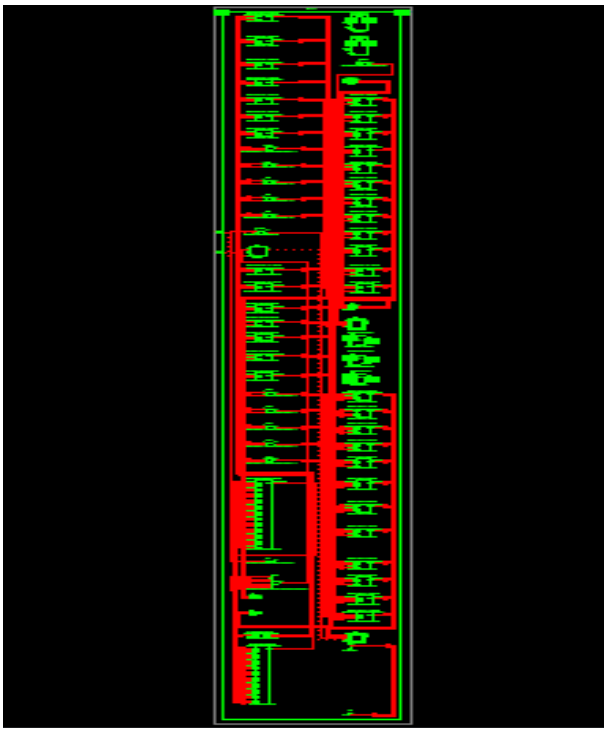


**Figure 18: RTL schematic for QPSK Modulator**

## 8. SIMULATION RESULTS OF QPSK MODULATION TECHNIQUE

The proposed modulator programmed with the VHDL language for modelling, design and analysis of the proposed QPSK modulator. The Figure 19 shows the simulation result for one address bit of QPSK signal, Figure 20 shows the simulation result for all 32 address bits of QPSK signal.

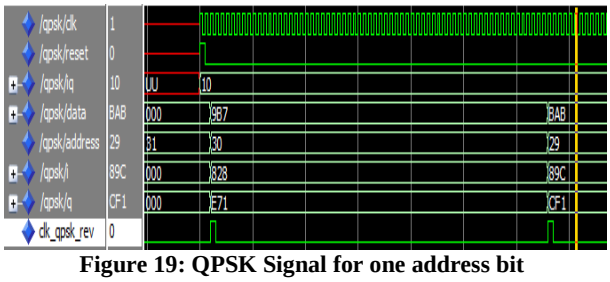



**Figure 19: QPSK Signal for one address bit**

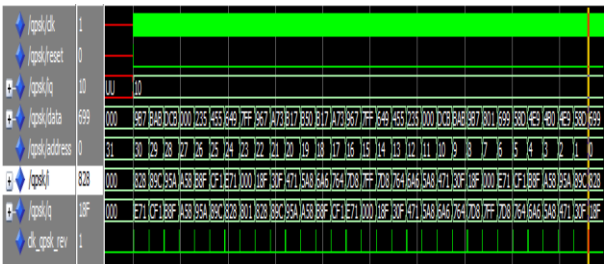


**Figure 20: QPSK Signal for 32 address bits**

## 9. CONCLUSION

This paper proposes the implementation of a subsystem module of digital communication like...QPSK modulation using reversible logic is done. The design of reversible logic QPSK modulator unit will be done by using 4*4 Reversible DKG Gate and QPSK modulator unit will be modeled using HDL code and simulation will be done by ModelSim 6.0 simulator to verify their functionality.

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