A Novel Design of Carry Skip BCD Adder using Reversible Gates

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ABSTRACT
In this paper revolves around the design and implementation of Carry Skip BCD adder using reversible logic to improve the design in terms of the number of garbage outputs and the number of gates used. In recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology and optical computing because of its zero power dissipation under ideal conditions. In this paper, the reversible logic implementation of Carry skip BCD adder is done so as to minimize the number of gates used and their garbage outputs. The existing and the proposed Carry skip BCD adders are designed using Verilog and simulated using Xilinx ISE 9.1i tool.

Keywords
Reversible Gate, Garbage Outputs, Constant inputs, Quantum Cost.

1. INTRODUCTION
In modern VLSI systems, power dissipation is very high due to rapid switching of internal signals. It has been shown that for every bit of information lost in irreversible logic computations, kT*log2joules of heat energy is generated, where kis Boltzmann's constant and T isthe absolute temperature at which computation is performed. But this power dissipation can be avoided if the circuit is made reversible by using reversible gates in place of conventional logic gates. A reversible circuit is one in which the inputs can be reproduced from the outputs and vice versa. A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. The inputs to reversible gates can be uniquely determined from its outputs. A reversible logic gate must have the same number of inputs and outputs. A reversible gate is balanced, i.e. the outputs are 1s for exactly half of the inputs. A circuit without constants on its inputs and composed of reversible gates realizes only balanced functions. It can realize non balanced functions only with garbage outputs. Garbage outputs are those outputs that are not used as inputs to other circuit blocks. Some of the major problems with reversible logic synthesis are that fan outs cannot be used, and also feedback from gate outputs to inputs is not permitted [2]. In current literature most of the researchers realized complex gate using realizable gates and the cost is significantly high. They used the circuit as a single gate in their design to claim success in terms of number of gates. Although the number of gates is proposed as a major metric of optimization [3]. Reversible gates have applications in Nuclear Magnetic Resonance (NMR), quantum computation, Quantum dot Cellular Automata (QCA), and optical computing. The most prominent application of reversible logic lies in quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates. The main objective of this project is to design and implement a 4-bit Carry skip BCD adder such that,

- Minimum number of gates are used for implementation
- The number of garbage outputs are restricted to as few as possible
- Minimum number of constant inputs are used
- Following are the need of reversible circuits:
- To reduce the amount of heat dissipation due to information loss in irreversible circuits, reversible circuits are used.
- Reversible logic circuits are in demand for high speed power efficient circuits and are needed to recover the state of inputs from outputs.
- Reversible computing will lead to improvement in energy efficiency which will eventually affect the speed of most computing applications.
- To increase the portability of devices again reversible computing is required [4].

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2. DIFFERENT TYPES OF REVERSIBLE LOGIC GATES

2.1 Not Gate
The simplest reversible gate is the NOT gate and it is a 1*1 gate. This NOT Gate has a Quantum Cost of zero and is as shown in Fig 1.

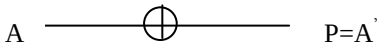


Fig.1: NOT Gate

2.2 Feynman / CNOT Gate
Controlled NOT (CNOT) gate is an example for a 2*2 gate. This reversible 2*2 gate with Quantum Cost of one having a mapping input (A, B) to output (P = A, Q = A^B) is as shown in Fig 2

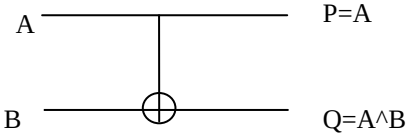


Fig.2: CNOT Gate

2.3 Double Feynman Gate
The Double Feynman gate (F2G) is a 3*3 reversible gate with three inputs and three outputs. This reversible 3*3 gate with a Quantum Cost of 2 has a mapping input (A,B,C) to the output (P=A,Q=A^B,R=(A^C)) is as shown in Fig 3.\

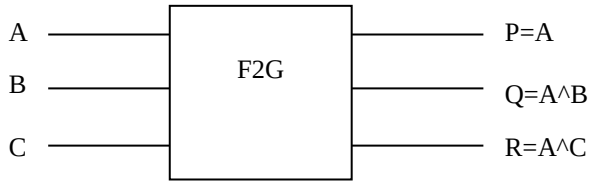


Fig .3: Double Feynman Gate

2.4 Toffoli Gate

The Toffoli gate is a 3*3 reversible gate with three inputs and three outputs. Toffoli gate is one of the most popular reversible gates and has a Quantum Cost of 5.This reversible 3*3 gate having a mapping input (A,B,C) to the output (P=A,Q=B,R=(A*B)^C) is as shown in Fig 4.

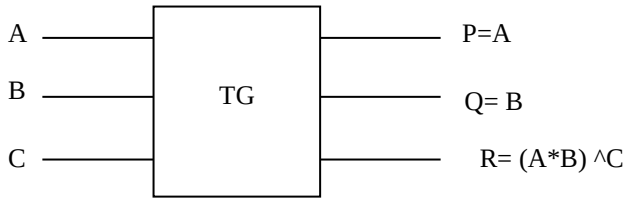


Fig .4: Toffoli Gate

2.5 Peres Gate

The Peres gate is a 3*3 reversible gate having inputs (A, B, C) mapped to outputs (P = A, Q =A^B, R = (A*B)^C).This gate has a Quantum cost of 4 and is as shown in Fig 5.

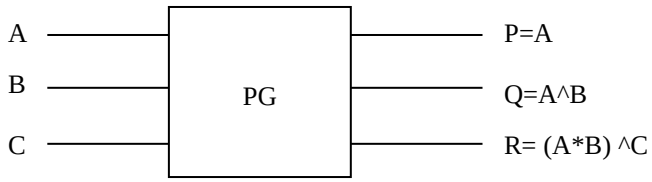
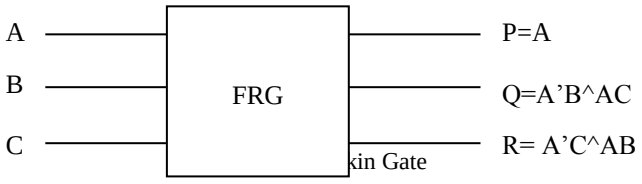


Fig.5: Peres Gate

2.6 Fredkin Gate

The Fredkin gate is a reversible 3*3 gate that maps the inputs (A, B, C) to the outputs (P=A, Q=A'B^AC, R=A'C^AB).This gate has a Quantum cost of 5 and is as shown in Fig 6.



kin Gate

2.7 TSG Gate

The TSG gate is a reversible 4*4 gate that has mapping inputs (A,B,C,D) to the outputs (P=A,Q=A'C'^B', R=(A'C'^B')^D, S=(A'C'^B')C^(AB^D)). This gate has a quantum cost of 13 and is as shown in Fig 7.

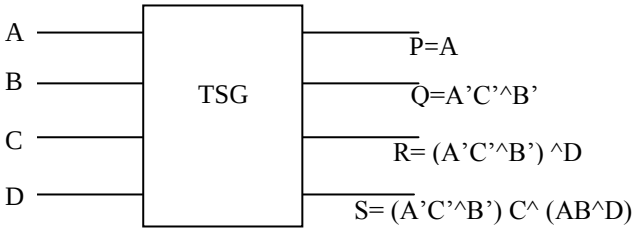


Fig.7: TSG Gate

2.8 Double Peres Gate

The Double Peres Gate(DPG) gate is a reversible 4*4 gate that has mapping inputs (A,B,C,D) to the outputs(P=A,Q=A^B,R=A^B^D,S=(A^B)D^AB^).This gate has a quantum cost of 8 and is as shown in Fig 8.

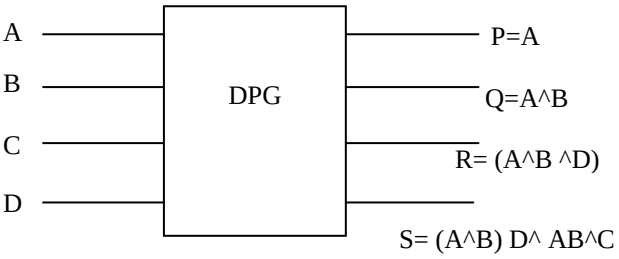


Fig.8: Double Peres Gate

3. EXISTING METHOD

In the existing method, a Carry Skip BCD adder was implemented using Feynman ,Toffoli , Peres and MRFGgates. The block diagram consists of a MUX, Carry Propagation Block and a Correction Block and is shown as Fig 9[1].

Here, the full adder is realized using Toffoli (TG) and Feynman (FG) Gates where the TG gate has a Quantum Cost of 5 and the FG gate has a Quantum Cost of 1. In this implementation, a reversible full adder is implemented using two TG gates and two FG gates. So each full adder consists of four gates and its Quantum Cost amounts to 12. Fig 10 shows the full adder circuit.

For multiplexer block we modify the Frekdin gate. Here input A works as a selection input and B and C as mux inputs to be selected by A. When A=0 the thirdoutput is C and when A=1 the third output is B. Thus this block performs the function of a multiplexer. The quantum cost of modified FRG gate is 4 and it produces 2 garbage outputs. Fig 11 shows the MUX block.

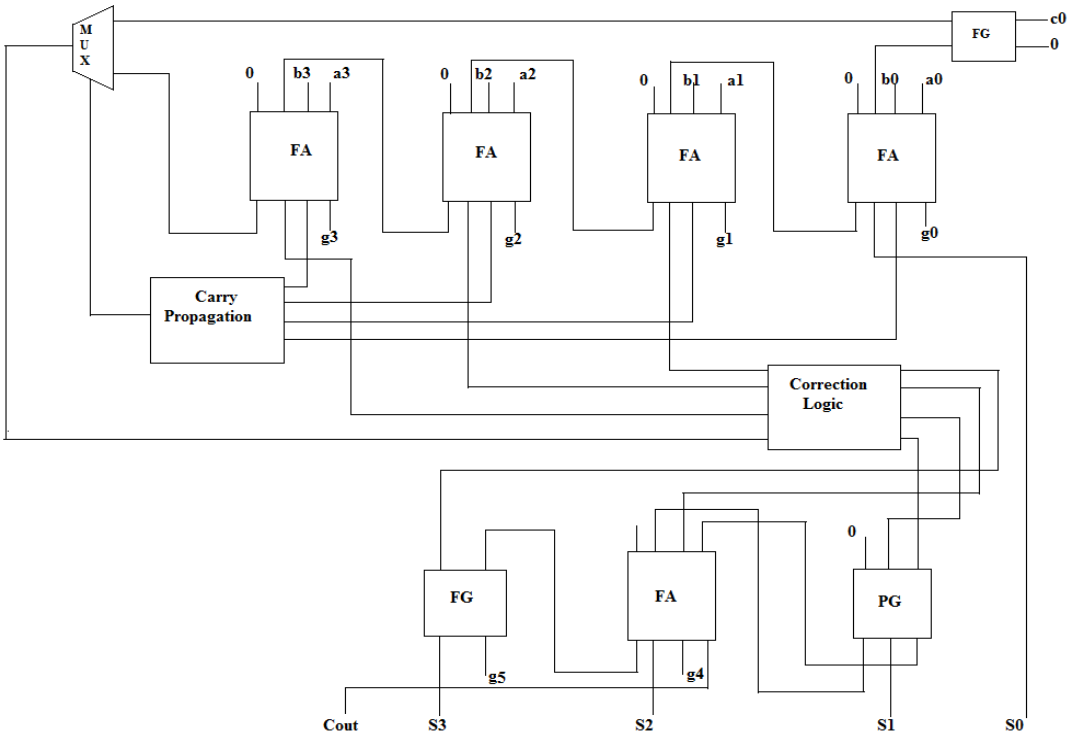


Fig.9: Carry Skip BCD Adder Using A Combination Of TG And FG Gates As Full Adder

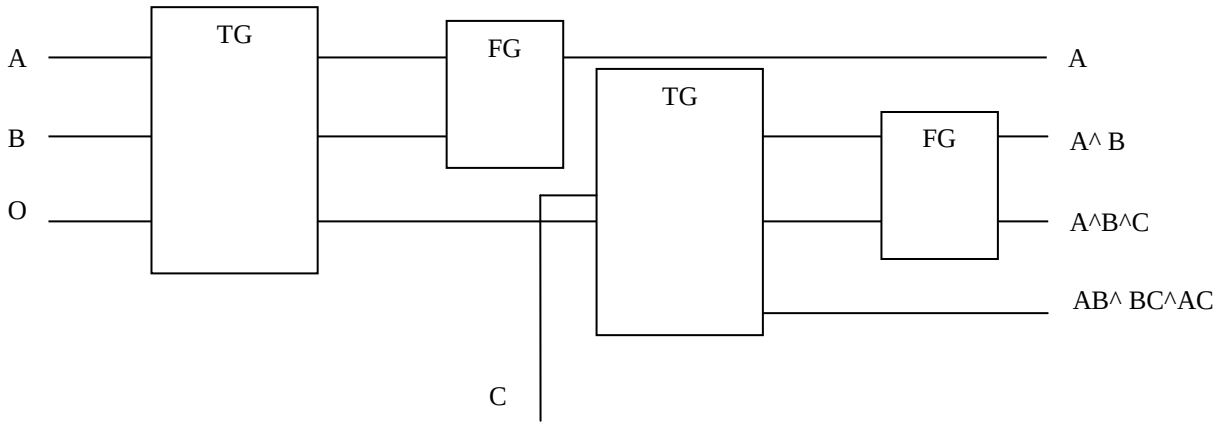


Fig.10:Full Adder

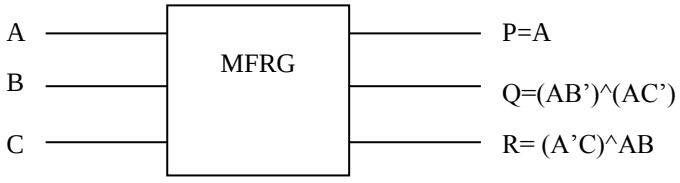


Fig.11: MUX Block

Carry propagation block receives 4 inputs P0,P1,P2 and P3 and we have to generateP0P1P2P3. It can be realized by three Peres gates. Since the Quantum Cost of Peres gate is 4, the Quantum Cost of the carry propagation block is 12. This block is shown as Fig 12.

The Correction logic block is realized using two FG gates and one TG gate. This block receives carry C4and three sum terms S1, S2 and S3as inputs. The required logic for the correction block is S1 (S2^S3)^D. This block has a Quantum Cost of 7and is as shown in Fig 13. All these blocks are used in Fig 9[1].

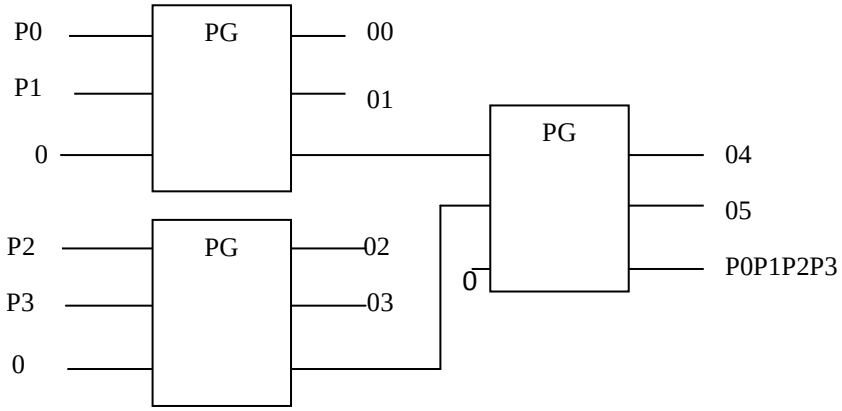


Fig.12: Carry Propagation Block

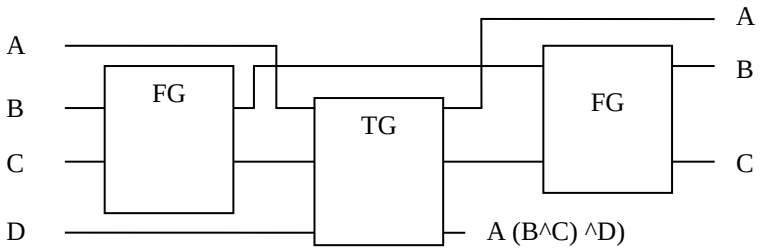


Fig.13: Correction Logic Block

4. PROPOSED METHOD

In the proposed method, a reversible Carry Skip BCD adder has been realized in which a Double Peres Gate (DPG) is used as a full adder. A DPG can be used singly as a full adder circuit and is used in place of the full adder circuit realized using a combination of FG and TG gates in the existing circuit.This gate can work singly as a reversible full adder circuit when its fourth input is set to zero (D=0) and it has a Quantum Cost of 8.The DPG gate is as shown in Fig 14. This Carry Skip BCD adder circuit consists of the same three blocks namely MUX, Carry Propagation and Correction Logic blocks. These blocks are also implemented similar to that used in the existing method. The Carry Skip BCD adder circuit using DPG as full adder is as shown in Fig 15.

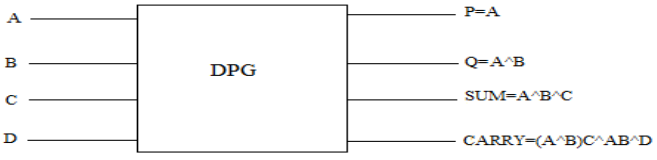


Fig.14: DPG Gate

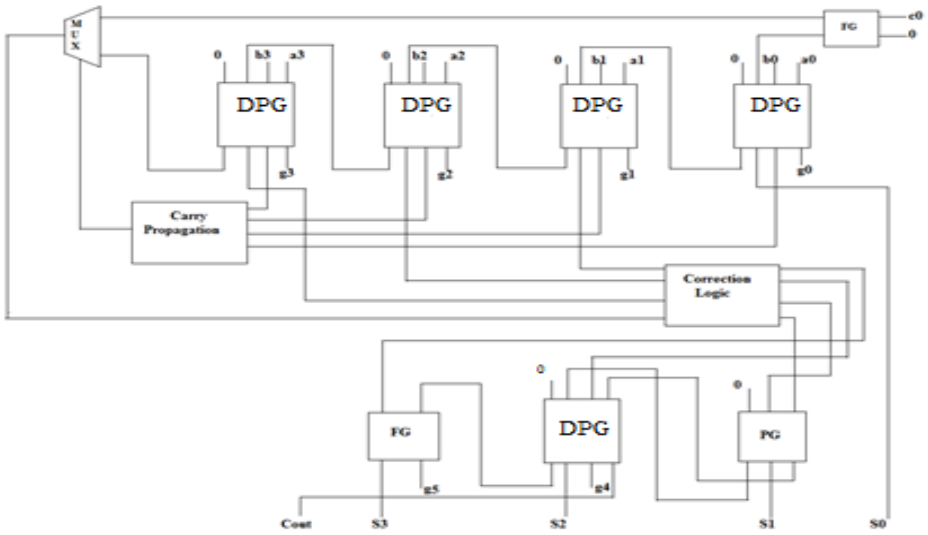


Fig.15: Proposed Carry Skip BCD Adder

5. RESULTS AND OBSERVATIONS

Fig 16 and Fig 17 show the waveforms obtained for both Existing and Proposed Method.

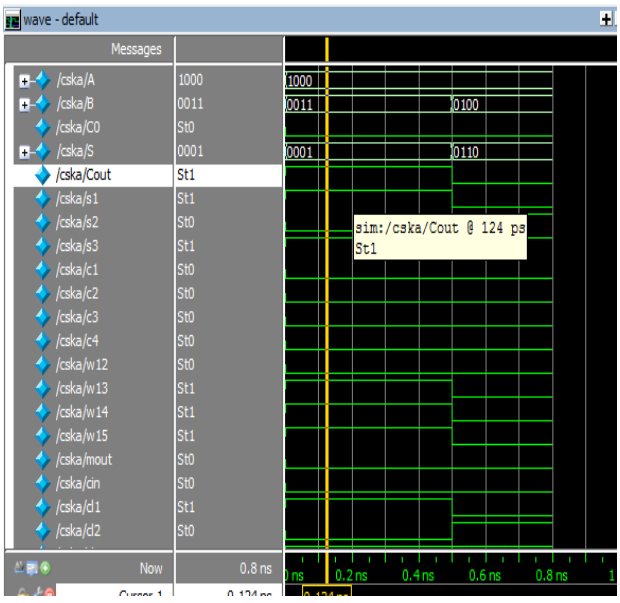


Fig.16: Waveform for Existing Method

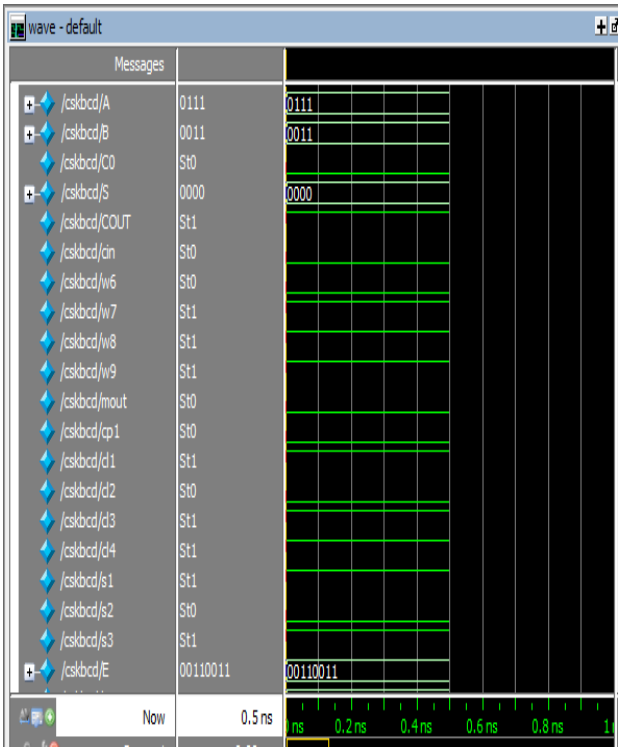


Fig.17: Waveform for Proposed Method

The following table shows a comparison between the existing method and proposed method in terms of the number of gates used and their garbage outputs.

Table 1. Comparison between the Existing and Proposed methods

Carry Skip BCD Adder	Number of Gates used	Number of Garbage outputs
Proposed Method	15	14
Existing Method	30	14

From the above table, it can be seen that in the Proposed Carry Skip BCD Adder only 15 gates are used which is the exact half of that used in the Existing method.

6. CONCLUSION AND FUTURE WORK

Thus the Proposed method was designed and was found to be more efficient than the Existing method in terms of the number of gates used in the circuit. The Proposed method can be used to realize more complex circuits

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