Analyzing the Impact of Stacking Power Gating Technique on Ground Bounce Noise Effect of 3-Bit Flash Analog to Digital Converter

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ABSTRACT
In present scenario high speed and low power devices in signal processing system is generally needed the efficient design and reduced complexity of converters, therefore conventional flash ADC is not fully meet the required specifications.ADC with high speed and low resolution is required in present communication technologies. Lower leakage current with low power consumption is considerable effect for different parameter optimization of flash ADC. The approach for reducing the leakage current is stacking power gating technique in three modes sleep, active and sleep-to-active modes. The design circuit has been simulated using cadence virtuoso tool with 45nm CMOS technology at various supply voltages. Ground bounce noise reduction has been done in flash ADC with stacking power gating approach to reduce the leakage current and active power.

Keywords
Flash ADC, Ground bounce noise, Stacking power gating, Active power, Leakage current.

1. INTRODUCTION
ADC is the most popular components used in every consumer electronics and computer systems as there rapid incline of electronics system design including communications and signal processing based systems. Flash ADC is mostly used in high speed and low power application [1]–[4] In recent years system–on-chip grows rapidly therefore signal processing component optimization is an important factor. Analog to digital converters (ADCs) is a mixed signal integrated component that converts analog signals to digital signal; which are the real world signals that has been used for information processing component. Design of high speed, low operating voltage, low power consumption and the high input signal bandwidth analog-to-digital converter demand increasing rapidly [5]-[9]. Comparators are the important component of any flash ADC and performance. ADC is strictly depended on comparators .Area, speed and power consumption of computational intensive VLSI systems are contributed and well implemented by flash ADC. Low power and high speed flash ADC is in high demand [10]. Technology is defined by making device size smaller one, so it has become difficult to achieve a good tradeoff by device scaling or sizing of the transistors [11]. Gate leakage increases 30 times with new technology [12]. Reducing the leakage, improved design techniques are important. Sleep transistor is connected between the actual ground and circuit ground in the power gating technique [12]- [13]. To cut the leakage path the sleep mode of this transistor was off. Power gating technique reduces the leakage with minimal impact on the performance of circuit [14] Other power gating techniques are Multi-threshold CMOS (MTCMOS) [15] and Transistor Gating [16].These all reduce leakage current and ground bounce noise. Focus of this paper is reducing sub-threshold leakage power and ground bounce noise, with the help of a stacking power gating technique.

2. PROPOSED DEVICE ARCHITECTURE

2.1 Flash ADC
Figure 1 shows block diagram of conventional flash ADC that has been implemented using cadence virtuoso tool with 45 nm technology. A 3 bit flash converter has been designed and investigated in this work. Flash"3 bit converter, simply require 2^3-1= 7 comparators. A resistive divider that incorporated in converter employs 2^3 = 8 resistors for providing the reference voltage in the comparators or converters. Resistive divider provides the reference voltage to each comparator become one LSB (least significant bit) that means it is higher than the reference voltage for the comparator just below the previous one . Each comparator achieves the output "1" whenever input voltage source (analog) Vin is higher than the reference voltage Vref provided for comparators .The comparator give output "0"when analog input source becomes lower than reference voltage applied to it.

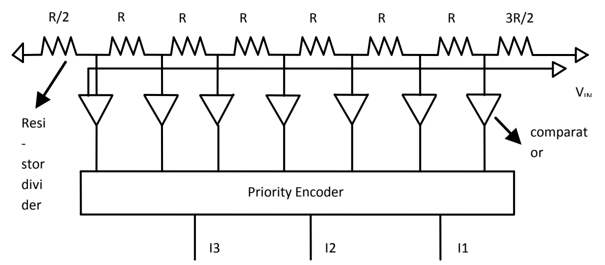

Figure .1 Conventional flash ADC architecture [17]

Each resistor in divider section divides the reference voltage that is applied in upper extreme resistor to feed a comparator. Each comparator achieved the output "1" whenever input voltage source (analog) Vin is higher than the reference voltage Vref provided for comparators. The output of the comparators is not in digital form but there is need to achieve encoded signal, therefore a priority encoder is employed to convert the encoded signal into digital form means "n" bit data format generated in binary code format. Current consumption by the device becomes lower whenever the resistance value getting higher which minimized the power dissipation in the device .Flash ADC "n" bit architecture provides 2^n-1 comparators that consist of differential amplifier based.

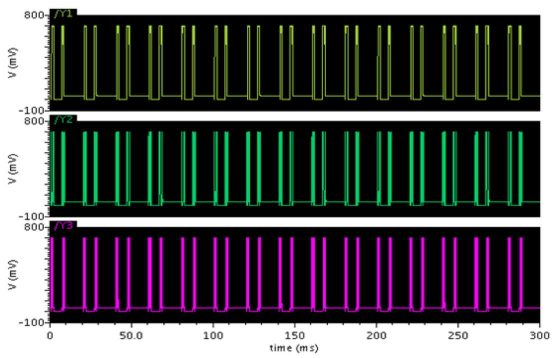

Figure. 2Transient behaviour of flash ADC

Figure 2 shows the Flash ADC transient output analysis of "3" bit flash ADC for analog input signal VSIN of 5000 Hz frequency. Bit "0" represent the LSB and bit "2" represent the MSB of the binary digital output of "3" bit flash ADC.

2.2 Comparator

Comparator is important component of analog-to-digital converter that plays the important role to achieve overall good performance. . It is used in front-end signal processing and electronics components [18] Lowering the input impedance is effective to improve the better performance of comparator [19]-[22].Inverter based comparator is reducing the offset error [23]-[24]. Whenever input voltage is just close to reference voltage then it may be high possibility that noise can make the variation of input voltage around reference voltage. This noise can generated output glitches that consume lot of power and provide higher leakage whenever circuit is in standby mode therefore there is need to design a comparator

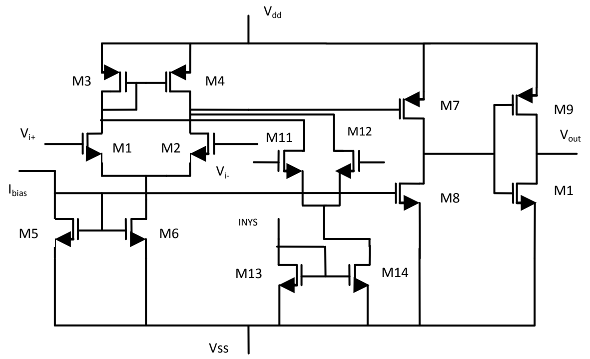

Figure . 3 Schematic of comparator

with hysteresis effect to minimize the noise problem and reducing the leakage power.

3. STACKING POWER GATING TECHNIQUE

Stacking power gating technique is the effective way to reduce ground bounce noise greatly. There are two modes that generally describe in stacking power gating technique include the leakage current reduction by stacking mode and reduction of ground bounce noise by simply vary and controlling the intermediate node voltage .

3.1 Leakage current reduction

Stacking power gating technique is generally used to reduce the leakage current by stacking effect where both ST1and ST2 sleep transistors are in OFF condition. Peak current and voltage glitches power rails i.e. ground bounce noise are important factor that effect performance of circuit therefore Stacking sleep transistors are used in this technique for reduction the magnitude of peak current and voltage glitches power to enhance the performance. In stacking power gating technique the leakage current is reduced by the stacking effect, where both ST1and ST2 sleep transistors are in OFF condition.

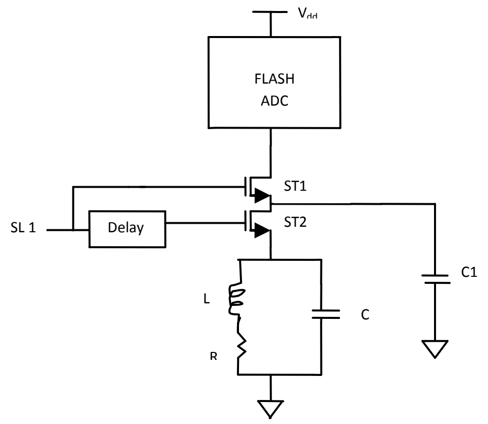

Figure. 4 Flash ADC with stacking power gating technique.

Stacking power gating technique describes three modes of operation:

3.1.1. *Active Mode*

The sleep transistor remains at logic '1' in active mode where both the sleep transistors ST1and ST2 are staying in ON condition. In this situation both transistors having low resistance and virtual ground node potential is maintained equal to ground potential, making the logical difference in circuit effectively that becomes equal to the supply voltage.

Voltage across C1 = VC1 (active mode) = V (R1ON) + V (R2ON)

Voltage across C2 = VC2 (active mode) = V (R2ON) = 0V

3.1.2. *Standby Mode*

Both the sleep transistor's ST1 & ST2 are OFF in standby mode and both offers high resistance. Capacitance C1 charges up-to voltage V1 and the capacitor C2 charges up-to voltage V2 during standby mode

So, VC1 (standby mode) = V1
VC2 (standby mode) = V2

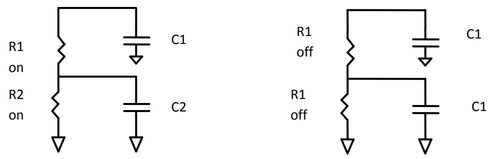

Figure.5 and 6 Equivalent circuit of sleep transistor ST1 and ST2 in active mode and standby mode

3.1.3. *Sleep to Active Mode transition*

Initially the transistor ST1 is turned ON and after some delay of very small duration of time transistor ST2 is turned ON to reduce the ground bounce noise considerably in sleep-to-active mode transition,. The parameters T1 and the capacitances C2 are kept to particular value that is based on following important factors:

- Minimum ground bounce noise
- Minimum leakage current

4. Simulation and Performance Characteristics

4.1. *Active power simulation*

The power is dissipated by the circuit at the time of the operation is known as active power. Active power contains both dynamic and static power. Active power of the circuit is calculated at different voltages for the 45nm technology. Active power also calculated by equation [25].

$$\mathbf{P_{act} = P_{dyna} + P_{stat}} \tag{1}$$

$$\mathbf{P_{act} = P_{swi} + P_{s-c} + P_{leak}} \tag{2}$$

$$= \left(\boldsymbol{\alpha_{0\to1}} \times \mathbf{C_{load}} \times \mathbf{V_{dd}^2} \times \mathbf{f_{clock}}\right) + (\mathbf{I_{s-c}} \times \mathbf{V_{dd}}) \quad (\mathbf{I_{leak}} + \mathbf{V_{dd}}) \tag{3}$$

Where,Pact=active power,Pdyna=dynamic power,Pstat=static power,Pswi=switching powr,Ps-c=short circuit power,Pleak=leakage power,Cl = capacitance at load, fclock = frequency at clock, α = switching activity, Is-c = current when circuit is short, Ileak = leakage current, Vdd = supply voltage. It is clear from the table that in case of flash ADC with stacking power gating technique active power calculated at the different voltages.

Table.1 Active power analysis at different voltages

Different voltages	**Active power(uw)**
0.9	50.63
0.7	46.85
0.5	46.14
0.3	45.44

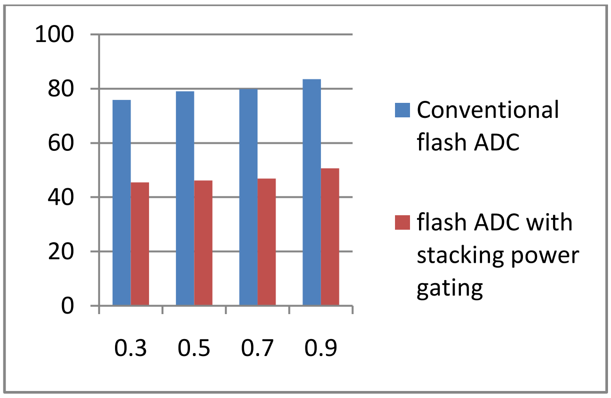

Figure.7 Active Power Dissipation of 3 bit flash ADC

Table 1 describes the active power at different operating voltages of the flash ADC .Figure 7 shows the comparison between conventional flash ADC and flash ADC with stacking power gating technique The leakage current and leakage power is reduced to 80% with stacking power gating technique that enhance the performance of flash ADC. Stacking power gating technique is used to reduce the active power. The active power is reduced up-to 20% in 45nm technology.

4.2. Leakage current simulation

Leakage current of the flash ADC is estimated during the standby mode. To estimate the leakage current of the flash ADC, NMOS transistor is required to measure the leakage current that is connected at the pull down network below the whole circuit. Sleep transistor is OFF for this technique whenever leakage current calculation is analyzed. Leakage current is derived and calculated by the equation given below [26].

$$\mathbf{I_{leak} = I_{sub-thr} + I_{gat-ox}} \qquad (4)$$

Where, Isub-threshold = sub-threshold leakage current, Igat-ox = gate-oxide leakage current.

$$\mathbf{I_{sub-threshold} = K_A W\, e^{\frac{-V_{th}}{nV_\theta}} (1 - e^{\frac{-V}{V_\theta}})} \qquad (5)$$

Where, KA and n are experimentally derived, W = gate width, Vth = threshold voltage, n = slope shape factor, VƟ = thermal voltage.

$$\mathbf{I_{gat-ox} = K_B\, W\, (\frac{V}{T_{ox}})^2\, e^{\frac{-\alpha T_{ox}}{V}}} \qquad (6)$$

Where, KB and α are experimentally derived, Tox = oxide thickness.

Table 2. Describe the leakage current analysis at different voltages

Different voltages(V)	Leakage current(pA)
0.9	18.54
0.7	16.83
0.5	16.06
0.3	11.63

Table 2 describes the leakage current at different operating voltages in the standby mode of the flash ADC .Figure 8 shows the comparison between conventional flash ADC and flash ADC with stacking power gating technique. The leakage current and leakage power is reduced to 80% with stacking power gating technique that enhance the performance of flash ADC.

4.3. Leakage power simulation

The leakage power of the circuit is measured during the standby mode. It explained that how several percentage of power is wasted by the whole circuit during off state condition whenever there is no supply. Leakage power is the product of the leakage current and supply voltage. The basic equation of leakage power is realized by Equation. (7) [25]

$$\mathbf{P_{leak} = I_{leak} \times V_{dd}} \qquad (7)$$

Where, Ileak = leakage current, Vdd = supply voltage.

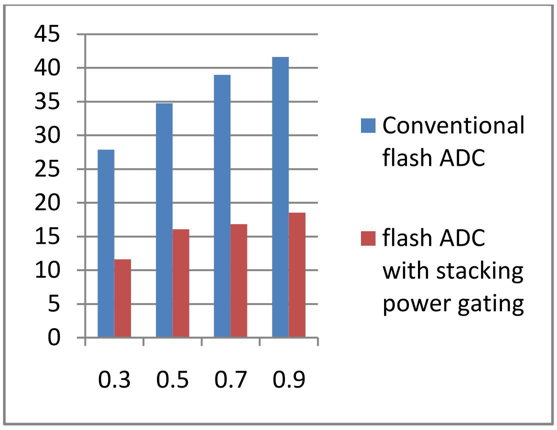

Figure.8 Leakage current of 3 bit flash ADC

4.4. Ground bounce noise reduction

Ground bounce noise can be controlled in stacking power gating technique by control the intermediate node .Some delay is provided to the ST2 transistor for controlling intermediate node voltage.In sleep to active mode transition ,sleep transistor ST1 is turned ON initially and after few delay sleep transistor ST2 is turned ON therefore the ground bounce noise occurs twice in sleep to active mode transition when ST1 is turned ON and then ST2 is turned ON. Peak of the ground bounce noise is dependent on the voltages whenever capacitors C1 an C2 are discharging ,while ST1 and ST2 transistors are turned ON respectively.

The amount of voltage discharged by the capacitor C2 is expressed as

$$\mathbf{V_{c1}(Discharge) = V_{c1}(0) - V_{c1}(min\ delay)}$$
(8)

The amount of voltage discharged by the capacitor C2 is less than the capacitor C1

$$\mathbf{V_{c1}(Discharge) > V_{c2}(Discharge)}$$
(9)

The peak of ground bounce noise when ST1 transistor is turned on at the first time is high and the peak of ground bounce noise when ST2 transistor is turned on at the second time

Minimum ground bounce noise condition is expressed as:

$$\mathbf{V_{c1}(Discharge) = V_{c2}(Discharge)}$$
(10)

Figure 9 describes the ground bounce noise effect with stacking power gating technique of flash ADC. Signal to noise ratio (SNR) [27] can be calculated with the help of peak amplitude of signal and noise . Ground bounce noise is shown in figure 9 and SNR can be calculated by given equation.

$$\mathbf{SNR = 20\log_{10}(\frac{A_{signal}}{A_{noise}})dB}$$
(11)

Where Asignal and Anoise is the peak amplitude of signal and noise.

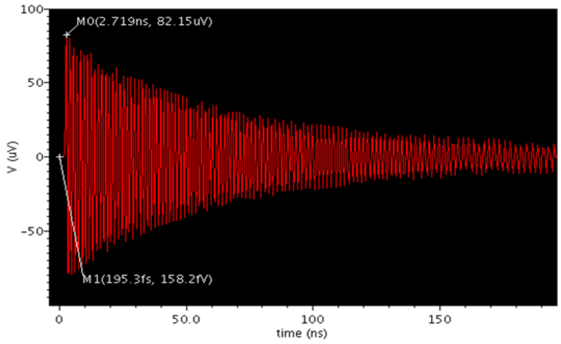

Figure .9 Showing ground bounce nosie of flash ADC.

Table 4. Performance comparison of conventional flash ADC and flash ADC with stacking power gating technique

	Conventional flash ADC	**Flash ADC with diode based stacking power gating technique**
SNHR	5.817 dB	106.2 dB
SFDR	5.967 dB	8.145 dB
SNR	56.36 dB	78.60 dB
ENOB	3.45-bit	0.56 –bit

Table 4 describes the diode based stacking power gating technique effect on the performance of conventional flash ADC. It clearly indicates that diode based power gating technique improve the performance of ADC that degrade due to the ground bounce noise effect.

5. Conclusion

In this paper “3” bit flash ADC for signal processing and communication systems with low ground bounce noise is described here. Stacking power gating technique is used to reduce different parameters that are active power, leakage current, leakage power and ground bounce noise. Reduction of the leakage current is achived in standby mode and ground bounce noise in sleep-to-active mode transition. In stacking power gating technique, ground bounce noise is controlled by using a stacked sleep transistors with delayed signal. The leakage current and leakage power is reduced to 80% with stacking power gating technique that enhance the performance of flash ADC. The active power is reduced up-to 20% in 45nm technology. Ground bounce noise is reduced nearly 50% with stacking effect. The flash ADC is operated at various voltages.

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