# Low Leakage Multi Threshold Level Shifter Design using Sleepy Keeper

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## ABSTRACT
In this paper, a low leakage multi $V_{th}$ level shifter is designed for robust voltage shifting from sub threshold to above threshold domain using MTCMOS technique and sleepy keeper. Multi Threshold CMOS is an effective circuit level technique that improves the performance and design by utilizing both low and high threshold voltage transistors. Power dissipation has become an overriding concern for VLSI circuit designers. In this a "sleepy keeper" approach is preferred which reduces the leakage current while saving exact logic state. New low-power level shifter using sleepy keeper is compared with the previous work for different values of the lower supply voltage. The circuits are individually analyzed for power consumption at 45nm CMOS technology, new level shifter offer significant power savings up to 37% as compared to the previous work. On the other hand, when the circuits are individually analyzed for minimum propagation delay, speed is enhanced by up to 48% with our approach to the circuit. All these simulation results are based on 45nm CMOS technology and simulated in cadence tool.

## Keywords
Level shifter(LS), Multi threshold CMOS, Sleepy Keeper

## 1. INTRODUCTION

Deviation from constant field scaling due to the non-scaling parameters of the MOS transistors (thermal voltage, silicon energy band gap, and source/drain doping levels) leads to an increase in the power consumption and power density with each new technology[1],[3]. The increased power dissipation degrades the reliability, increase the cost of the packaging and cooling system, and lower the battery lifetime in portable electronic device.

The multi-supply voltage domain technique [3], based on partitioning the design into separate voltage domains (or voltage islands) with each domain operating at a proper power supply voltage level is preferred depending on its timing requirement. Time-critical domain run at higher power supply voltage ($V_{DDH}$) to enhance the performance, whereas noncritical sections work at lower power supply voltage ($V_{DDL}$) to enhance power efficiency. Power consumption is the top concerns of VLSI circuit design. To solve this power dissipation problem, many researchers have proposed ideas differing from the device level to the architectural level and above.

However, there is no universal way to avoid tradeoffs between delay ,power, and area, and thus, designers are in demand to choose appropriate techniques that satisfy application and product needs.

Power consumption of CMOS consists of dynamic and static components. Dynamic power consumption is when transistors are switching and static power consumption is regardless of transistor switching. One of the main reasons causing the increase in leakage power is the increase of subthreshold leakage power. When technology scales down, supply voltage also scales down simultaneously. The Sub threshold leakage power increases exponentially as threshold voltage decreases.

To down-convert from a higher voltage (within the oxide breakdown limits) to a lower voltage domain, CMOS inverters are usually adequate [4]. On the other hand, more complex LS topologies are required to up-convert signals from the lower to the higher power supply domain [5]. This issue is particularly compounded when the $V_{DDL}$ is lowered below the transistor's threshold voltage. In fact, in such a case, balancing the input section driving capability of the LS with sections of the circuit working at the $V_{DDH}$ voltage level requires proper design techniques [4]. In standby mode sleep transistors are used as switches to shut off power supplies to parts of a design. A sleep transistor is referred to either a PMOS or NMOS high $V_{TH}$ transistor that connects permanent power supply to circuit power supply. The sleep transistor is managed effectively by a power management unit to switch on and off power supply to the circuit. Sleep transistor PMOS is used to switch $V_{DD}$ supply.

This paper deals with a novel low-power LS designed to convert near-threshold or sub-threshold voltages to above threshold voltage levels with reduced power dissipations. When implemented with the 45-nm CMOS technology, the new design successfully converts input voltages as low as 0.7V to the 2V nominal output voltage, with a delay of 74.52 ps and consuming only 14.99 µW of static power.

The remainder of the paper is organized as follows. Section II provides a brief review of existing LS circuit. Our approach to level shifting and power reduction in circuit is presented in Section 3 and Section 4 discusses and evaluates obtained results. Finally, in Section 5 conclusions are drawn.

## 2. RELATED WORK

The conventional LS was differential cascade voltage switch circuit, as shown in Figure 1. It consists of two PMOS transistors (P2 and P3) working in a half latched form. A differential low input voltage signal in the form of D and DN is applied to the pair of transistors N2 and N3. When a low to high transistion is applied at the input segment D transistor N2 is turned ON leading P3 to turn ON. Once P3 is turned ON the node NL starts charging. Thus the positive feedback accelerates the voltage level conversion.

As a consequence, pull-up and pull-down strengths need to be properly balanced to assure correct functionality. This requirement is difficult to achieve in practice when input signals have sub-threshold voltage levels [4].

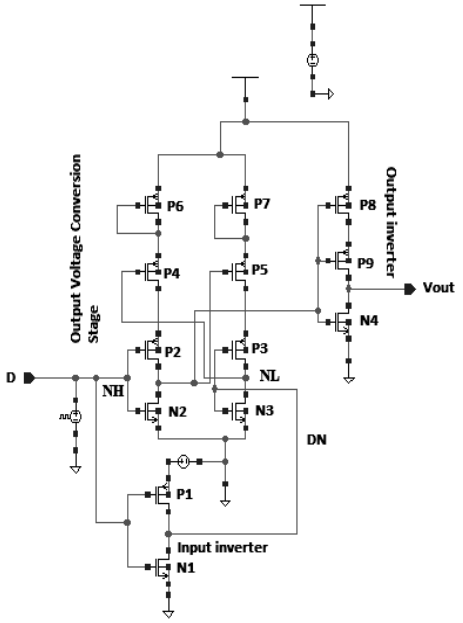


**Figure 1: Conventional Level Shifter**

Lutkeimer et al. [10] presented a new subthreshold to above-threshold level shifter circuit based on a Wilson current mirror. The circuit does not have a static current path between the supply and therefore offers a reduced static power dissipation. The simulation results of the level shifter in a 90-nm process technology show that this circuit topology offers good performance and low power dissipation. In this respect, the level shifter behaves similar to traditional CMOS logic gates in subthreshold.

S. N. Wooters et al. [7] demonstrated a subthreshold level converter that is fabricated in a 130-nm process. The level converter successfully and reliably upconverts to 1.2 V a signal generated by a supply voltage ranging between 188 mV and 1.2 V, making it suitable for both subthreshold and DVS operation.

A.Chavan et al. [8] evaluated in the context of translating signals from subthreshold levels to traditional CMOS levels. Three conventional circuits were included in the evaluation as well as three novel level shifters proposed for the first time. All six circuits were evaluated in terms of power, performance and radiation hardness for a constant area.

Solaeman et al. [11] discussed two novel subthreshold logic families. A new control circuit for the stabilization of subthreshold circuit is also discussed. Both VT-sub-CMOS and sub-DTMOS logic families show superior robustness and tolerance to temperature and process variations than that of regular subthreshold CMOS logic. VT-sub-CMOS logic can be readily implemented in twin-well process technology, but it requires additional circuitry for stabilization.

Marco Lanuzza et.al [1] briefly described the differences between the new architecture and the conventional DCVS. A high to low transition of the main input causes P4 to turned ON and causes P6 device into the saturation region. This creates a voltage drop (i.e., $V_{TH}$, P6) across P6 terminals that produce a correspondent bulk source voltage drop on P4. The reduced voltage level on the source terminal of P4 limits its $V_{GS}$, and also weakens the P4 action. All the above effects reduce the disputation on the node NH, thus allowing faster discharging to be achieved. When P4 is turned ON, P5 is therefore turned OFF. In this case, the small leakage current flowing through P5 is not enough to turn P7 ON. For this, P5 results power gated from the $V_{DDH}$ power rail, leading to a significant reduction in its sub-threshold current. The diode-connected P7 device minimizes the leakage current, also by increasing the threshold voltage of P5. In fact, P7 causes the source of transistor M5 to be at lower voltage than the bulk node and thereby reduces the sub-threshold leakage current due to the bulk effect.

The above described circuit differs from those adopted in other LS designs that use diode-connected transistors [7]. Since P6 limits the output range of the main conversion stage to [0V, $V_{DDH} - V_{TH}$], an output inverter is connected to node NH, to assure a rail-to-rail conversion. The pull-down of such an inverter uses svt (standard threshold voltage) device, whereas its pull-up is designed by using an hvt (high threshold voltage) PMOS transistors stack, thus limiting the leakage current flowing through the pull-up network of the output inverter, when NH is high. Opposite and considerable threshold voltage variations on P6 and P8-P9 can cause the latter transistors to go in weak inversion, thus increasing the static power dissipation.

# 3. LS USING SLEEPY KEEPER

The new multi $V_{TH}$ level shifter is described in this section. This level shifter uses a multi $V_{TH}$ CMOS technology in order to eliminate static dc current. As shown in Figure 2., the circuit consists of an input inverter, a main voltage conversion stage, an output inverting buffer and sleepy keeper. To increase the strength of the pull-down network of the main voltage conversion stage, it was also designed by using 1V transistors [1]. The current flowing through the nodes NH and NL at the beginning of their high to low transition could be of concern. Thus, to reduce this effect, two PMOS devices (MP2 and MP3) are adopted. MP4 and MP5 helped in weakening the pull-up networks of the main voltage conversion stage, thus reducing conflict NH and NL nodes. This choice also reduced the leakage current flowing through the pull-up networks when they are turned OFF. Finally, to acheive reliable voltage conversion, two diode-connected PMOS devices (MP6 and MP7) were placed between the pull-up logics and the supply rail $V_{DDH}$. These devices limit the pull-up strength, but also reduces static power. This section briefly describe the working of the circuit. A high to low transition of the main input causes MP4 being turned ON. Its drain current brings the diode-connected MP6 device into the saturation region.

This creates a voltage drop across MP6 terminal that produce a bulk source voltage drop on MP4. Due to this bulk effect, there is increase in the MP4 threshold voltage and the reduced voltage level ($V_{DDH}$-$V_{TH}$, MP6) on the source terminal of MP4 limits its $V_{GS}$, thus further weakening the MP4 action. When MP4 is turned ON, MP5 is therefore turned off. In this case, the small leakage current flowing through MP5 is not enough to turn MP7 ON. For this reason, MP5 results power gated from the $V_{DDH}$ power rail, leading to a significant reduction in its sub-threshold current.

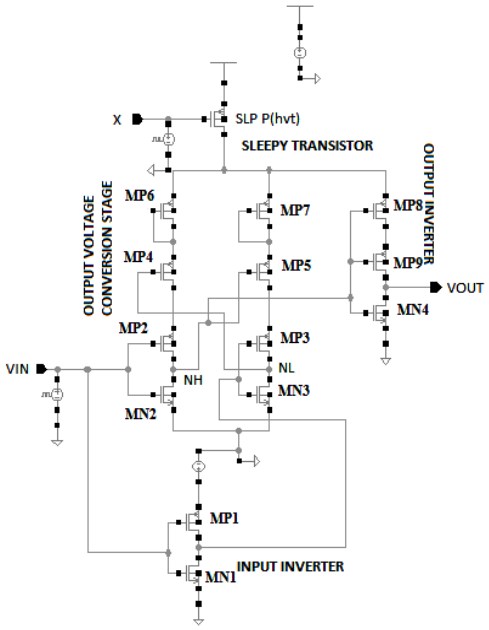


**Figure 2: Level Shifter Design**

The diode-connected MP7 device minimizes the leakage current, also by increasing the threshold voltage of MP5. In fact, MP7 causes the source of transistor MP5 to be at lower voltage than the bulk node and thereby reduces the sub-threshold leakage current due to the bulk effect. This significantly differs from those adopted in other LS designs that implemented diode connected transistors [7]. Since MP6 limits the output range of the main conversion stage to [0 V, $V_{DDH} - V_{TP}$], an output inverter is connected to node NH, to assure a required conversion. The pull-down of such an inverter uses a MP8, MP9 and MN5 device, whereas its pull-up is designed by exploiting PMOS transistors stack, thus limiting the leakage current flowing through the pull-up network of the output inverter, when NH is high. Opposite and substantial threshold voltage variations on MP6 and MP8-MP9 could, cause the latter transistors to go in weak inversion, thus increasing the static power dissipation. Now sleepy transistor is placed in series with MP6, MP7, MP8 and power supply. A sleep control scheme is used for efficient power management. In the active mode, X is set low and SLP P(hvt) is turned ON. Since their on-resistances is small, the supply voltage almost function as real power line. In the standby mode, X is set high, SLP P(hvt) turned OFF and decreasing the power dissipation.

## 4. RESULTS AND ANALYSIS

In this section, the new level shifter is compared to the conventional level shifter for average power consumption and propagation delay. The available gaps in the propagation delay paths, the power consumption and delay overhead of the level shifter, the availability of high efficiency power supplies, and the availability of a multi-$V_{TH}$ CMOS technology are the important factors affecting the optimum supply voltages in a Multi-$V_{DD}$ system. A wide range of lower supply voltages is considered in this paper since the factors vary with the technology and the application at prelayout and postlayout values . The simulations are carried out for the following values of VDDL: 0.7V, 0.8V and 1V for conventional level shifter and then for same voltages LS using sleepy keeper is verified at prelayout and postlayout levels. Desired and far better results are obtained using LS with sleepy keeper than conventional Level shifter. The results are listed in Table I. It is observed that our approach gave far better results.

**Table I - Performance chararterstics and comparisons**

| Circuits | Voltage | Results | Dynamic power (Watt) | Propagation delay (Sec) | Power delay product (Joule) |
|---|---|---|---|---|---|
| Conventional LS | 0.7 V | Pre layout | 38.64E-6 | 80.52E-12 | 3.11E-15 |
| | 0.8 V | Pre layout | 44.87E-6 | 52.66E-12 | 2.36E-15 |
| | 1 V | Pre layout | 53.95E-6 | 37.27E-12 | 2.01E-15 |
| LS using sleepy Keeper | 0.7 V | Pre layout | 14.99E-6 | 74.52E-12 | 1.117E-15 |
| | | Post layout | 15.05E-6 | 163.5E-12 | 2.460E-15 |
| | 0.8 V | Pre layout | 26.61E-6 | 42.03E-12 | 1.180E-15 |
| | | Post layout | 26.64E-6 | 83.84E-12 | 2.230E-15 |
| | 1 V | Pre layout | 38.21E-6 | 33.38E-12 | 1.276E-15 |
| | | Post layout | 38.26E-6 | 51.58E-12 | 1.970E-15 |

Figure 3. depicts the layout drawn for the designed schematic of level shifter. In this power supplies are available through the top and the middle metal-1 rails, while a shared ground rail travels at the bottom of the cell. Signals routing have been realized using only metal layers 1 and 2, thereby keeping the other metal layers available for interconnections on higher abstraction levels. The obtained layout dimensions are 4.46 µm × 6.76 µm. Postlayout verifications are also done for the schematic and the obtained results are verified with prelayout simulation. Respective delay minimizations and reduction in power consumtion required is achieved as shown in table I.

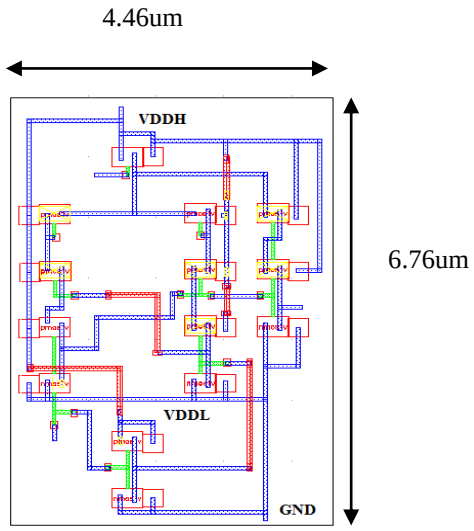


**Figure 3: Layout of Level Shifter Design**

Level Shifter has been made to operate on 0.7V. It has been observed that level shifter upconverts the output voltage level to 2V.The transient analysis Figure 4. is shown and dynamic power graph Figure 5. is analysed at 0.7 V using cadence virtuoso. It has been observed that PDP is 64.30% improved in this design than conventional level shifter.

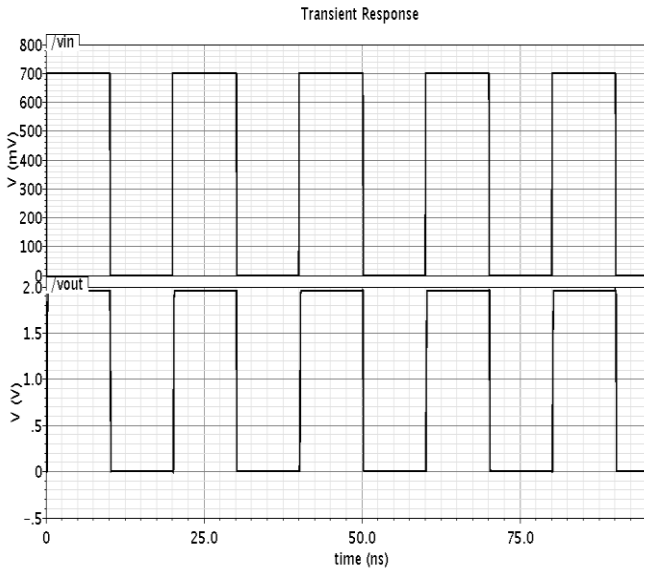


**Figure 4: Transient response at 0.7V**

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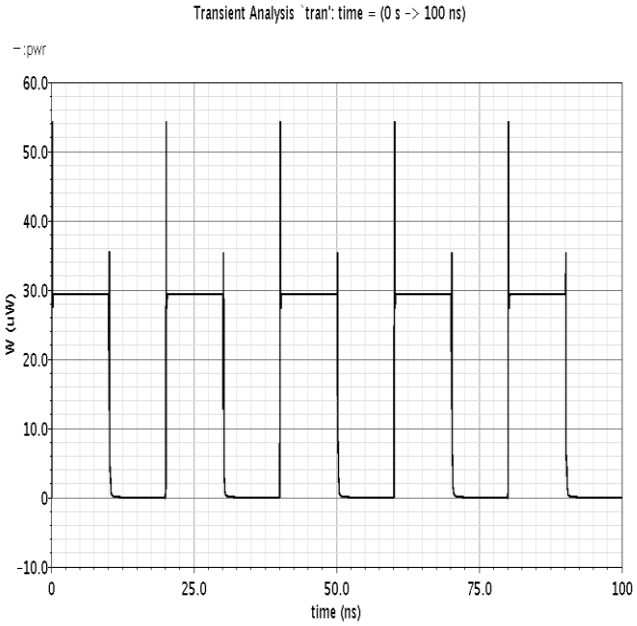


**Figure 5: Dynamic power at 0.7 V**

Level Shifter has been made to operate on 0.8V. It has been observed that level shifter upconverts the output voltage level to 2V.The transient analysis Figure 6. is shown and dynamic power graph Figure 7. is analysed at 0.8V using cadence virtuoso. It has been observed that PDP is 50% improved in this design than conventional level shifter.

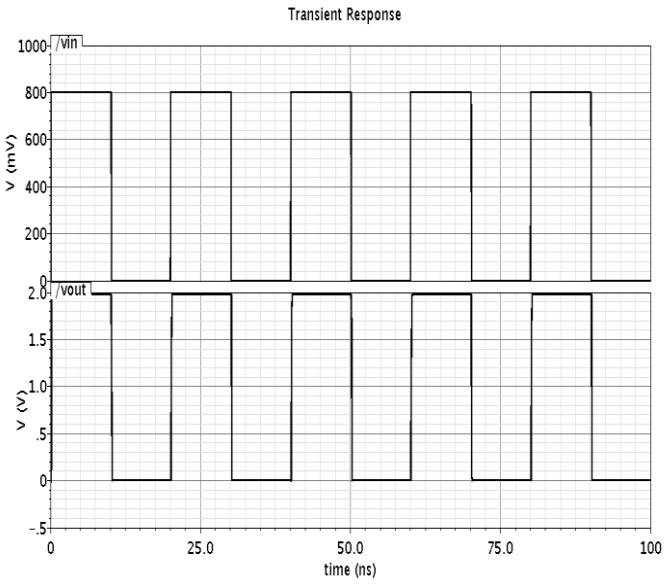


**Figure 6: Transient response at 0.8V**

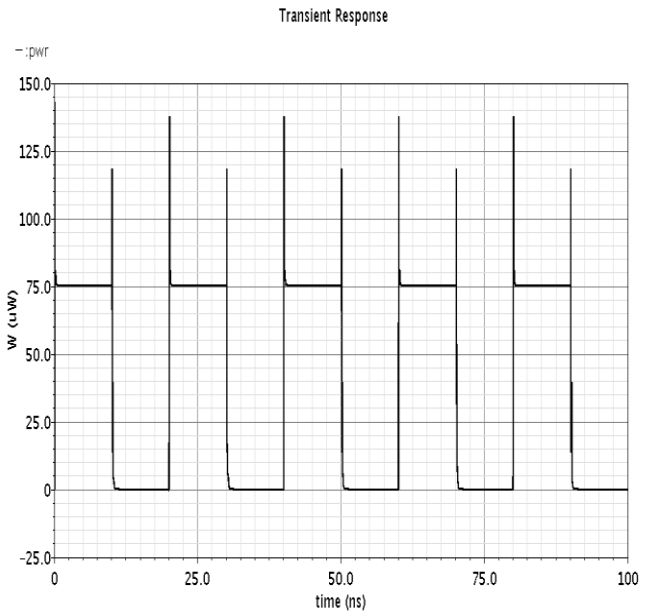


**Figure 7: Dynamic power at 0.8 V**

Level Shifter has been made to operate on 1V. It has been observed that level shifter upconverts the output voltage level to 2V.The transient analysis Figure 8. is shown and dynamic power graph Figure 9. is analysed at 1V using cadence virtuoso. It has been observed that PDP is 36.81% improved in this design than conventional level shifter.

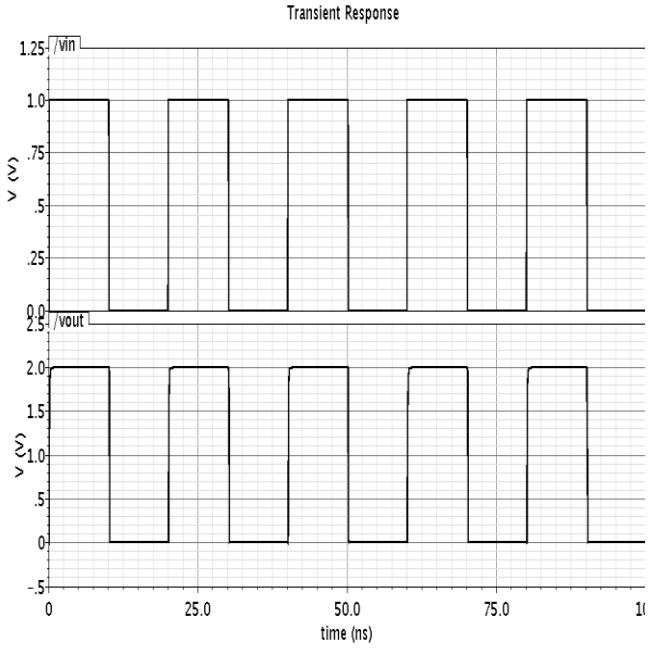


**Figure 8: Transient response at 1V**

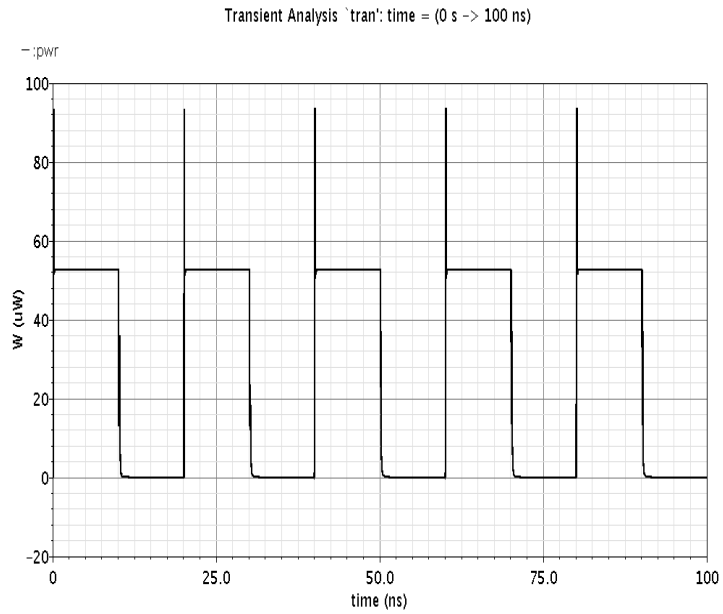


**Figure 9: Dynamic power at 0.8 V**

$V_{DDL}$ graph in different threshold regions is plotted at various frequencies and following characterstics are observed at different threshold regions.

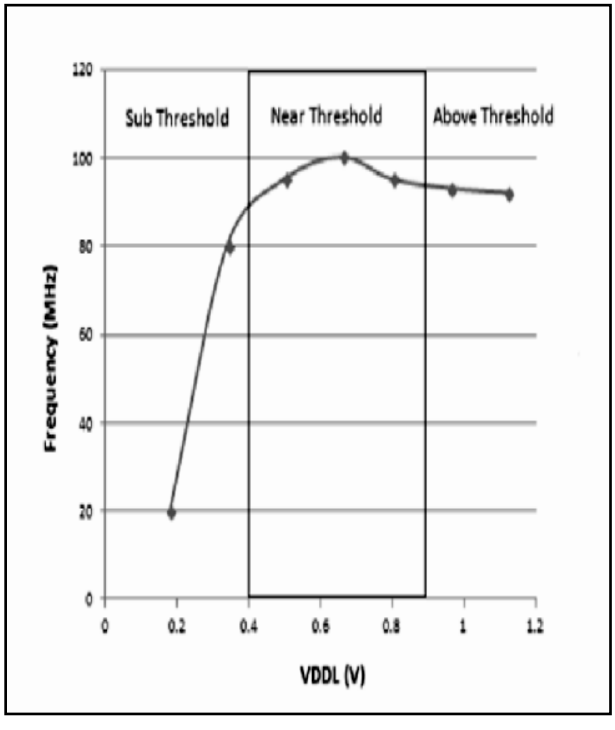


**Figure 10: Frequency Vs VDDL Graph in different threshold regions**

## 5. CONCLUSION

This paper has been presented a new low-power LS suitable for robust logic voltage shifting from near/sub-threshold to above threshold domain with reduced power dissipation.This circuit exploits proper design strategies to limit energy and static power consumption. When this circuit used for sub-threshold to above threshold voltage conversion, the new design exhibits the lowest static power and energy consumption with respect to previous proposed LSs that used similar design parameters. Moreover, even though the new designed LS is optimized for low power consumption, it also reaches high-speed performances and supports a wide voltage conversion range.

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