# Characterization of 6T SRAM Cell DRV for ULP Applications

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## ABSTRACT
This paper examines the characteristics of 6T SRAM Cell Data Retention Voltage (DRV). It also presents different DRV minimization techniques for ULP applications. The 6T SRAM cell is designed in 180nm CMOS technology. The cell is simulated to by varying different DRV dependent parameters to understand the effects on it.

## Keywords:
CMOS; SNM; DRV; CR; PR

## 1. INTRODUCTION
SRAM memory is massively used in VLSI systems; it is because of its inherent speed. ITRS 2009 quoted that the density of SRAM can go beyond 5 billion transistors / $cm^2$, by 2015. So to achieve this objective, the SRAM cells are designed having transistors of near minimum size, thus making it more vulnerable to process variations [7].
Stability is of great concern & issue for SRAM cell design. This stability defines how the memory is affected by process variation & operating conditions. The objective is to operate the memory correctly even if noise is present.

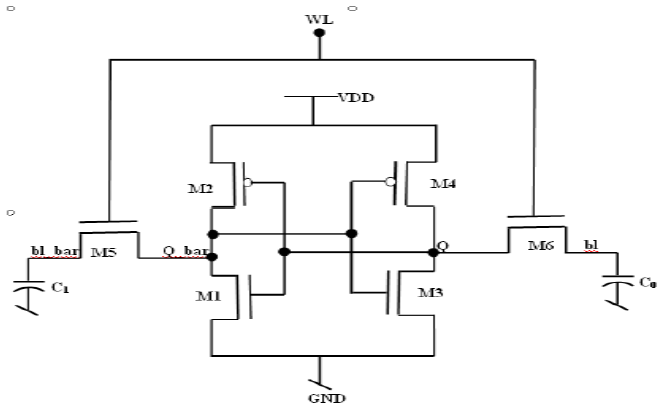



**Fig1. Six-transistor (6T) CMOS SRAM cell**

The measurement of stability of SRAM cell in the presence of DC noise is done by Static Noise Margin (SNM). SNM is the amount of voltage noise required to flip the state of the cell. It can be obtained from the voltage transfer characteristic (VTC) of the two cross coupled inverters of the SAM cell.

Figure 1 shows the schematic of a mainstream six transistors SRAM cell. It consists of six transistors. Four transistors (M1−M4) comprise cross-coupled CMOS inverters and two NMOS transistors M5 and m6 provide read and write access to the cell. Upon the activation of the word line, the access transistors connect the two internal nodes of the cell to the true (BL) and the complementary (BLB) bit lines. A 6T CMOS SRAM cell is the most popular SRAM cell due to its superior robustness, low power and low-voltage operation. An SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation. These two requirements impose contradicting requirements on SRAM cell transistor sizing.

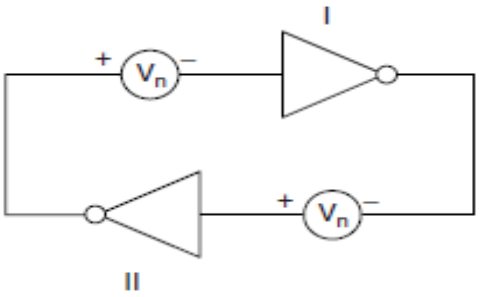



**Fig2. Inverters with two noise sources with adverse polarities**

For calculation of SNM (& indirectly DRV) the method or approach we have used is explain with the help of figure 2. It consists of two inverters connected back to back. The sources $V_n$ are the noise sources connected to the input and output of the

two cross coupled inverters. The two inverters hold the bi-stable state and their outputs nodes retain the voltage level stored in

the cell. As the noise voltages $V_n$ increases, the output nodes voltage

changes, this depict the SNM i.e. the allowed voltage levels of noise and thus the ability of the inverters to hold the state in the presence of noise.

The SNM depends on $V_{th}$, $V_{DD}$ and cell ratio [6]. So to improve the SNM performance of the SRAM cell, the cell ratio must be increased but increasing cell ratio means increasing SRAM cell area. Similarly the pull up ratio is important during write operation as its value determines how robust write operation can be performed under worst case conditions.

The goal of this paper is to present approaches and techniques to minimize the DRV, the parameters on which DRV is majorly dependent and lastly the simulation results to show the effects of DRV & SNM dependent parameters.

Section II presents and lists the parameters on which DRV is dependent. Sections III, the review of DRV minimization techniques are discussed. Section IV presents simulation results on 180nm CMOS process technology. Lastly, conclusions made from the paper.

## 2. PARAMETERS ON WHICH DRV IS DEPENDENT

The DRV is dependent on process & design parameters. Fluctuation in temperature & process variation causes degradation in SRAM cell performance and mismatch between two cross coupled inverters has a strong impact on its DRV. This mismatch could be global or local i.e. variation in $V_{th}$ & length of the transistors of the inverters may result in substantial change in the DRV of the cell.

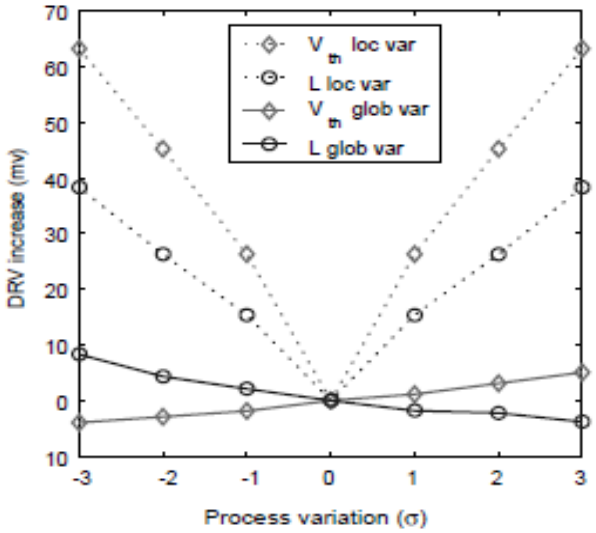



**Fig3. DRV Sensitivity to local and global parameter variation.**

Shown in figure from [1], it is observed, that the local mismatches among transistors $V_{th}$ and L results in substantial increase in DRV whereas a global change in the $V_{th}$ & L in the same direction, does not mismatch and hence, has a much weaker impact on DRV, the reason being the relative change in the driving strength of the inverters transistors whereas in global change their impacts compensate each other and result in small change of DRV.

Other parameter is temperature fluctuation, its affects has a weak influence on DRV as the change in transistors properties of the inverter is uniform.

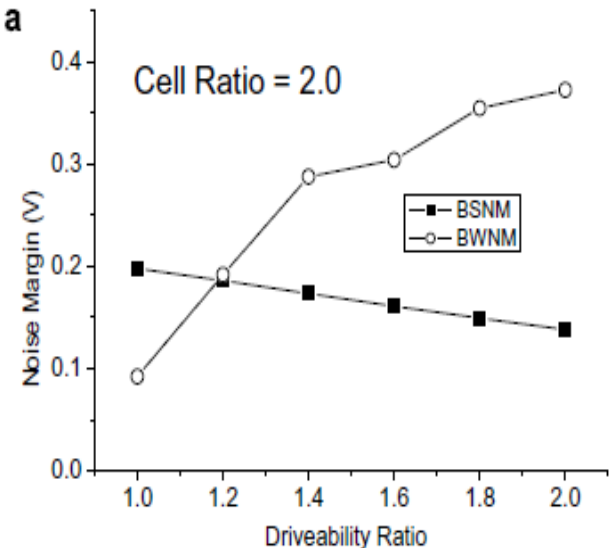
## 3. DRV MINIMIZATION TECHNIQUE – EXISTING & PRROPOSED

### 3.1 DRV minimization using Driveability Ratio

The most common & popular way to improve DRV is to improve SNM performance [5] and traditionally it was achieved by increasing cell ratio (i.e. the ratio of the driver transistor's W/L to the access transistor's W/L) but this technique cannot be applied as the SRAM cell is also continuously scaling and it would result into increase in cell area. Another technique is decreasing driveability ratio this will lead to improvement in SNM performance without cell area penalty.

The driveability ratio is defined as the ratio of the current driveability of the access and load transistors. In addition to this definition we assume that for the same device size, the current driveability of each driver transistors is twice that of each load transistor. The driveability ratio is derived for Write Noise margin (WNM) as this WNM is actually the magnitude of difference in driveability between PMOS load and NMOS access transistors in the SRAM. So the designing of SRAM cell inverters has to be done carefully before calculating the write margin of SRAM cell during write operation. Pull up ratio also fully depends on the size of the transistor.

As it is understood that in CMOS process the NMOSFET current drive is around twice that of same width PMOSFET, this alone provides sufficient DC noise margin for write operation but for SNM it is unacceptable. So the WNM & SNM follow opposite trends and larger the driveability ratio is , easier it will flip the state of the two inverters during read/write operation which in turn gives better WNM but worse SNM and it is also evident from [3] that the impact of driveability ratio is stronger than the cell ratio on WNM.



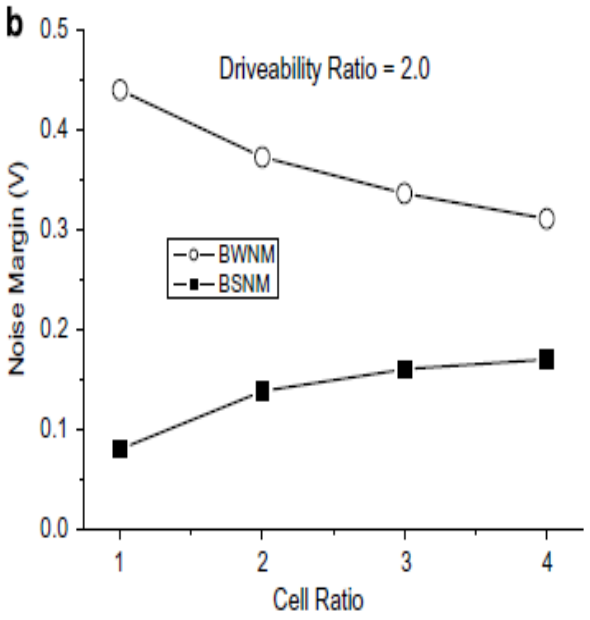



**Fig4. WNM, SNM against cell parameters (a) driveability ratio, (b) cell ratio.**

There are two ways to adjust the driveability ratio. First is dual threshold technology, where the access transistors can have high threshold voltage whereas the driver transistors have normal value of threshold voltage. Another way is to improve the mobility of load & driver transistor

Although driveability ratio improves SNM performance but it degrades the SRAM read/write time and due to this reason it is of major concern. Decreasing the driveability ratio will degrade the average read time i.e. increase in read operation time. Similarly the write time also has behaviour but in the case of relatively small change in the driveability ratio, the write time is determined by both load and access transistors. Even though, low value of driveability ratio has a much stronger impacts on intrinsic write time than the read time, the intrinsic write time is more than one order faster than reading due to much smaller load capacitance during write operation. So writing will not affect the overall system performance. Thus, the SNM performance improvement due to decrease in driveablity ratio is more prominent effect as compare to write time degradation.

Besides this we should also take into account that with this new SRAM cell design strategy that combines adjustment of driveability ratio & at the same time adjustment of cell ratio, there is a lower limit on the driveability ratio & if it moves down beyond the lower limit, the importance of WNM over SNM would be lost & will strongly affected by process variation & temperature fluctuations [8]. To cope with the lower limit problem of driveability ratio, "Write Assist" technology can be used in which the ground voltage is increased during write operation & this is realized using a peripheral circuit. By using the "Write Assist" technology the WNM performance will considerably improve.

## 3.2 DRV minimization by variation in length & Width of SRAM Cell Transistors

As the technology scaling progresses, the need for DRV scaling with technology is a major concern. Now days ULV SRAM memories are manufactured that targets ULP systems. But with voltage scaling, comes severe reliability hazard of SRAM data preservation. So in order to meet the voltage scaling of CMOS technology and low power design requirements, the degradation of DRV must be carefully done. So the effective technique to reduce the DRV with minimum secondary effects, such as area, hardware cost and performance for ULV and ULP designs, the sizing of SRAM is the solution. This can be easily understand from [1] figure 5 that shows DRV variation on its dependent parameters $\beta_i$ and $L_i$. In the figure parameter $\beta_i$ represents (W/L) ratio of the transistor: the pull up PMOS ($\beta_p$), pull down NMOS ($\beta_n$), and the access transistors ($\beta_a$). The value of $\beta_i$ >1 and $L_i > L_{min}$. It can be observed from the figure that DRV can be reduced only by increasing $\beta_p$ or $L_n$, with $L_n$ having stronger influence on DRV, whereas $L_p$ has smaller influence. It also observed from the figure that the sizing of access transistors has a very small impact on DRV because the two access transistors doesn't significantly affect the conducting path formed by the strong pull down NMOS transistor and the weak pull up PMOS device.

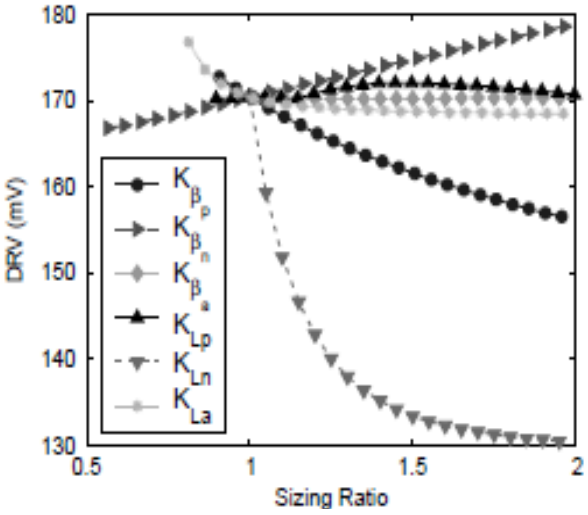



Fig5. DRV as a function of sizing parameters $\beta_i$ and $L_i$

In a non ULV performance optimized SRAM cell, the pull down NMOS devices are sized about 2x larger than the PMOS devices. These NMOS transistors are also with minimum L to minimize cell area is also highly sensitive to process variation, which results in increase in DRV [7].

There are certain techniques at circuit and architectural level that contribute to minimization of DRV by suppressing the leakage current in memories.

## 3.3 DRV minimization at circuit level

At the circuit level, the effective method of minimizing leakage power are to lower supply voltage and increase transistors threshold voltage ($V_{th}$), both degrades the speed of memory read/write operations and due to this reason it is not employ in performance critical memory design. Another method is dynamic control of transistor gate-source and substrate-source bias to enhance driving strength during read/write operation and low leakage paths during standby periods. Another technique is the negative word-line driving (NWD) scheme. It uses low $V_{th}$ access transistors with negative cut-off gate voltage and high $V_{th}$ cross-coupled inverter pair with boosted gate voltage to achieve both improved access time and reduced standby leakage power. Last technique is Dynamic Leakage cut-off (DLC) scheme, in

this the substrate voltages of non-selected SRAM cells biased at a voltage of ~2$V_{DD}$ for $V_{nwell}$ and ~ - $V_{DD}$ for $V_{pwell}$.

### 3.4 DRV minimization at architectural level

At architectural level, leakage reduction techniques include gating-off the supply voltage ($V_{DD}$) of idle memory sections, or putting less frequently used sections into drowsy standby mode. To achieve optimal power-performance tradeoffs, compiler-level cache activity analysis are employed to balance the potential for saving leakage energy against the loss incurred in extra cache misses. To further exploit leakage control in caches with large utilization ratio, the approach of drowsy caches allocates inactive cache lines to a low-power mode, where VDD was lowered while preserving memory data.

## 4. SIMULATION RESULTS

### 4.1 SNM Dependences

SNM is a key performance factor during read & write operations. During read operation SNM takes its lowest value and the state of cell is weakest. The value of SNM depends on the Cell Ratio (CR), Pull up Ratio (PR) and Supply voltage.

In this section simulation results of SNM variation on different parameters is measured & shown in plots. Apart from these parameters, observation on other parameters related to process variation & temperature fluctuation are also done.

In process variation, the threshold voltage of load & driver transistors is varied and its effects on SNM are observed. Similarly the effect of temperature variation above & below the room temperature on SNM is observed & calculated.

| | Vdd (V) | SNM (mV) |
|---|---|---|
| Technology 180nm | 1.4 | 252.4642 |
| | 1.6 | 325.4613 |
| | 1.8 | 383.4193 |
| | 2 | 432.4538 |
| | 2.2 | 476.4456 |
| | 2.4 | 517.4365 |
| | 2.6 | 556.428 |
| | 2.8 | 593.4241 |
| | 3 | 630.415 |
| | 3.2 | 665.4113 |

**Table1. Supply Voltage Vs SNM**

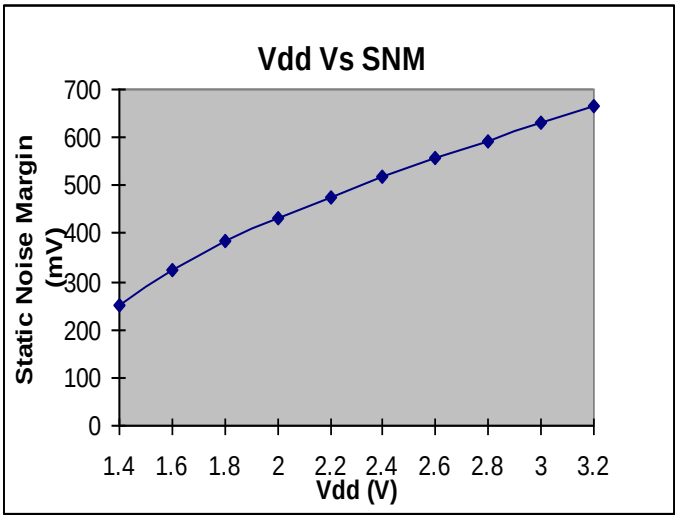



**Fig6. Supply Voltage Vs SNM**

| | Cell ratio | SNM (mV) |
|---|---|---|
| Technology 180nm | 1.5 | 404.4488 |
| | 1.7 | 414.4517 |
| | 1.9 | 423.4516 |
| | 2.1 | 431.4494 |
| | 2.3 | 437.4533 |
| | 2.5 | 443.4524 |
| | 2.7 | 448.4527 |
| | 2.9 | 453.4488 |
| | 3.1 | 457.4474 |
| | 3.3 | 460.4521 |

**Table2. Cell Ratio Vs SNM**

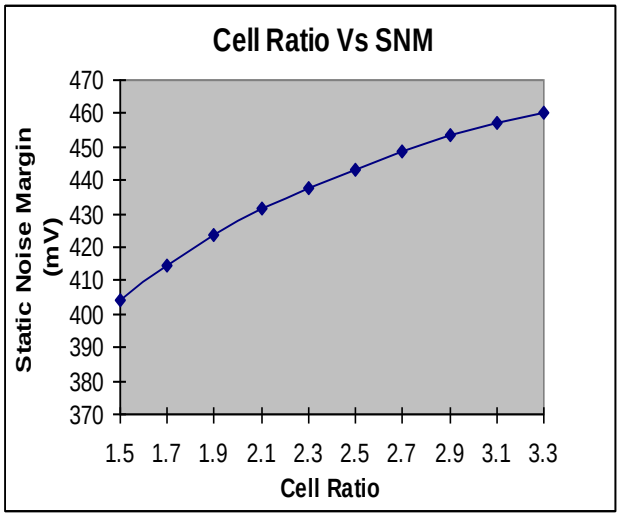



**Fig7. Cell Ratio Vs SNM**

| | VT,p (V) | SNM (mV) |
|---|---|---|
| Technology 180nm | -0.37 | 461.4519 |
| | -0.39 | 460.452 |
| | -0.41 | 459.452 |
| | -0.43 | 458.4516 |
| | -0.45 | 457.4508 |
| | -0.47 | 456.4487 |
| | -0.49 | 454.4539 |
| | -0.51 | 453.4525 |
| | -0.53 | 452.4493 |
| | -0.55 | 450.4535 |

**Table3b. Vt,p Vs SNM**

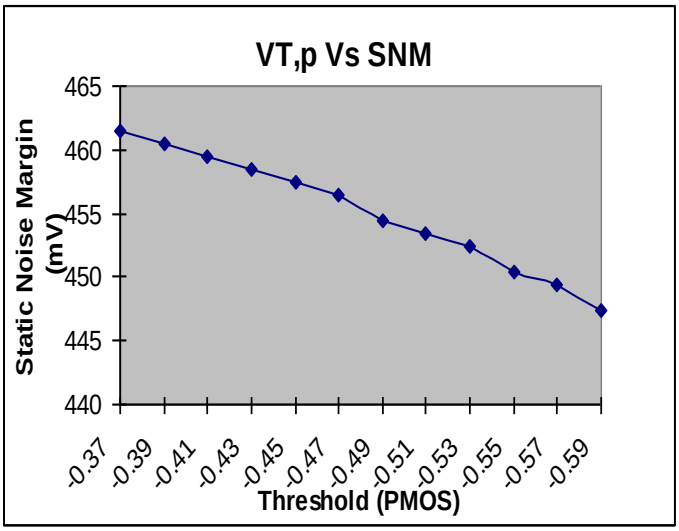



**Fig8b. Vt,p Vs SNM**

| | VT,n (V) | SNM (mV) |
|---|---|---|
| Technology 180nm | 0.37 | 458.4519 |
| | 0.41 | 474.4522 |
| | 0.43 | 505.4567 |
| | 0.45 | 520.4601 |
| | 0.47 | 535.4625 |
| | 0.49 | 551.4595 |
| | 0.51 | 565.4655 |
| | 0.53 | 580.466 |
| | 0.55 | 595.4648 |
| | 0.57 | 609.4676 |

**Table3a. Vt,n Vs SNM**

| | Temp. (°C) | SNM (mV) |
|---|---|---|
| Technology 180nm | 27 | 432.4538 |
| | 30 | 432.45 |
| | 33 | 431.4525 |
| | 36 | 430.4541 |
| | 39 | 430.4512 |
| | 42 | 429.4532 |
| | 45 | 429.4496 |
| | 48 | 428.4532 |
| | 51 | 427.454 |
| | 54 | 427.4516 |

**Table8c. Temp Vs SNM**

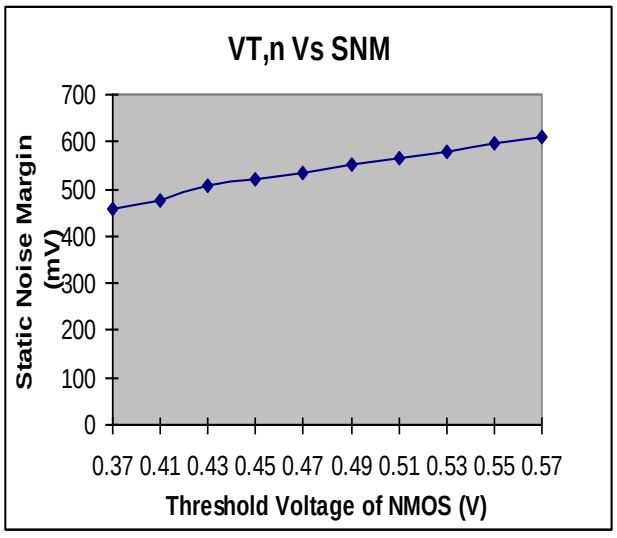



**Fig8a. Vt,n Vs SNM**

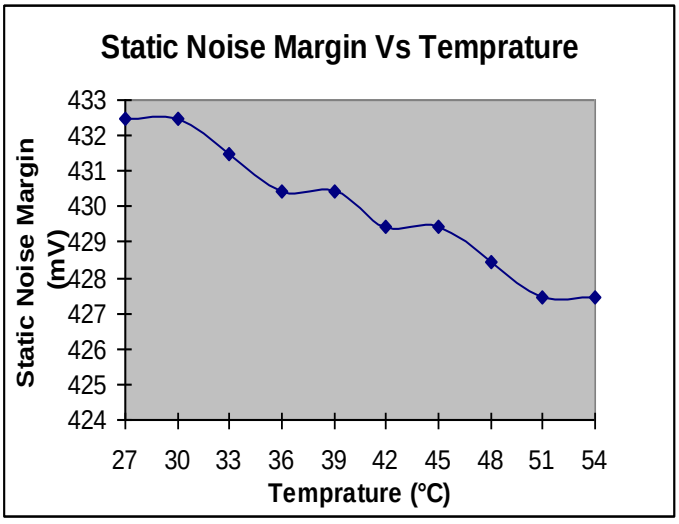



**Fig3c. Temp Vs SNM**

## 4.2 Effect of Cell Ratio & Pull up ratio on Read & Write Margin

Read and write operation of a 6T SRAM cell are affected by the cell ratio and pull up ratio. Thus, the SNM is also affected by these ratios [5]. The cell ratio is defined as ratio between the sizes of the NMOS transistor of the inverters and the NMOS access transistor. Similarly pull up ratio is defined as the ratio between the sizes of NMOS access transistors and PMOS transistors of inverters. It has a significant effect on all noise margins, since the strength of pull up ratio determines the strength of the cell to retain its stored data.

| | Pull up ratio | WM (V) |
|---|---|---|
| Technology 180nm | 0.5 | 1 |
| | 0.7 | 1.03922 |
| | 0.9 | 1.098 |
| | 1.1 | 1.1548 |
| | 1.3 | 1.206 |
| | 1.5 | 1.2612 |
| | 1.7 | 1.29 |
| | 1.9 | 1.35 |
| | 2.1 | 1.3967 |
| | 2.3 | 1.44194 |

**Table4. Pull Up Ratio vs. Write Margin**

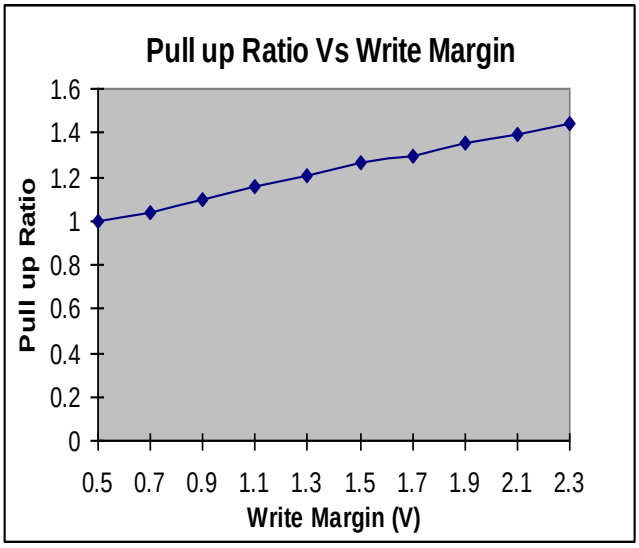



**Fig9. Pull Up Ratio vs. Write Margin**

| | Vdd (V) | RM(mV) |
|---|---|---|
| Technology 180nm | 1.4 | 530.4937 |
| | 1.6 | 565.4958 |
| | 1.8 | 597.4945 |
| | 2 | 627.4932 |
| | 2.2 | 657.4914 |
| | 2.4 | 687.4895 |
| | 2.6 | 717.4876 |
| | 2.8 | 747.486 |
| | 3 | 778.4829 |
| | 3.2 | 808.481 |

**Table5. Supply Voltage vs. Read Margin (RM)**

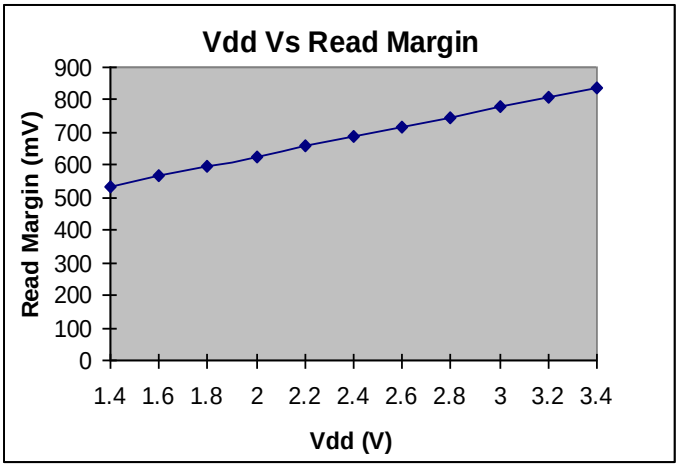



**Fig10. Supply Voltage vs. Read Margin (RM)**

5 Data Retention Voltage (DRV) vs. Static Noise Margin (SNM)

| | DRV (V) | SNM (mV) |
|---|---|---|
| Technology 180nm | 2 | 474.4126 |
| | 1.8 | 455.4148 |
| | 1.6 | 433.4433 |
| | 1.4 | 408.4325 |
| | 1.2 | 378.4472 |
| | 1 | 343.4527 |
| | 0.9 | 321.4606 |
| | 0.8 | 296.4619 |
| | 0.7 | 265.4719 |
| | 0.6 | 230.4731 |

**Table6. Data Retention Voltage (DRV) Vs Static Noise Margin (SNM)**

The static power consumption can be reduced by lowering power supply voltage to its standby limit. The SNM is calculated using conventional butterfly curve.

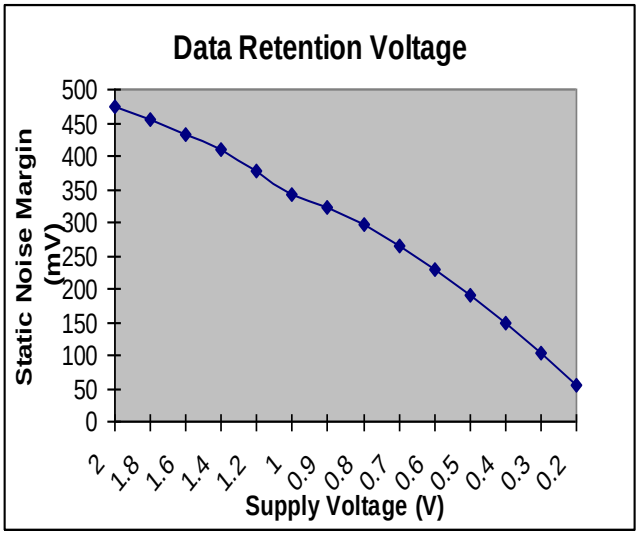



**Fig11. Data Retention Voltage (DRV) vs. Static Noise Margin (SNM)**

## 5. CONCLUSION

This paper present the limitations put on DRV under SRAM size scaling and under ULV. The DRV is concluded to be strongly dependent on process variation and also on temperature fluctuation. The DRV minimization techniques are discussed that further reduces the DRV but at the cost of SRAM cell area.
This paper also present the effects of supply voltage, process variation and temperature fluctuation on SNM through simulation on 180nm CMOS technology. In addition to this effects of Cell Ratio and Pull up Ratio are also observed.
The DRV minimization in this has been discussed at circuit level, the techniques comes at architectural level for achieving higher stability in ULV applications.

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