Systematic Approach in Building Clock Tree for SOC's

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ABSTRACT

The biggest problem we faced in designing clock trees is skew minimization. The reasons that add to clock skew include loading mismatch at the clocked elements, mismatch in RC delay. In the present scenario, if we set target insertion delay to the tool then minimum insertion delay is target and maximum insertion delay is floating i.e., global skew is not constant. This is undesirable so we achieve the control on insertion delay by performing many experiments on different parameters like target insertion delay, Global skew, clock shielding, Inserting redundant vias and Non-Default Routing rules (NDR). So far, we achieved 11.76% and 1.7% reduction in global skew and target insertion delay without clock shielding. But this is going to effect crosstalk even worse. So, with the help of NDR rules, we achieved 25.29% and 3.675% reduction in global skew and target insertion delay respectively. This project was done with the help of IC-compiler tool from synopsys. This deals with the controlling of Insertion delay and framing systematic approach in building clock tree for SOC's.

Keywords

Insertion delay, Global skew, clock shielding, NDR rules

1. INTRODUCTION

System-on-a-chip (SOC) design is defined as an IC, designed by arranging all individual VLSI designs so as to get full functionality for an application [1].Now a days, doing clock tree synthesis [2] is became major concern because we are going to suffer a lot from issues like Insertion delays [3], global skew, Crosstalk [4], Clock shielding [5]. Insertion delay is the delay from the clock definition point to the clock pin of the register. Global skew is defined as the maximum difference in the insertion delays of any two clock sinks in that corner.

Now a days, controlling the clock latency and skew [6] in the design is became most essential phenomenon. Large values of clock skew cause race conditions that increase the chance of wrong data being clocked in the flops. Controlling the skew and latency requires a lot of effort and hence Clock Tree Synthesis (CTS) [2] plays a crucial role in the design. Reducing the skew in all corners Prevents data mismatch as well as avoids data lock-up latches. When designing a clock tree, you need to consider performance specifications that are timing-related. Clock-tree timing specifications [7] include clock latency, jitter and skew. Non-timing specifications [7] include signal integrity and power dissipation. Many clock-design issues affect multiple performance parameters; for example, adding clock buffers [8] to balance clock lines and decrease skew may result in additional clock-tree power dissipation.

2. MOTIVATION AND PROBLEM FORMULATION

The biggest problem we faced in designing clock trees is skew minimization [6]. The factors that contribute to clock skew include loading mismatch at the clocked elements, mismatch in RC delay. In the present scenario, if we set target insertion delay to the tool then minimum insertion delay is target and maximum insertion delay is floating i.e., global skew is not constant. This is undesirable so we want to achieve the control on insertion delay by performing many experiments with varying target Insertion delay.

Though there is some literature regarding reducing insertion delay through Schmitt trigger [8], resizing cells and buffers [9]. But those are very difficult to implement practically because used substrate as input to another gate.

In this project, the whole idea is if insertion delay is 900ns and 100ns as global skew clock, then target insertion delay will be 900ns and target to tool will be 850ns, which acts as minimum insertion and 950ns as maximum insertion delay.

3. ADOPTED PROCEDURE AND RESULTS

In this section, we are going to discuss about the procedure followed to reduce maximum insertion delay, so as to keep constant global skew across all the stages in the design process all the way from netlist to GDSII format. Initially, we took target insertion delay as parameter and done multiple experiments and set those results as our reference. These results shows us from which stages global skew is varying. Target insertion delay results are as follows. To obtain this, we need to set target insertion delay in the cts_params.tcl file in the scripts directory before running the design.

Majorly the APR(place and route) flow starts from Verilog netlist to all the way GDSII format which is the final design going to send fab. Fig 1 shows the general APR flow for which data setup includes importing design from synthesis tool. So, we need to import design from synthesis tool and do some data setup i.e., setting environment variables and project paths, then there is a need of floorplanning [10], placement of all macros at some corners first followed by all blocks because macros will consume a lot of space and can be huge occupies 5-6 metal layers also, clock tree synthesis, routing clock first then all data signals because clock signals are very high frequency and frequently passing signals, node area checks (checks for any random particle defects), add_filler stage will take care of base layer continuity, fill stage will be responsible for to prevent metal etching and the final stage will dump all reports for the entire flow. After routing remaining stages comes under chip finishing category.

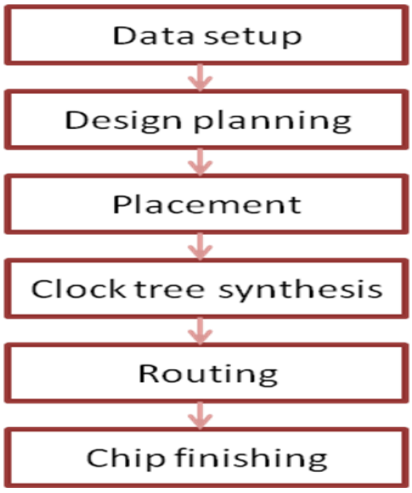

Fig 1: General APR flow

Chip finishing includes nac_ze_fix(node area checks with zener diodes to fix them), adding metal fillers and checking base layer continuity and finally verifying the design.

fig.2, we consider 5 stages for every experiment. The stages are CTS (clock tree synthesis)[11], post_place_opt, clk_pre_route, route and route_opt respectively.CTS stage is responsible for building clock tree and inserting buffers. Post_cts_opt is responsible for fixing all hold violations. Clk_pre_route is responsible for routing clock first than data signals due to the clock's high frequency signals and clock shielding too. Route is responsible for actual routing of data signals. Route_opt is responsible for optimization. From the fig.1, we can say that global skew is out of control in the clk_pre_route stage.

Global skew as a second parameter, we done experiments and concluded that global-skew is not responsible. settings same as target insertion delay. In the Table 1, our desired results are 100 as global skew and 550 as Target Insertion delay.

Clock shielding [6][12] as a third parameter, done multiple experiments and concluded that it is the one causing global skew out of control. By disabling clock shielding in the block_setup.tcl file in the scripts directory, we achieved 11.7% and 1.7% reduction in the global skew and insertion delay respectively. Though, this is in favour of reducing global skew range, it is causing severe damage in form of crosstalk.

As a fourth parameter, we took inserting redundant vias [6] parameter in the design. Inserting Redundant vias means replacing single vias with double vias which reduces resistance because 2 vias will be in parallel and leads to reduction in delay (T = RC). We initially applied this all over the design and didn't achieve result because out of too many vias only few (100) got replaced with double vias.

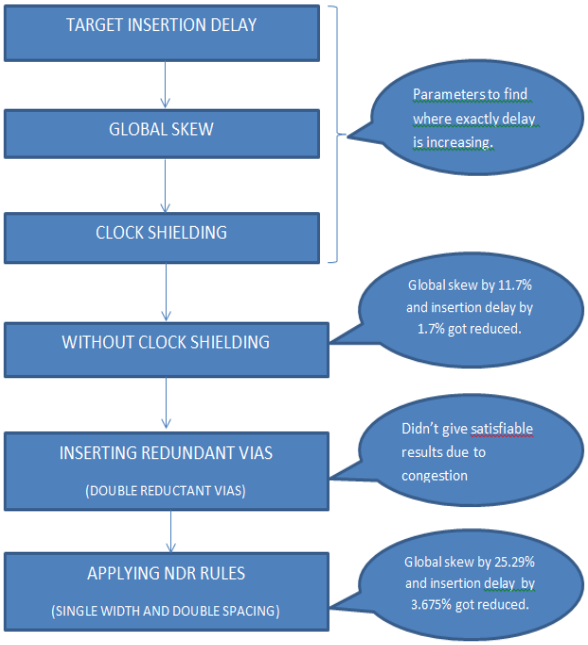

Fig 3: Adopted Procedure

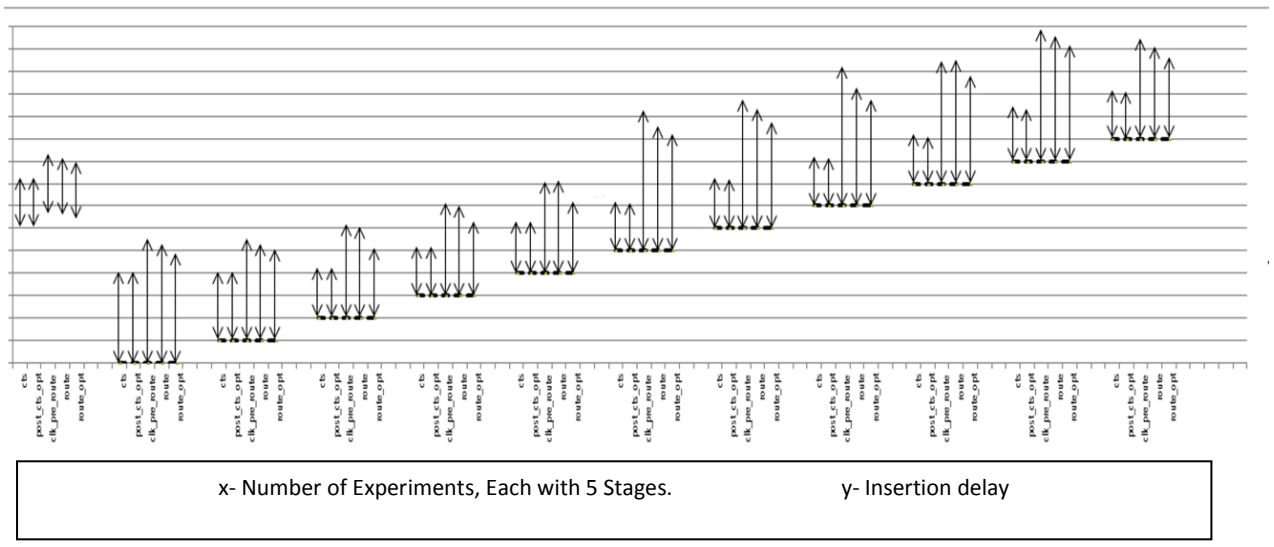

Fig 2: Variation of insertion delay in each stage

Table 1: comparison of Global skew and Insertion delay across various parameters

With Shielding		With-Out Shielding		With Shielding & With NDR	
Global skew	**Target insertion delay**	**Global skew**	**Target insertion delay**	**Global skew**	**Target insertion delay**
170	**585**	**150**	**575**	**127**	**563.5**
		11.76%	**1.7%**	**25.29%**	**3.675%**

4. CONCLUSION

The systematic approach in building clock tree for SOC's will provide you the novel procedure in controlling insertion delay and global skew by 25.29% and 3.675% respectively. There is still a scope for further research on these topic.

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