Design a Low Power ADC for Blood-Glucose Monitoring

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Abstract:

This paper describes the design of a low-power CMOS based current-frequency (I–F) Analog–Digital Converter. This ADC is designed for blood-glucose monitoring. This current-frequency ADC uses *n*A-range input currents to set and compare voltage oscillations against a self-produced reference to resolve 0–32*n*A with an accuracy of 5-bits at a sampling rate of 225MHz. The comparator used is dynamic latched comparator and the 5-bit counter and 5 bit latch is used to fetching the output in parallel form. This is designed in a 0.6µm CMOS technology supplied at 1.8V; it operates for a range of 0.0- 1.8V input voltage with power consumption below 1.1µw using Cadence tools.

Keywords

Current-frequency ADC; Low power; Dynamic Latch comparator

1. Introduction

Blood glucose meters use to measure the concentration or amount of glucose in blood diabetics allowing for the direction of the proper dose of insulin to maintain balance. Blood glucose meters are small computerized machines that "read" your blood glucose, then applying the blood to a chemically active disposable 'test-strip'. Different manufacturers use different technologies, but most of them, measure an electrical characteristic, and further use this to determine the glucose level in the blood.

The analog to digital convertor must resolve the current that a miniaturized ampere-metric glucose sensor generates, which is typically in the range of 1 *n*A to 1 µA, in this case the maximum value of current can reach up to 31*n*A with five-bits of resolution. Similarly, because miniaturized kinetic harvesters can generate less than 10µW, the design aims to dissipate around 1µW. As alluded earlier, the time constant associated with glucose variations in the body is on the order of minutes, so over-sampling the system at around 100 Hz is sufficient.

2. Organization of the paper

This paper presents a current–frequency (*I–F*) analog to digital convertor, working at 0.6µm CMOS technology that is able to resolve nA's to within five bits of accuracy while drawing 1.1nA from a 1.8-V supply. In this design a dynamic latched comparator [2] is used to compare the input value with the reference voltage, a five-bit counter [3] is used to get 5-bit parallel output which further fetch to controller to find the concentration of glucose in the blood sample by 5 bit latch [4]. The input range that the proposed ADC receives corresponds to what ampere-metric sensors produce and the power level it requires to operate is within the range that energy-harvested systems can supply [1].

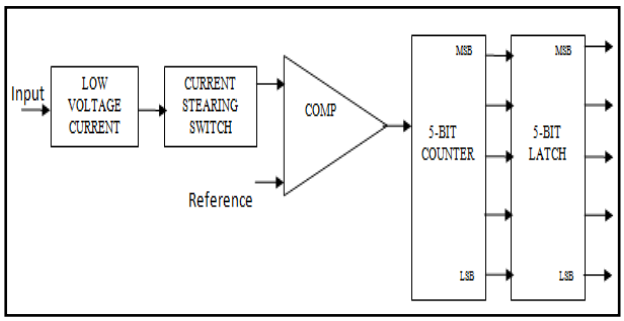

Fig 1: Block Diagram of Current-Frequency ADC

The block diagram of I-F ADC is shown in Fig.1, this explains that the signal (analog form) is firstly given to input stage (contains low voltage current mirror and current steering switch) to drive the current to comparator, then a comparator is used to compare this signal with the reference signal. Now we get a data to which we want in parallel form, for this we use a counter that fetch the output and forward the signal to latch.

3. Circuit Design

Frequency-based ADCs generally match the low-power and low-speed requirements that harvester-powered ampere-metric glucose monitors impose. More particularly, because glucose sensors ultimately generate a current, directing input current into the capacitor of a ramp-based oscillator converts current into frequency directly, which means current–frequency ADCs of this sort need not include additional power-consuming stages to condition the input. What is more, the integrating capacitor inherent in these ADCs filters unwanted noise.

3.1 Schematic of I-F ADC

Current-frequency ADC is based on voltage-to-frequency converter (VFC), in which an oscillator is used whose frequency is linearly proportional to a control voltage. In this schematic we are feeding input to the current mirrors, to drive the input to the comparator. As shown in Fig.2, cascode-mirrors PM0–PM4 and NM2–NM10 receive and fold input current i_1 or I_R so switches PM6 and PM5 can steer it into or away from integrating capacitor *C* with a value of 1pF.

Comparator senses C voltage V_C to determine the connectivity of NM0 and PM5. PM6 And NM1 keep the mirrors conducting to the supply and ground when their corresponding switches NM0 and PM5 are off, so the mirrors do not suffer from start-up delays, which would otherwise extend the delay across the loop (i.e., increase t_d and distort V_C's ramp.

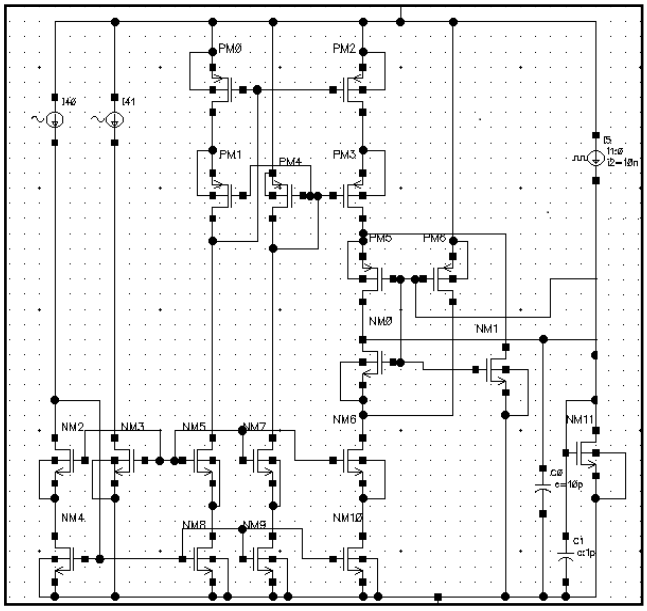

Fig 2: Schematic of Current mirror and current steering circuit

Now as we give an analog signal at the input, it first goes through the current mirror and current steering circuit, then this signal is compared with the reference signal at frequency of 225 MHz and a voltage of 1.8V.

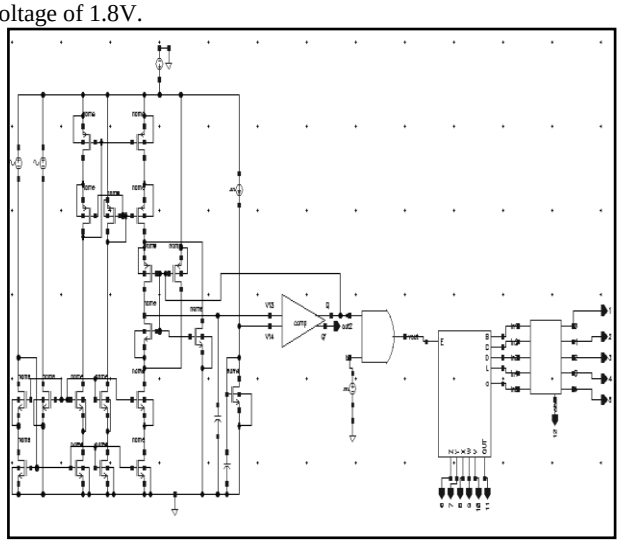

Fig 3: Schematic of Current-Frequency ADC

The output of comparator is given to counter which separate this digital signal into 5 different samples, which is latched through which we get output of 5-bit resolution.

This resolution is calculated by the formula

$$resolution = log_2(\frac{VF_S}{\delta V}) \qquad (1)$$

Where VF_S is full-scale output voltage range

δV is full-scale input voltage range

3.2 Dynamic Latch Comparator

The dynamic latched comparator consists of three stages, includes an input stage which consist current mirror, a flip-flop and SR latch. This architecture uses two non-overlapping clocks (ϕ1 and ϕ2) shown in Fig.4, which operates in two modes, regeneration mode during ϕ1 and reset mode during ϕ2.

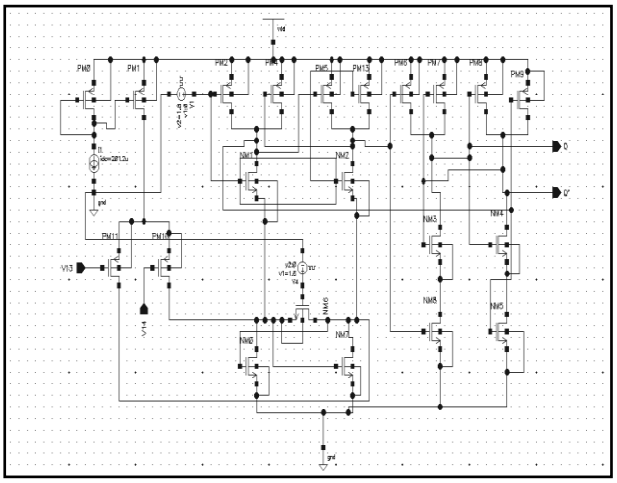

Fig 4: Schematic of Dynamic Latch Comparator

During reset mode the input voltage difference is established at node A and B. The regeneration happens during a short time when ϕ1 is rising and ϕ2 are falling. At the end of regeneration process the SR latch is driven to the digital output levels. The power consumption of the comparator is 33µW at a frequency of 225MHz.

The design was implemented at 0.6µm CMOS technology operating at a ±1.8 V power supply with 8-bit of resolution and input range of 1.8 V, the reference taken is 1.8V. And transistor widths are calculated as per the comparator requirement [2].

W_{12} = 4*u*m, W_1 = 6*u*m,

W_8 = 4*u*m, W10 = 10*u*m,

W_6 = 30*u*m

These widths are calculated by using following formula

$$\tau_{reg} = \frac{(\alpha W_4 + C_P)}{\sqrt{\frac{2\, I_4\, W_4}{L_4\, K_{pm}}}} \qquad (2)$$

Considering $\alpha W_4 = C_p$

Where

C_p is the other parasitic capacitances at node a or b

W_4 is the width of transistor M4

I_4 current at transistor M4

3.3 Five-Bit binary synchronous counter

The Counters are among the most basic of designs in digital systems. Along with being simple to make, counters, in general, are archetypal components of most digital systems as they are used to store (and sometimes display) the number of times a particular event has occurred.

The different number of implementations of a 5-bit counter is vast. Here counter used is synchronous counter which used to count from 0 to 31.

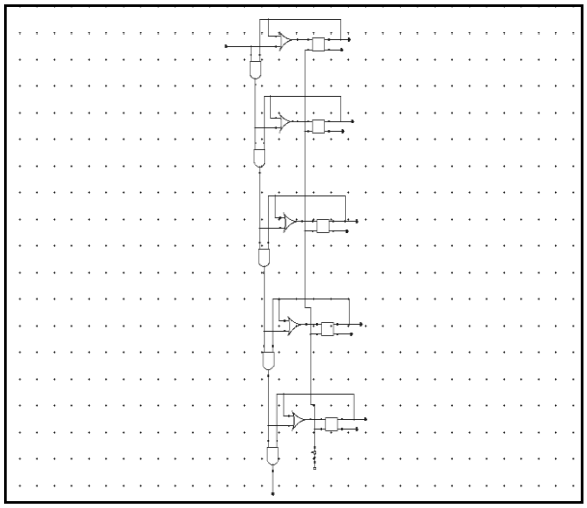

Fig 5: Schematic of 5-bit counter

The counter described in this paper was designed to be an up-counter as shown in Fig.5. This means that the whole design is controlled by a single clock and that the counter will only count from 0 to F and start back over. The counter is realized using D flip-flops [6]. The D flip-flop was chosen because of its simplicity over the JK flip-flop; it only takes one input instead of two, and requires less interconnect which should lead to less delay. Also, the synchronous up-counter nature of the design was chosen because it was easy to implement. This counter is counting from 0 to 1.8 volts, with a precision of 0.59375V.

3.4 Five Bit 2:1 Mux-Latch

A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. The working of 2:1 Mux is, when select line is 1 b is the output and when select is 0, a will be there at output.

Fig.6 depicts the preferred dynamic latch circuit. The latch circuit either transfers the input logic level to the output (during clock signal is kept at logic "1") or keeps the last output logic level (during clock signal is kept at logic "0") depending on the controlling clock signal.

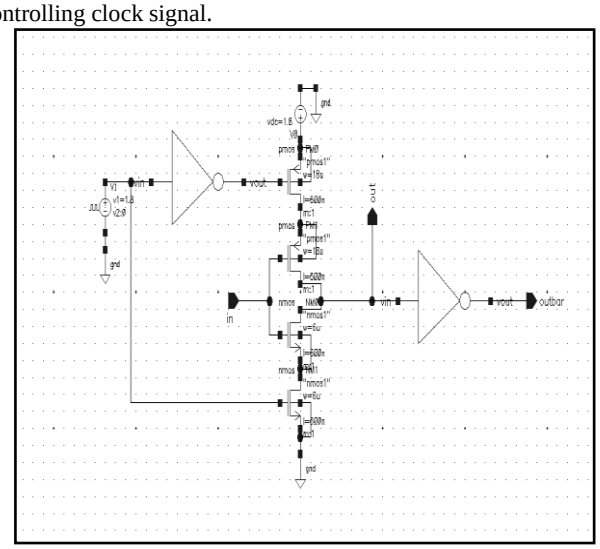

Fig 6: Schematic of Dynamic latch

In other words, clock "0" means conversion phase, and clock "1" means sampling phase. This control between digital and analog parts of ADC is obtained. In fact, it is not possible to convert an analog input level to its digital value instantly. A very small time period is necessary for the digital part to complete its job. Therefore, a dynamic latch circuit usage is inevitable for ADC design. This time is called as "conversion time" in general and it is shortest in I-F ADCs, but very long for serial type of ADCs.

The output of the latch is given as input to 2:1 mux and is also used as select line for the mux of next block as shown in Fig. 7, for 5-bit resolution.

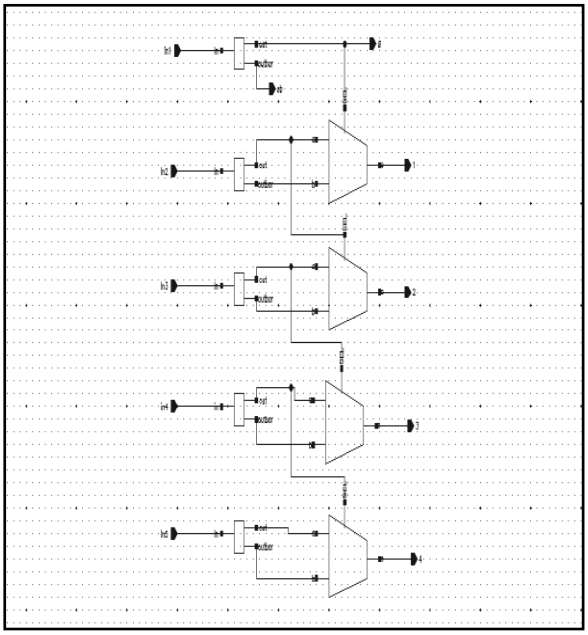

Fig 7: Circuit diagram of 2:1 mux type latch

4. Power Reduction

While designing any CMOS circuit power is a very important issue and in ADC we always required low power. This power can be reduced by using low power techniques such as decoupling capacitor, variable frequency, Clock gating, scaling down voltage etc. Clock gating technique is one of these power reduction techniques adopted in this design is shown in Fig.8

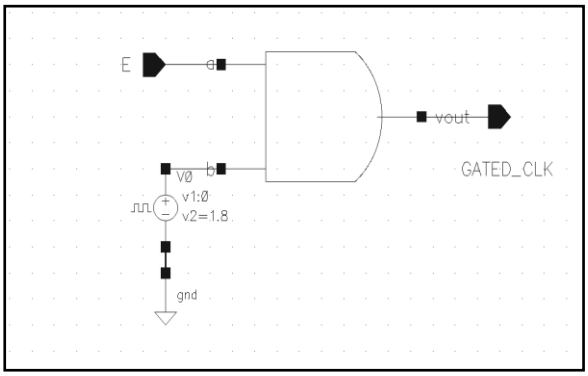

Fig 8: Circuit of Clock gating without latch

Clock-gating is a well-known technique to reduce clock power. In a sequential circuit individual blocks usage depends on application, not all the blocks are used simultaneously, giving rise to dynamic power reduction opportunity. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation [16].

5. Experimental Results and Simulations

Designing, simulation, schematics and comparison of various performance parameters were done for two different ADC's.

Simulations were carried out using Cadence Tools. The present work, technology taken is 0.6µ with sampling frequency of 225MHz and a power supply of 1.8V.

Table1. Design Specifications

Parameters	Value
Technology	600nm
Sample frequency	225 MHz
Power Supply	1.8 V
Stop time	200 ns
Resolution	5 bit
Power	1.1 µw
Reference Voltage	1.8 V

A 5-bit data is achieved with a power of 1.1µW, as shown in Table.1

The transient response of the I-F ADC is shown in Fig.9 output waveform is collected from the 5- bit latch, which is collected in parallel form. This 5 bit data has sampling rate of 225MHz.

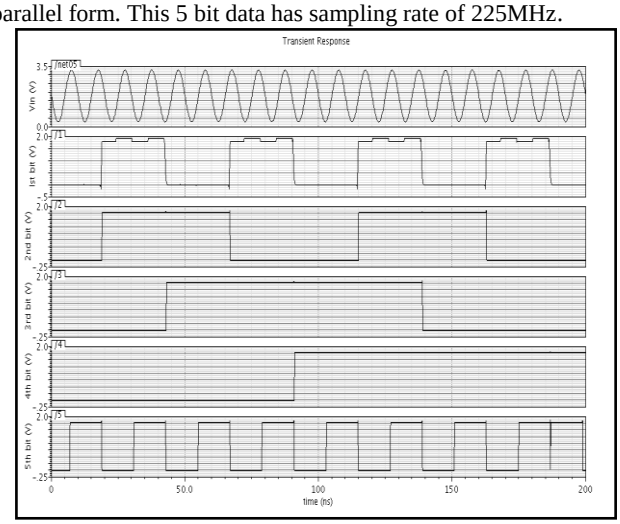

Fig.9 Transient response of I-F ADC

The waveform is taken with a stop time of 200ns.The first bit is MSB and last one in LSB of ADC's output. The designed ADC results are compared with the current I-F ADC and the flash ADC [7].

Table 2 shows the comparison between these two ADC's. Reference ADC is done at 0.6µm, so firstly design with same parameters, then with 0.6µm technology and got a improved power of 1.1µW at a sampling frequency of 225 MHz with a improved resolution of 5 bit from 4.25.

Table2. Comparison between flash and current-frequency ADC's

	PREVIOUS WORK	PRESENT WORK
Parameters	**I-F ADC**	**I-F ADC**
Technology	0.6 µ	0.6 µ
Resolution	4.25	5
Power supply	1.2 V	1.8V
Power(W)	1.3µ	1.1µ
Sampling Freq.(MHz)	225	225

6. CONCLUSIONS

This paper presented low power 5-bit current- frequency ADC design at 0.6µm technology and compare the work with the previous current frequency ADC. This ADC is designed for implantable blood glucose monitoring. With improvement in the power consumption of 1.1µW at 225MHz sampling frequency and power supply of 1.8 V.

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