Low Power BiCMOS SRAM using 0.18µm Technology

Rajani Saini
M Tech Scholar
Lovely Professional University,
Phagwara, Punjab, India

Pawandeep Kaur
Asst. Professor
Lovely Professional University,
Phagwara, Punjab, India

ABSTRACT
Rapid advances in the field of very large scale system designs brought memory circuits are continuously regulated and in turn, more number of cells could made possible to integrate on small chip. CMOS technology prove boon to memory circuits, which replaced the most of complex circuits to simpler circuits. But the combination of bipolar junction transistors changes the entire scenario. The objective of this paper is to design low power SRAM cell array by using BiCMOS technology. In this paper, BiCMOS technology is used to design SRAM cell using 0.18µm technology. The results are compared with standard 6T SRAM cell. The proposed design results in significant reduction in power consumption as compared to standard 6T SRAM cell and it is verified that the proposed cell can operate at much low supply power with much reduction in power consumption. All the simulation is completed on the Cadence Virtuoso tool.

Keywords
BiCMOS SRAM, Standard 6T SRAM, Power Consumption, Power Dissipation and 0.18µm technology.

1. INTRODUCTION
The evolution of CMOS in the field of electronics provides opportunity to bring an important and necessary change in the designing field. Its advantages of low power consumption, reliable performance and high noise immunity help in designing compact circuits which can be used in handheld devices. It mainly influences the memory devices like RAM, ROM and flash memories. The applications of memory devices in the electronics gadgets like mobiles, digital cameras, toys increase the demand to innovate or to improve the memory devices. The BiCMOS technology changed the whole scenario of designing memories [2][3][14]. The combination of bipolar and CMOS, put forward the opportunity to design systems. The advantage of high switching speed, high gain and high current drive capability of bipolar output transistors and low power, high noise immunity, high input impedance, zero static power dissipation and high density provided by CMOS, can be used to improve the existing memory devices for hand held portable devices.

The basic architecture of large memories is basically comprised of pre charge circuit, cell array, decoders, control circuit, read and write circuits word lines and bit lines [5].

Each cell contains a cross coupled inverters to store data. Row and column control circuitry has control to access the cell for read or write operation. The row and column decoders identify or select on which particular cell the read or write store 1 bit data and the data is overwritten by write circuit

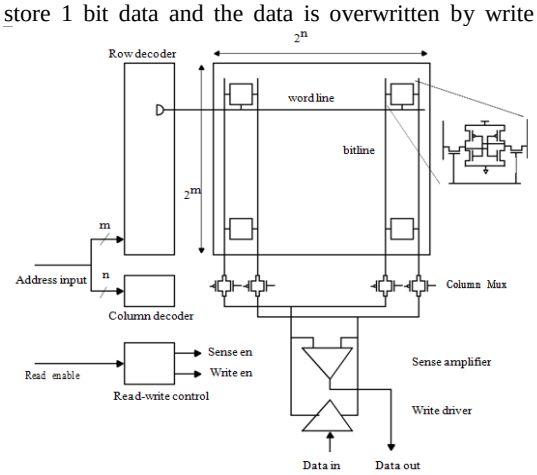

Figure 1: Memory cell array

whenever new data is appeared and when write circuit is enabled. The horizontal lines are "word lines" which are driven outside the array and the vertical line are called "bit lines" along which the data flows. Whenever data is written or read from a particular cell, the row and column of that cell is selected by row and column decoders respectively and the operation is performed.

1.1 The proposed BiCMOS SRAM cell:
The conventional SRAM cell consists of 4 NMOS and 2 PMOS. The combination of NMOS and PMOS form an inverter. These two inverter pair connected back to back, which act as a latch and store data and rest 2 NMOS act as access transistors. As long as the supply exists, the latch will preserve one of its two possible states i.e. "1" or "0". The word line (WL) is turned high whenever read or write operation is to be performed. It enables the access transistors and the data will be read or written. The bit lines bl and blb contains complimentary data.

In this paper, one of the inverter pair of SRAM cell is replaced by BiCMOS circuit. In the BiCMOS inverter pair, the CMOS are connected with BJTs with common emitter configuration. There are total 8 transistors in the cell, two NMOS, two PMOS and two BJTs along with two NMOS access transistors. The BJTs are connected in common emitter configuration.

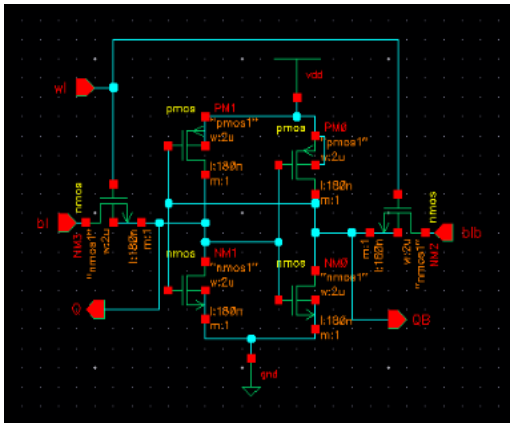

Fig 2: Standard 6T SRAM cell

The gates of both BJTs are controlled by CMOS pair to gain maximum advantages of both the transistors. The word line WL controls the access of transistors for the cell operations. From the cell design, M1 and M5 along with Q2 and Q1 respectively form BiCMOS inverter and M5 and M6 form CMOS inverter. Transistors M3 and M4 act as the access transistors to control the cell operations and connect the cell to BL and BLB bit lines. These bit lines, BL and BLB are pull up by precharge circuit. The sense amplifier is connected to the cell through the nodes Q and QB to read the stored data from the cell by measuring its voltage difference between BL and BLB.

The write driver circuit writes the data to the cell through its driver transistors. When the input is high, the NMOS transistor M1 is on, causing Q2 to conduct, while M5 and Q1 are off. The result is a low output voltage. A low V_{in}, on the other hand, causes M5 and Q1 to turn on, while M1 and Q2 in the off state, resulting in a high output level. In steady state operation, Q1 and Q2 are never on simultaneously, keeping the power consumption low. In BiCMOS structure, the input stage and the phase splitter are implemented in CMOS, which results in a better performance and higher input impedance.

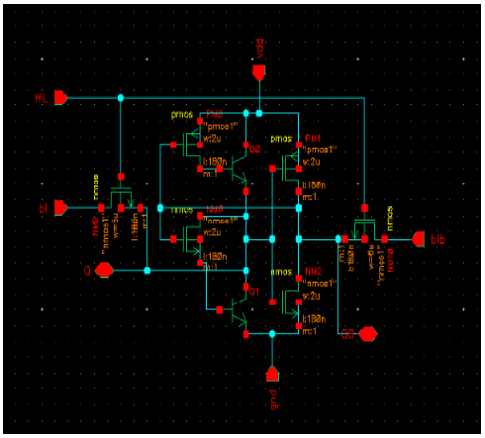

Fig 3: Proposed BiCMOS SRAM cell design

1.1.1 The Proposed cell operation: There are main three operations:

1.1.1.1 Hold Operation: When the word line, WL=0, the access transistors are disabled. Assume that node QB is higher than node Q, most of the current will flow through Q_p causing voltage drop from V_{dd} to Q. Where QB remains at the same potential as V_{dd}. Hence, the cell holds the state with a voltage difference between internal nodes Q and QB.

1.1.1.2 Read Operation: To read data from the cell, both the bit lines BL and BLB are precharged high to V_{dd} voltage before the word line, WL is turned on. When WL is turned on, it enables the access transistors. To read "1" as stored data, the voltage across nodes Q=VDD and QB=0. In this situation, the transistor M5 is on, setting the base of the Q1 to V_{DD}. Q1 acts as emitter follower and conduct most of the current. As the transistor M1 is off, allows Q2 to drain the base charge to ground. Since the Q2 operates in forward-active mode, the stored charge is small and Q2 turns off. As Q1 conducts most of the current, this causes BL to clamp at same voltage, V_{DD}. The difference in the bit line voltages is sensed by current mirror sense amplifier, which will sense which line has higher voltage and tells what is stored in the cell. To read "0", the reverse action is true. The voltage across nodes is Q=0 and QB=V_{DD}. In this case, Q2 will conduct most of current and BLB is clamped at the same voltage. As the node Q is lower than the reference voltage, the bit line BL will charge to V_{BE} below V_{dd}. Transient waveform for read operation is shown in figure.

1.1.1.3 Write Operation: To write data in the cell, firstly, what the data is to be written is applied to bit lines through the input DATA of write circuitry and write enable WE should be high. Then WL is put high. The new data is overwritten into cell. To write "1", the BLB should be high. M1, Q2 and M6 will work linearly. The high voltage across BLB drives the M1 and Q2. As in this case Q2 acts as the emitter follower and draws maximum current, which causes to drain the voltage across BLB to ground, thereby pulling all charge from BLB to ground and causes BLB low. There by forcing to write "1" in the data. It is mandatory to note that for write capability of the cell, the sizing of the transistors should be checked. The cell ratio should be greater than "1", i.e. the ratio W_3/L_3 should be greater than W_1/L_1. To write "0" into the cell, operation is reversed. M5, Q1 and M2 will operate linearly. As the BL is high, the voltage across node Q is also high and pulled down by Q1 through Q2 which operate in forward-active mode, forcing the cell to change the value to "0". The transient waveform of write operation is shown in figure.

2. RESULT

The simulation is done on the Cadence Virtuoso tool using 0.18µm technology. The results of proposed BiCMOS SRAM cell are compared with standard 6T SRAM cell.

2.1 Power consumption

The static power and dynamic power are the main components of power. In static phase, the power consumed is calculated when transistors are not in switching process. It is given by

$P_S = I^* V_{dd}$

Where I is the total current flowing through the cell

Dynamic power is due to switching process during SRAM operation.

2.1.1 Dynamic power: Further, dynamic power is divided into two: the setup phase and the operation phase.

In setup phase, the power is subjected to precharging and discharging of bit lines and word line. It is given by

$P_D = C^*V_{dd}^2*f$

Where C is sum of load cpacitance and internal capacitance,

F is the clock frequency.

Power dissipation can be reduced by reducing switching activity and clock frequency, but it deteriorates the performance of the circuit and reduction in V_{dd} result in data instability. The only way of reduction is by lowering the bit line capacitance. But using the proposed cell design, V_{dd} can also be lowered to reduce the power dissipation. Because the proposed circuit operate with low power even at 0.5 V V_{dd}.

In operation phase, the power consumed is dominated by active power and leakage power. When both pull-up and pull-down networks are active, the power is consumed in creating direct current path from V_{dd} to ground (gnd) is reffered as active power and the power consumed when charge leaks through transistor when it is off, is leakage power.

The power consumption in case of proposed cell is much less as compared to power consumed by standard 6T SRAM cell as shown in table 1.

Table 1. Comparison of power consumption in proposed cell to standard cell

	Power Consumption
Standard 6T cell	142.6µW
Proposed cell	76.85µW

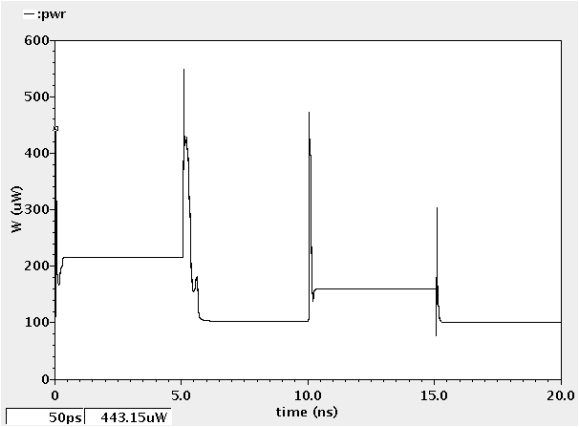

Fig 4: Power consumption of 6T SRAM cell

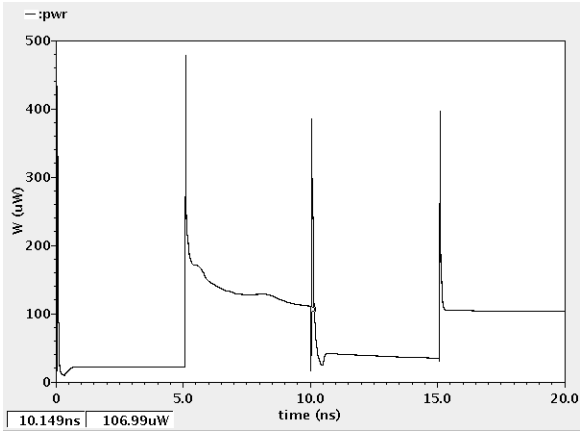

Figure 5: Power consumption of proposed cell

2.1.2 *Read and write Operation:* The results of read are shown below. It is clear that there is significant power reduction is seen in proposed cell design as compared to standard 6T SRAM cell.

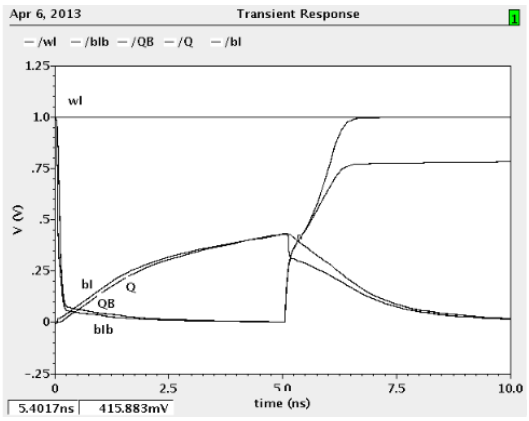

Fig 6: Write operation

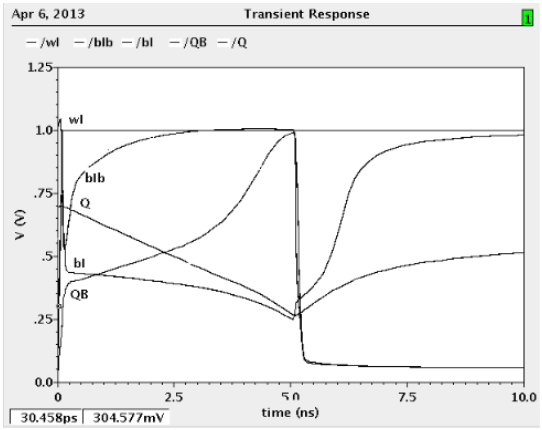

Fig 7: Read operation

Table 2. Read and write power consumption

	Standard 6T SRAM cell	Proposed BiCMOS SRAM cell
Write 0	73.0µW	60.3µW
Write 1	72.7µW	42.5µW
Read 0	152.4µW	87.5µW
Read 1	150.6µW	102.3µW

2.1.3 *Delay:* Delay is the important parameter of the memory cells, which tells how much efficient the memory cell is. It depends upon the read and write operation of the cell. The delay of conventional 6T SRAM cell and BiCMOS SRAM cell is given in table. The read and write operation delay is also calculated, which is listed in table 3.

Table 3. Delay comparison

Cell Operation	Conventional 6T SRAM cell	Proposed BiCMOS SRAM cell
Write (1-0)	2.69 ns	2.49 ns
Write (0-1)	6.79 ns	5.19 ns
Read 1	3.46 ns	1.05 s

2.1.4 Power Dissipation reduction: It is seen that to reduce the power dissipation, lowering the supply voltage, V_{dd} is not good decision, as it leads to data instability. The results of power consumption by proposed BiCMOS cell at different supply voltages are given in table 3. The reading show that as we reduce the supply voltage the power consumption by proposed cell also reduces. This shows that by using the proposed circuit, we can lower the power dissipation of the cell in parallel to bit lines capacitance.

Table 4. Power reduction at different supply voltages

Supply voltage	Standard 6T SRAM cell	Proposed BiCMOS SRAM cell
1.5 V	529.3µW	386.6µW
1.2 V	273.5µW	120.5µW
1 V	142.6µW	76.8µW
0.75 V	53.5µW	27.3µW
0.5 V	28.9µW	3.5µW

3. CONCLUSION:

In this paper, low power circuit is designed by using BiCMOS technology on 0.18µm technology. In this proposed paper, the power consumption by the cell is greatly reduced about 55% by using BiCMOS circuit. The combine features of CMOS and BJT, results in a low power consumed, low dynamic power dissipation SRAM and reduced read and write operation power. It is also observed that by improving read and write circuitry further power can be reduced, which can prove a boon to memory design arena.

4. REFERENCES

[1] Xuelian Liu, Hadrian Olayvar Aquino, Alexey Gutin and John. Mcdonald. 2010 A 125-ps Access, 4GHz, 16KB BICMOS SRAM. IEEE, (2010) 1222-1225.

[2] Takada, M. Nakamura, K.; Yamazaki, T. 1995 High speed submicron BiCMOS memory. IEEE Trans. Elect. Dev. 42 (1995) 497-504.

[3] Santoro. M, Tavrow. L, and Bewick,G. 1994 A subnanosecond 64K BiCMOS SRAM. IEEE Proc, 1994 Bipolar/BiCMOS circuits Technol Meet.,95

[4] Hirdaya Narain Mishra and Yashwanta Kumar Patel. 2010 Design, Simulation and Characterization of Memory Cell Array for Low Power SRAM using 90nm CMOS Technology. IEEE.

[5] S. M. Kang and Y. Leblebici. 2003 CMOS Digital Integrated Circuits, Analysis and Design. McGraw-Hill, New York.

[6] H. Kawaguchi, K. Nose, and T. Sakurai. 2000 A super cut-off CMOS (SCCMOS) scheme for 0.5 V supply voltage with picoampere stand-by current. IEEE J. Solid-State Circuits (Oct. 2000), vol. 35, no. 10, pp. 1498–1501.

[7] K Itoh, Katsro Sasaki and Yoshinobu Nakagome. 1995 Trends in Low- Power RAM circuit technologies. IEEE (April 1995) Vol. 83, No. 4.

[8] Zhiyu Liu and Volkan Kursun. 2008 Characterization of a Novel Nine-Transistor SRAM Cell. IEEE Trans. on VLSI systems (April 2008) VOL. 16, NO. 4.

[9] Kavita Khare, Nilay Khare, Vijendra Kumar Kulhade and Pallavi Deshpande,. 2008 VLSI design and analysis of low power 6T SRAM cell using Cadence tool. IEEE Proc., 117- 121.

[10] Evelyn Grossar, Michele Stucchi, Karen Maex and Wim Dehaene. 2006 Read stability and write ability of SRAM cells for Nanometer Technologies. IEEE Journal of solid state circuits (Nov 2006), Vol. 41, No. 11.

[11] Henry Park and Chih Kong Ken Yang. 2013 Stability estimation of 6T SRAM cell using a nonlinear regression", IEEE Trans. On very large scale integration (VLSI) systems.

[12] H. Nambu, et al. 1995 A 0.65ns, 72-kb ECL CMOS RAM macro for a 1 Mb SRAM., IEEE J. Solid state circuits, Vol. 30, No. 4, 491-499.

[13] Amrutur, B. and Horowitz, M. 1994 Techniques to Reduce Power in Fast Wide Memories. Proc. Symp. Low Power Electronics, October, 92-3.

[14] Masataka Matsui, Hiroshi Momose, Yukihiro Urakawa, and et. al. 1989 An 8ns 1Mb ECL BiCMOS SRAM", IEEE International Solid-state Circuits Conference.

[15] Nobuo Tamba. 1994 A 1.5-ns 256-kb BiCMOS SRAM with 60-ps 11-K Logic Gates. IEEE JOURNAL OF SOLID-STATE CIRCUITS (Nov 1994), VOL. 29, NO. 1, 1344 to 1352.

[16] Sheriff ATawfik and Volkan Kursun. 2008 Low power and robust 7T dual V_t SRAM circuit. IEEE, 1452 to 145.