High PSRR Full On-Chip CMOS Low Dropout Voltage Regulator for Wireless Applications

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ABSTRACT
This paper presents a high PSRR full on-chip and area efficient low dropout voltage regulator (LDO), exploiting the nested miller compensation technique with active capacitor (NMCAC) to eliminate the external capacitor. A novel technique is used to boost the important characteristic for wireless applications regulators PSRR. The idea is applied to stabilize the Low dropout regulator. The proposed regulator LDO works with a supply voltage as low as 1.8 V and provides a load current of 50 mA with a dropout voltage of 200 mV. It is designed in 0.18 µm CMOS technology and the active area on chip measures 241×187 μm^2. Simulation results show that the PSR of LDO is -60 dB at a frequency of 60 KHz and -41.7 dB at a frequency of 1 MHz.

Keyword
Low Dropout Regulator (LDO); MOSCAP; NMCAC; active feedback; high PSR; system on chip.

1. INTRODUCTION
Over the last decade, power management in integrated circuits has become an increasingly important design consideration for numerous products, especially those relying on battery power. Complicating the power management situation, as more features get integrated into products, the number of required voltage supplies increase. Utilizing multiple local on-chip voltage regulators is a very promising approach in system-on-chip development [1], [3]. Especially, where the power consumption reduction is required, the latest generation of low drop-out linear regulators(LDO) offer the optimal answer for powering circuitry in many of the portable device applications such as cell phones, PDAs, pagers, notebooks, cameras and other handheld portable systems. In fact, they can provide regulated and accurate supply voltages for noise-sensitive analog blocks, and they are often arranged in series to switch regulators to remove the inherent noise produced by the switching activity [5, 8]. This advantage makes LDO widely used in portable systems, especially in RF circuitry to increase battery life and reject the ripple in supply voltage of different RF circuits.

In conventional LDO, as shown in fig.1, a large off-chip capacitor (0.47 µF to 4.7 µF) at output is necessary to locate the dominant pole at very low frequency to achieve the frequency compensation and provide a good dynamic performance [1], 2, 4, 9]. The large off-chip capacitor occupies a large chip area, and it is difficult to integrate multiple LDOs on a single chip. In order to design a full on-chip LDO regulator, the number of compensating capacitors must be minimized [3, 6], and [8].

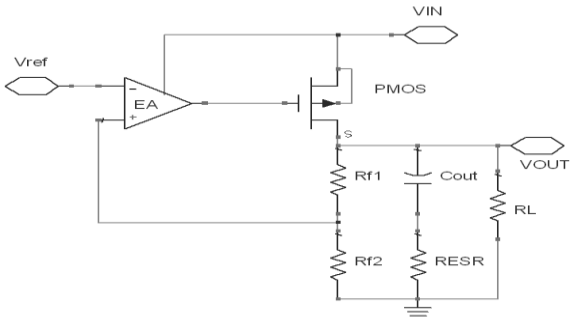


Figure. 1. Schematic of conventional CMOS LDO

Different methods have been introduced recently to improve the performance of full on-chip LDO. The nested Miller compensation (NMC) technique presented in [4] has a trade-off between the dc loop gain and damping factor. In [5], the proposed LDO utilize the NMCAR technique to control the damping factor and the non-dominant complex poles. The regulator is based on a multistage amplifier, and provides an output voltage of 1.8 V, a maximum output current of 150 mA and 108 mV of line regulation; however, the overshoot at the output of LDO proposed in [5] is too large (900 mV) at no load capacitance, and the settling time is about 5 µs. It is not recommended for SoC applications. In [7], the proposed structure achieves a good stability, a high dc loop gain, but problems still remain in this design. The overshoot is about 350 mV, the PSRR at 20 KHz is -35 dB in case this regulator is implemented to supply the wireless system on-chip and the ripple rejection is not good. Moreover, the complicated Miller frequency compensation is needed [7]. In [8], a small on- chip capacitor (30 pF) stabilizes the proposed design with a good phase margin, but at the expense of the low dc-gain and low PSRR (power supply rejection ratio).

To avoid these constraints, one of the possible solutions is the use of MOS capacitor [15]. In this approach, the gate oxide is thin compared to MIMs. CMOS capacitors called MOSCAPs have larger capacitance per unit area [15, 16]. The main problem in largely used MOSCAPs in analog applications is due to linearity issues. This is because of different regions of MOSFET experiences when its gate-bulk voltage varies. For small bias voltages, the transistor is working in depletion region, thereby leaving the capacitor a function of the gate-bulk voltage. This degrades overall performance and mostly adds complexity to the design of analog circuits [6, 7]. In the saturation region of CMOS transistor, the variation capacitance of the MOSCAP with a VBS=0 is neglected [15, 16].

In this paper, we present a modified NMC with a NMOS gain stage at PMOS transistor gate to charge rapidly the gate power

PMOS capacitance and improve high PSRR. The CMOS capacitor (MOSCAP) is used as a miller capacitor instead of MIMs (Metal-Insulator-Metal) capacitors or MOM (Metal-Oxide-Metal) capacitors to reduce the area occupied by the Miller capacitance without influencing stability and realize the full on-chip capacitor LDO. Also, an active resistor feedback is used to reduce more chip area and improve power efficiency.

2. PROPOSED LDO

The proposed LDO, shown in Fig. 2(a), is composed of two gain stages, a power PMOS transistor and the feedback resistor network. The first stage is the error amplifier (EA). The second is a NMOS gain stage. Cm1, Cm2 are the on-chip active MOS capacitances. Rf1 and Rf2 construct the active feedback resistive network. RL and CL model the equivalent load resistance and load capacitance at the output of LDO. CL is the interconnection lines parasitic capacitor, and typically up to 100 pF. The n-well resistor has a high value for its voltage coefficient, which affect the accuracy in the ICs [15]. Weak inversion region MOS transistors are used as a feedback network resistor instead of conventional n-well resistors in order to lowers quiescent current and save silicon area.

1.1. Error Amplifier

The design of error amplifier (EA) is more complex, when a high performance is required to guarantee the stability and transient response, a specific topology is necessary. To move the dominant pole at the output of E.A to low frequencies, low output impedance is designed. To charge rapidly the capacitance seen at the gate of pass transistor (may be as large as 50 pF), EA must provide a sufficient output current [9, 10]. On the contrary, the EA itself should provide very low power dissipation, and its bias currents must be kept as low as possible. In this paper, the proposed EA is the folded cascode amplifier which offers better performances such as high gain, enough load current to drive the power transistor PMOS and improved PSRR characteristic of LDO.

1.2. MOSCAP compensation network

In the full on-chip LDO, the load capacitor modelled at drain of pass transistor is determined by the interconnection lines and typically up to 100 pF. This capacitive value is too small to set a dominant pole at the output node of on-chip LDO [9, 11, and 12]. Therefore, the compensation must be achieved through the miller effect. In [18], the Miller compensation technique is applied to compensate a two-stage Op Amp. As a result, the dominant pole is placed at the output of first stage and moved to low frequencies. The second pole is moved away from the origin of the complex frequency plane. Due to the feedforward path through the Miller capacitor, an undesirable zero occurs on the positive real axis of the complex frequency plane. Another technique used in [18] to remove the zero resulting from feedforward through the compensation capacitance is to insert a nulling resistor in series with a Miller capacitor. In this technique, the nulling resistor must be set equal to the inverse of output transconductance of the second stage to remove the RHP zero. The problem is while there is a fast variation in output load current, the transconductance of gain stage increases. In this case, it is difficult to design the cancelation technique of the RHP zero. With this approach, to ensure a phase margin about 60°, the output pole must be placed about 2.2 times higher than GB. As a result, the ratio of load capacitor and compensation capacitor must be greater than 0.22. These approaches require a large compensation capacitor and a high gain of second stage to ensure stability. Moreover, it is difficult to integrate a large capacitor on-chip LDO.

In the recent design of the system on-chip applications, it is very desirable to integrate the analog portion of a large mixed-signal system in standard digital CMOS technologies with no analog features. However, in order to implement constant capacitors for analog applications, a second poly or extra metal layers are introduced into the process, resulting in significant increase in fabrication cost. Furthermore, although available metal layers in mixed-signal technologies can be utilized for MOM (metal-oxide-metal) capacitors, due to the relatively lower scaling rate of the oxide between these layers, the occupied physical area is noticeable [13]. To avoid these constraints, one of the possible solutions is to employ the MOS gate junctions as capacitor. The problem with exploiting MOSCAPs in analog applications is due to the linearity issues [15].This is because of different regions a MOSFET experiences when its gate-bulk voltage varies.

In the proposed structure, the gate-bulk voltage of MOSCAP is controlled and determined by the designer as demonstrated in eq. (2). The MOSCAP is working in the accumulation region, where the capacitance is not dependent on the gate –bulk voltage.

The DC potential at the gate and bulk of MOSCAP C_{m1} are given by

$$V_{gcm1} = \frac{1}{\lambda_N}\left(\frac{B_2}{B_1}\frac{\beta_{14}}{\beta_4} - 1\right),$$

$$V_{bcm1} = V_{out},$$

$$V_{gbcm1} = \frac{1}{\lambda_N}\left(\frac{2B_2}{B_1}\frac{\beta_{14}}{\beta_4} - 1\right) - V_{out} \quad (1)$$

For keeping the value of capacitor C_{m2} independent to its gate-bulk voltage, the following condition must be respected by the designer.

$$\lambda_N\left(V_{out} + 0.74\right) \geq \left(2 * \frac{B_2}{B_1}\frac{\beta_{14}}{\beta_4} - 1\right) \quad (2)$$

Same as in eq. (2), the gate-bulk voltage of compensation capacitor C_{m2} is controlled by the following condition

$$\lambda_N\left(V_{out} + 0.74\right) \geq \left(2 * \frac{B_3}{B_2}\frac{\beta_{12}}{\beta_{11}} - 1\right) \quad (3)$$

Where B1, B2 and B3 are the current gain of current mirrors M4-M14 and M17-M18 respectively and β4, β11, β12 and β14 are the transconductance parameters of transistors M4, M11, M12 an M14 respectively. Ibias is the start-up current of the circuit. From eq. (2), the gate-bulk voltage is independent of the load in the regulation mode. In the worst case, when Iload increases instantaneously, from eq. (2), the bulk voltage of pass element drops in time or the load capacitor C_L and compensation capacitor MOSCAP dischargers to supply the extra current demanded at the output. As a result, the current gain of current mirror M4-M14 is decreased and the gate voltage of MOSCAP drops verifying the condition of the gate-bulk voltage V_{gbcm1} >0.74V as given in eq. (2).

The problem of this technique remains when the supply voltage drops under 1.2 V.

1.3. Stability analysis

The compensation technique used in this structure places the dominant pole at low frequencies and moves the parasitic poles to high frequencies. The LHP zero is created by the compensation capacitance and improves the phase margin in time when the RHP zero is placed at high frequencies. The small signal of the proposed LDO is in Fig. 2(b). g_{mp}, g_{m2}, g_{ma}, g_{m6}, g_{m8}, g_{m10} and g_{m13} represent the transconductance of transistors MP, M2, Ma, M6, M8, M10 and M13 respectively. g_{dsp}, g_{ds2}, g_{ds4} and g_{ds13} represent the conductance of transistors MP, M2, M4 and M13 respectively. r_p, r_{ds2}, r_{ds4}, r_{ds6}, r_{ds8} and r_{ds10} are the resistance of transistors MP, M2, M4, M6, M8 and M10, respectively. C1, C2, R_{O1} and R_{O2} are the output capacitors and resistors of EA and NMOS gain stage. Assuming that gma<<g_{mp}, and C_{m1}, Cm2 and C_L>>C_I, C_{EA}, the small signal loop gain is given by.

$$T(s)=T(0)*\frac{\left(1+b_1S+b_2S^2\right)}{\left(1+\left(S/p_{-3dB}\right)\right)\left(1+a_1S+a_2S^2\right)} \quad (4)$$

$$T(0)=g_{m2}g_{m13}g_{mp}R_{O1}R_{O2}R_{OUT}\left(R_{F1}/R_{F1}+R_{F2}\right) \quad (5)$$

Where the dominant pole is at

$$p_{-3dB}=\frac{1}{g_{m2}g_{mp}R_{o1}R_{o2}R_{OUT}C_{m1}} \quad (6)$$

And

$$b_1=C_{m2}/g_{ma},\quad b_1=-C_{m1}C_{m2}/g_{m2}g_{mp}$$

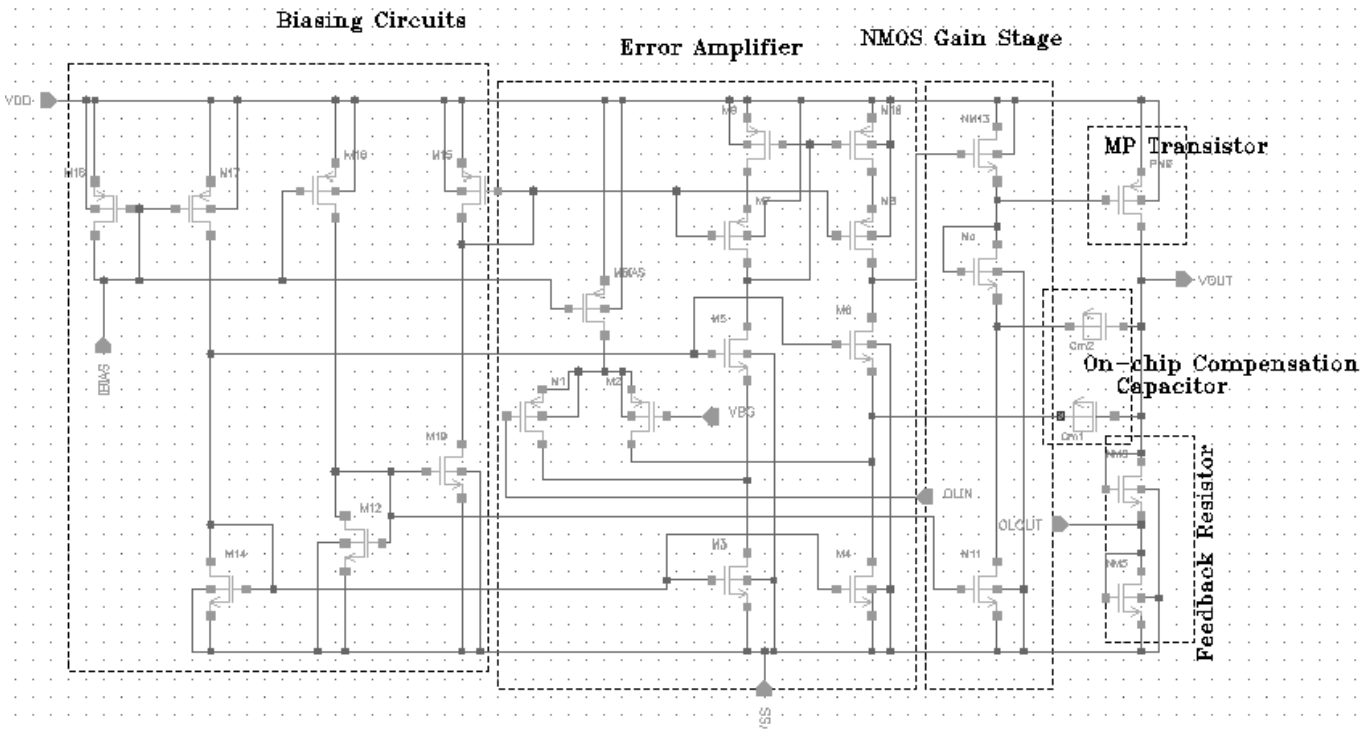
$$a_1=R_LC_L+C_{m2}\left(1/g_{m2}+1/g_{ma}\right),$$

$$a_2=C_{m2}C_L/g_{m2}g_{mp} \quad (7)$$

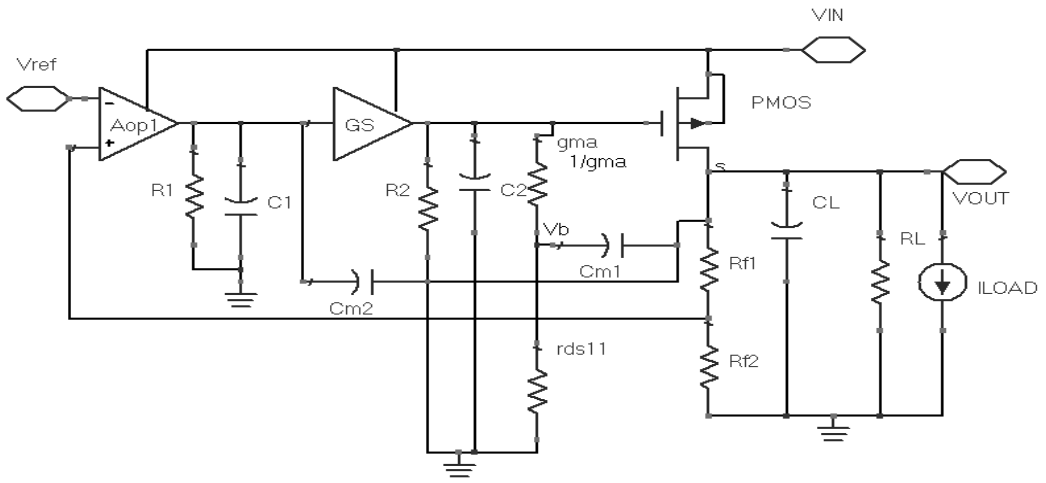
Assuming that g_{ma} is small and the non-dominant poles are widely spaced, then the roots of the second-order polynomial in the denominator in eq. (4) are rewritten as

$$P_{nd1}\approx-\frac{1}{R_LC_L+C_{m2}\left(\frac{1}{g_{m2}}+\frac{1}{g_{ma}}\right)}$$

$$p_{nd2}\approx\frac{g_{mp}}{C_{m2}} \quad (8)$$



a)



b)

Figure. 2. Proposed LDO a) schematic of CMOS LDO b) small signal of proposed LDO

In the NMCAC LDO, the dominant pole is unchanged, but the non-dominant poles are pushed to high frequencies. From the polynomial in the numerator of eq. (4) and assuming that the approximation in eq. (7) the two zero are expressed as

$$Z_{LHP} \approx -\frac{g_{ma}}{C_{m2}},$$

$$Z_{RHP} = \frac{g_{m2}g_{mp}}{g_{ma}C_{m1}} \approx \frac{g_{mp}}{C_{m1}} \qquad (9)$$

Increasing the load current, the RHP zero and non-dominant pole formed at the output of LDO move to higher frequencies, while the LHP zero is independent of the load current and moved to high frequencies by increasing the current in the NMOS gate stage. From Eq. (7, 9), the damping factor is derived as

$$\zeta = \frac{1}{2}\left(R_L C_L + C_{m2}/g_{m2} + C_{m2}/g_{ma} \right)\sqrt{\frac{g_{m2}g_{mp}}{c_{m2}c_L}} \qquad (10)$$

In the NMCACR LDO, a small g_{ma} enhances the damping factor without influencing the dc loop gain and without increasing C_{m2}. the damping factor is controlled by g_{ma} instead of gm2. From eq. (17) with $(W/L)_a$=5, the Z_{LHP} is placed at 11MHz as presented in fig. 4.

1.4. Power supply rejection ratio

Power supply rejection is the LDO ability to suppress power supply noise from its output. Recently, there is a lot of focus on designing high performance, especially low noise and high PSRR. Moreover, the integration level of power management is proportionally increased in time or the dimension of process is decreased rapidly and the parasitic capacitances are up to ten pF. In addition, the compensation capacitor drops to a few pF (0.18 pF) in [13]. In [16], a full on-chip LDO is realized using novel technique to boost the PSRR to -37 dB at 1 MHz. Furthermore, most literature focus in analytic of PSRR on parameters and devices transmit and control the ripple from the supply to the output on the PMOS parasitic capacitance neglecting the effect of the parasitic capacitances at the output of error amplifier and its high output stage gain. In this work, the error amplifier is a three gain stage, and the parasitic capacitance is in order of ten fF (about 50 fF). In this analysis, all sources of perturbation are taken into consideration and a new technique is proposed to boost and control the PSRR. The PSRR performance can be achieved with the insertion of NMOS gain stage at the output of EA. The small signal model of PSRR is shown in fig. 3. A small signal input voltage v_{dd} will induce an output voltage v_{out}. The PSRR can be seen to be

$$PSRR = \frac{\left(g_{mp} - g_{dsp}\right)\left(A_p + SC_p\right) - \left(g_{dsp} + SC_c\right)\left(g_{ds13} + SC_{gsp}\right)}{a_0\left(1 + a_1S^1 + a_2S^2 + a_3S^3\right)} \qquad (11)$$

Where

$$A_p = g_{m13} + g_{ds13} + g_{ma}\left(1 - A_{c2}\right),$$

$$C_p = C_{gs13} + C_{gsp} + C_{gdp},$$

$$C_c = A_{c2}C_{m2} + C_{gdp},$$

$$A_{c2} = \frac{r_{ds11}g_{ma}}{1 + r_{ds11}g_{ma}}, \quad A_{EA} = \frac{2+k}{1+k} * g_{m2} * R_{oA},$$

$$R_{OEA} = R_{II} \,//\left[g_{m6}r_{ds6} * \left(r_{ds4} \,//\, r_{ds2}\right)\right],$$

$$R_{II} = g_{m8}r_{ds8}r_{ds10}, \; k = \frac{R_{II}\left(g_{ds2} + g_{ds4}\right)}{g_{m6}r_{ds6}} \qquad (12)$$

And

$$a_0 = g_{mp}A_{EA}g_{m13} - R_L\left(g_{m13} + g_{ds13} + g_{ma}\left(1 - A_{c2}\right)\right),$$

$$a_3 = \frac{R_L C_L \left(\begin{matrix} C_C C_{AP} - \\ \left(C_{gdp} + C_{m2} + \left(1 - A_2 A_{EA}\right) C_{m1} C_P \right) \end{matrix} \right)}{a_0},$$

$$a_1 = \frac{\begin{matrix} g_{mp} g_{m13} A_{EA} R_L C_L + g_{mp} C_{AP} + AC_C \\ -\left(R_L g_{dsp} C_L + C_{gdp} + C_{m2} + \left(1 - A_2 A_{EA}\right) C_{m1} \right) A_p \\ - R_L \left(C_{gs13} + C_{gsp} + C_{gdp} \right) \end{matrix}}{a_0},$$

$$a_2 = \frac{R_L C_L \left[\left(\begin{matrix} \left(g_{mp} C_{AP} + AC_c \right) \\ -\left(\begin{matrix} C_{gdp} + C_{m2} + \\ \left(1 - A_2 A_{EA}\right) C_{m1} \end{matrix} \right) A_p \\ - g_{dsp} C_p \end{matrix} \right) \right] + C_c C_{AP}}{a_0} \quad (13)$$

Where

$$A_2 = \frac{r_{ds4} // r_{ds2}}{r_{ds4} // r_{ds2} + R_B},$$

And

$$R_B = \frac{R_{II}}{g_{m6} r_{ds6}},$$

$$R_{II} = g_{m8} r_{ds8} r_{ds10} \quad (14)$$

Assuming that $A_{EA} >> R_L$, gm_{13}, the dc gain of PSRR can be expressed as

$$PSRR|_{DC} \approx \frac{\left(g_{mp} - g_{dsp}\right) A_p - g_{dsp} g_{ds13}}{g_{mp} A_{EA} g_{m13}} \quad (15)$$

As can be seen from eq. (15), the dc gain of PSRR is controlled by the NMOS gain stage performance. At low frequency, in low load condition, g_{mp} decreases, and also the gain of EA decreases.

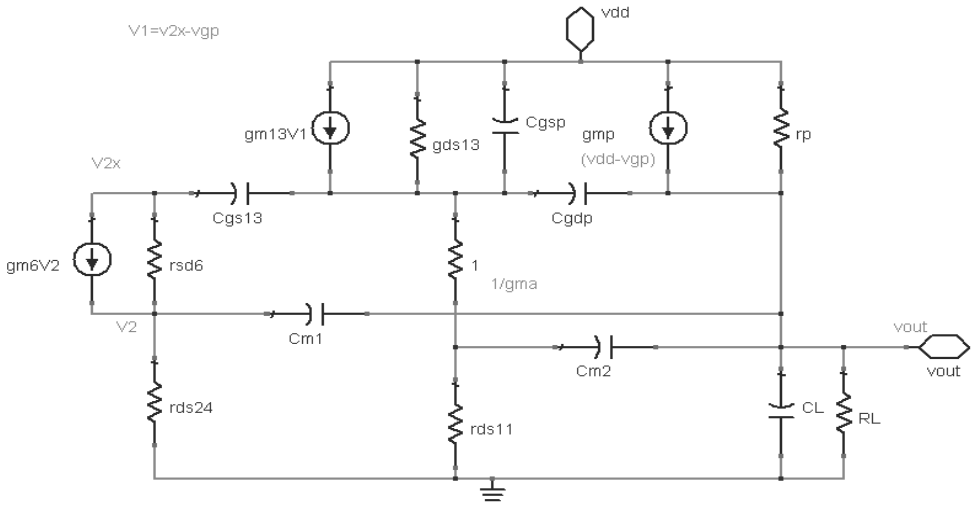


Figure. 3. Small signal model of PSRR

From eq. (15), g_{mp} in numerator and denominator hence $PSRR|_{DC}$ is not heavily affected by the transconductance variation of power transistor and is controlled by the gain of M13 and Ma. At full load condition, an increase in g_{mp} and gain of EA, enhance the $PSRR|_{DC}$ as given in eq. (15). In case of having the gate of MP transistor connected to the output of the EA without the NMOS gain stage as in [16]; $PSRR|_{DC}$ can be expressed as:

$$PSRR|_{DC} \approx \frac{g_{mp}}{R_L} \quad (16)$$

As the load current decreases, also the transconductance of MP decreases, the gain of PSRR and the performance of LDO is affected.

In case of having a PMOS gain stage at output of EA as in [17]. The transconductance ratio of the NMOS active inverter at gate power transistor is about 1 for the stability conditions. The PSRR is enhanced only by the open loop gain.

From eq. (11), the PSRR drops at two breakpoints Z_1 and Z_2. Assuming that $Z_1 << Z_2$, $g_{ds13} << g_{mp}$, Cp is about 24 pF and Cc is about 15 pF, at moderate frequency, the degradation gain of PSRR is starting at breakpoint zero (Z_1) and given by:

$$Z_1 = \frac{-A_p}{C_P} \qquad (17)$$

And

$$Z_2 = \frac{g_{mp}C_p - g_{ds13}C_c - g_{dsp}C_{gsp}}{C_c C_{gsp}} \qquad (18)$$

From eq. (17), the first break point Z_1 at moderate frequency is not influenced by different load conditions and can be pushed to high frequency by increasing the transconductance of transistor M_{13} M_a, or decreasing the gain of divider NMOS Ma-M11 at gate Power PMOS transistor. As can be seen from eq. (18), the negative time constant formed by C_{m2} and C_{gsp} is subtracted from the time of the second zero. Consequently, the second zero moves to higher frequencies resulting in higher roll-off PSRR.

1.5. Transient response analysis

In load regulation, when the load current suddenly steps from low load to its maximum value, the incapability of the pass transistor to provide the demanded current forces the load capacitor to supply the extra current and the capacitor voltage drops. The active feedback transmits the variation in output voltage of LDO to the EA which in turn downs the gate voltage of the pass element, thus increasing V_{SGP} and providing the output current demanded by the output load. In this structure, the compensation capacitor forms the feed-forward path to inject charges in the load capacitor and decreases the drop of output voltage. The injection of the charges stored in the capacitors C_{m1}, C_{m2}, C_{gdp} and C_L is expressed as

$$i_{out} = i_{MP} + i_{CL} + i_{Cm1} + i_{Cm2} - i_R \qquad (19)$$

i_R is the leakage current in load resistance.

From eq. (18), the different capacitors contribute to provide the required current I_{LOAD} by the output load at ac load transient and the drop of the output voltage of LDO will be small. Moreover, when the load current decreases instantaneously, the over current of the power PMOS transistor charges the all capacitors at output of LDO. As a result, the overshoot of the output voltage will be small.

In the line regulation, the ripple on the power supply is transmitted to the output in conventional LDO by a miller capacitor and gate drain parasitic capacitor of power PMOS. In the proposed design, the variation in the supply voltage increases the output impedance of the NMOS gain stage at the gate of power transistor. As a result, the path from gate MP to the output of LDO is almost turned off at low frequency. This result is improved by the high PSRR of the proposed LDO.

3. SIMULATION RESULTS

The proposed regulator LDO has been realized in 0.18 µm CMOS technology. The layout of the IC LDO is shown in Fig. 9 with an active chip area of 241 µm×187 µm, which is dominated by Power MOS transistor. The on-chip MOS capacitors occupy a small area on chip. The simulation of the proposed LDO was performed with Spectre. The loop-gain simulation has been performed with a total on-chip compensation capacitor C_{total}=24 pF, and the output capacitor C_L (up to 100 pF). The proposed LDO is stable with a good phase margin of approximately 82° at full load as shown in Fig. 4. At low load, the loop's gain drops to the low value of -39 dB and a phase margin is of 67°.

Fig. 5, Shows the simulation of PSRR at 50 mA load current. The impedance inserted at the gate of power MOS transistor by the NMOS gain stage and transistor M_a enhances the PSRR, and its value is -60 dB in the range of [0-60KHz]. As depicted in Fig. 5, when a simple NMOS gain stage is inserted at gate of power transistor the PSRR at 1 MHz is about -34 dB and when the novel technique is applied the PSRR at 1MHz is -41.7 dB.

The line regulation simulation of the proposed LDO is shown in Fig. 6. Fig 6(a) shows the AC line regulation for supply voltage change from 2 to 2.5 V. The AC line regulation is about 4 mV with a settling time of 2 µs. Fig 6(b) shows the transient response simulation of the proposed LDO with load current switching between 100 µA and 50 mA. The variation of output is about 110 mV with a settling time of 3 µs for 0.005% accuracy.

Another important characteristic of LDO is the DC load regulation as shown in Fig. 8(b), when the load current goes from 0 mA to 50 mA, the variation of the output voltage is 0.6 mV/mA. In the worst case (Load current increases from 0 to 50 mA), the output voltage variation is about 67 mV.

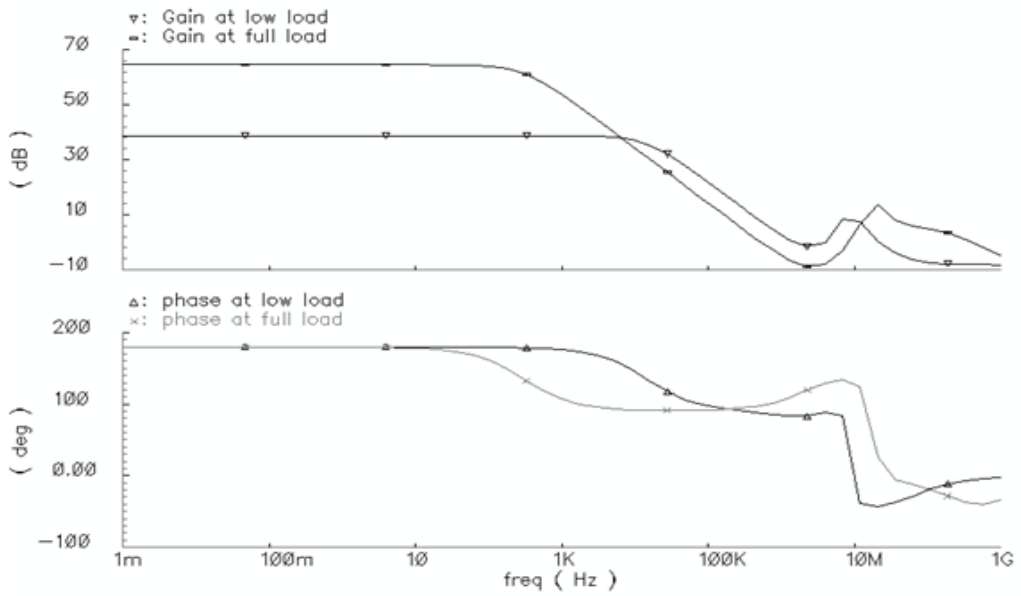


Figure 4. Simulated results of proposed LDO frequency response.

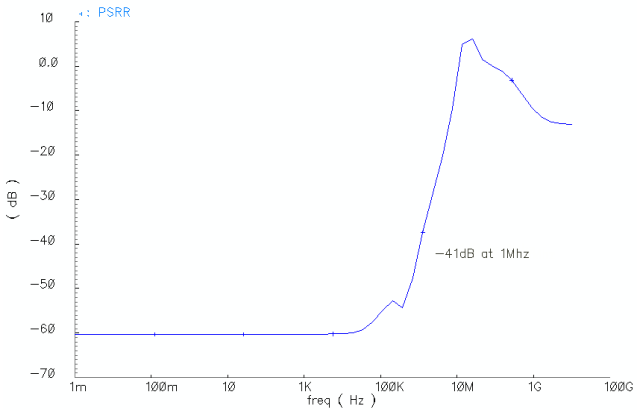
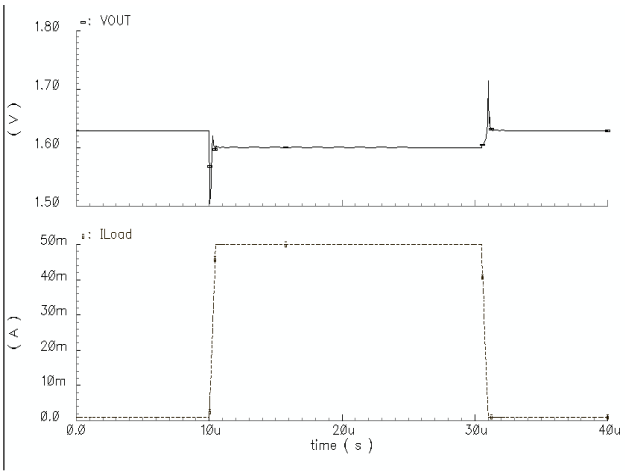
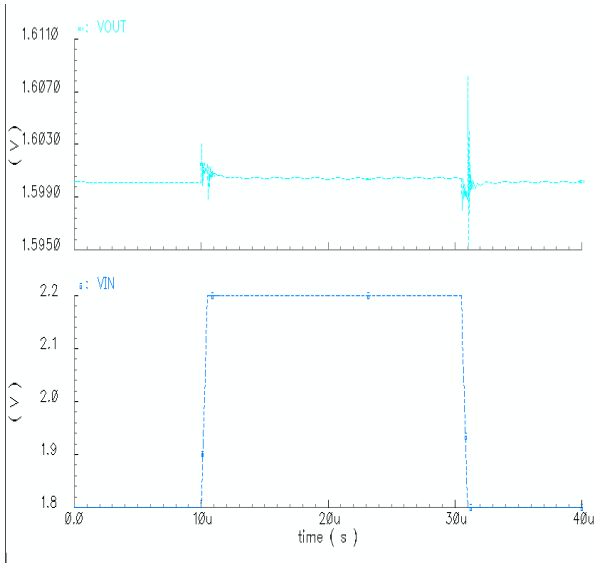


Figure 5. Simulated PSRR performance of the full on-chip LDO.



b)

Figure 6. Transient response of proposed LDO a) AC line regulation b) AC load regulation.



a)

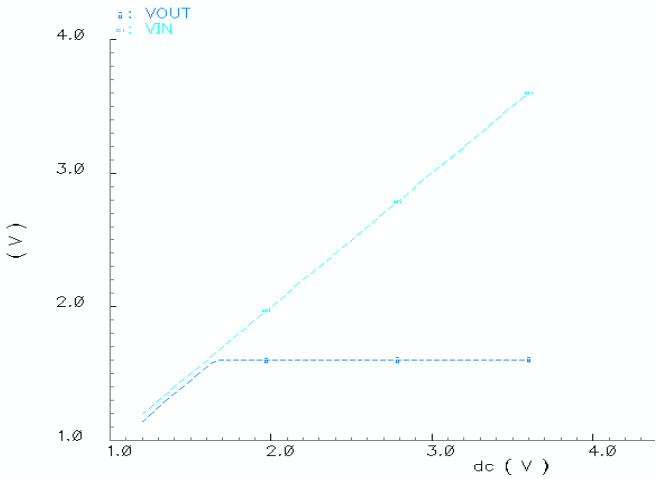


Fig. 7. Simulated of DC line regulation.

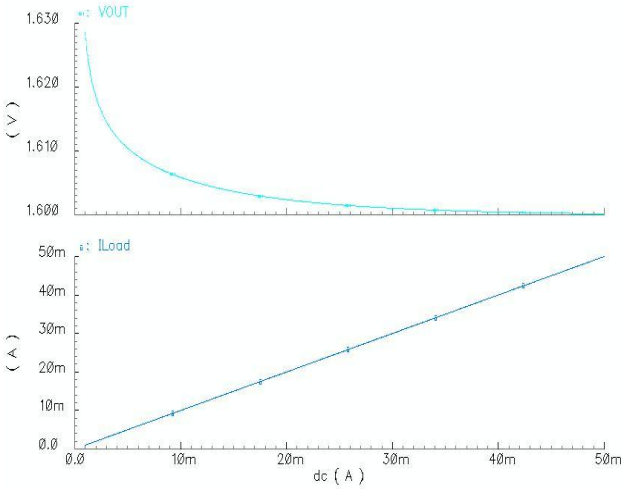


Figure 8. Simulated of DC line regulation.

Fig. 9. Layout of the proposed full on-chip CMOS LDO

Table 1.Performances and comparison with other works

Parameter	[8]	[14]	[16]	This work
CMOS Technology (µm)	0.35	0.35	0.18	0.18
VIN (V)	2-3.3	2.1	1.2-1.5	1.8-3.6
VOUT (V)	1.8	1.8	1	1.6
Drop-out (mV)	200	N/A	300	200
Compensation (pF) Cap	N/A	0.18	41	24
ILmax (mA)	60	50	50	50
Line regulation (mV/mA)	-13.1	NA	0.024%	0.26
Load regulation (mV/mA)	-1.05	0.45	0.7 mV/4 mA	0.6
Settling time (µs)	<10	N/A	1.6	2 (ACLN[1]) 3 (ACLD[2])
PSSR(dB)	<41	-58.7 @10Hz -20 @1MHz	-70 @ 1 KHz -37 @ 1 MHz	-60.4 @100 Hz -42 @1MHz
Active chip area (mm^2)	0.07	0.108	0.1044	0.045

1. AC line regulation
2 AC load regulation

4. CONCLUSION

In this paper, a full on chip CMOS LDO using a modified NMC technique has been presented. The regulator circuit design features an active compensation technique, which guarantees the stability through the full load current rage with high PSRR of -60 dB up to 100 KHz and -42 dB at 1MHz. The high performance is independent of the off-chip capacitor. The detailed analysis of the proposed structure is revealed to justify the performance of the technique utilized. The simulations prove the results theory.

The proposed LDO is capable of providing 50 mA with a drop-out voltage of 200 mV at VDD of 1.8 V. The stability is achieved by using the MOSCAP compensation capacitor in the accumulation region. The active area is reduced by 40 % compared to the state-of the-art designs using technologies with the same feature size. The proposed regulator is mainly used as a regulating power source for wireless applications, RFID and charge pumps.

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