Design of wide band Low Noise Amplifier for Antenna Testing System

Muhammad AsifZakariyya
SPEC Energy DMCC, Islamabad, Pakistan

Farman Ullah
Department of Electrical Engineering COMSATS Institute of Information Technology, Wah, Pakistan

Muhammad Farhan
University of Science and Technology, Bannu, Pakistan

1. ABSTRACT

A low Noise amplifier is an extraordinary family member of electronic amplifiers used frequently in the field of wireless communication systems. In case of wireless systems, the core task of LNA is to capture the received signal directly from the antenna and amplify this weak noisy signal in such a manner that its noise level is minimized to a certain threshold. In other words, gain of the amplifier is assumed to be kept to a certain desirable level in order to maintain lowest possible noise figure thus enabling enhanced spectrum for the support of wireless infrastructure.

KEYWORDS

LNA, Wide band, Antenna Testing System (ATS), data rate, SNR

2. INTRODUCTION

Noise is the major limiting factor in a typical communication system. Almost every fundamental parameter like coverage, data rate, capacity etc. depends upon the system capability to eliminate noise from the received signal. A signal propagating through a wireless medium confronts two major problems. The first being free space loss that is the decay of the signal energy density while it travels away from the transmitter. Second being the addition of noise and interference effect which is also a kind of noise or disruption, caused due to external sources of noise whose origin is outside the receiver circuitry. For better and reliable
communication it becomes essential to remove or minimize this addition of noise which tends to corrupt the information signal. Not only the quality of the received data gets affected by this corruption of signal, the data rates also get limited.
The rapid increasing popularity of wide band (0.3 – 3 GHz) and ultra wide band (3.1 - 10.6 GHz) applications has augmented the demand for manufacturing low cost but high performance low noise amplifiers (LNA). Wide band Low Noise Amplifier is vital component in many high data rate and wide band applications including optical sensors (<960 MHz) [18], Pulsed RADARs (200–1000MHz,1.2GHz-14 GHz,2 – 4GHz) [18-19], Satellites systems (950- 2150MHz), analog cable systems (50MHz – 850MHz), terrestrial television broadcasting networks (450-850MHz), cellular communication base stations(900MHz-2.4GHz) and software defined Radios etc. The major advantage of wide band Low noise amplifier over narrow band is that the former can replace several narrow band LC tuned low noise amplifiers in multi standard narrow band receivers[18]. This results in drastic reduction in cost manufacturing and circuit complexity. A wide band utilization also reduces the chip area and number of input and output pins if it is implemented in chip technology standard. Wireless wideband communication systems for Gbits/sec data rates, either regulated or not by the international standards, are going to be the centre of research and development in future.
The work will focus on design and fabrication of a high performance, low cost highly efficient wide band low noise amplifier for antenna testing systems. The operating frequency for this design is set at 5 GHZ. ATF58143, a low noise enhancement mode Pseudo morphic HEMT transistor IC in a surface mount plastic package will be used.

Excellent noise suppression, reasonable gain and achievability of high linearity make it most appropriate for cellular systems, PCSand WCDMA wireless base stations. It is also well suited to other applications like cordless phones systems, wireless local loop applications that require low noise and high linear performance in the operating range of 450 MHz to 6 GHz. [1]

The design methodology will be described in detail in the later design section. The targets are summarized below:

- Required frequency band 1- 5GHz
- Power gain: 8dB. [2]
- Noise figure: optimum noise performance

3. DESIGN METHODOLOGY AND SIMULATION RESULTS

In previous sections we have discussed the performance techniques for minimum low noise design and input matching for low noise performance. The simulator used throughout the course of this work is Agilent ADS 2010-11 version, a more user friendly having a wide range of enhanced design tools.
In this paper we will discuss different steps and procedures that will lead us to the design of Low noise amplifier for optimum noise performance. In the second section we will demonstrate the simulation results obtained during the design.

3.1 Design Methodology

Since the objective of this work is to design a low noise wide band pre amplifier for a typical antenna testing system ,where

the major performance parameter is to obtain the minimum noise figure or in other words better noise performance is desired, whether it is achieved at the cost of losing some gain . in the previous section we have proved this fact mathematically that the gain of the low noise pre amplifier installed in the first stage of the antenna testing system is not affecting the performance of the receiver for a typical antenna testing system. For other cases where different desired parameters like S_{11}, S_{21} and S_{22} are specified then these are achieved by doing some sort of tradeoff between noise performance and gain.

For the design of desired LNA, these essential steps are needed

1. In accordance with the required design objectives ,the very primary step is the selection of transistor ,which is a key component of amplifier circuit .the design objectives may be of various nature like narrow band amplifier ,high gain amplifier, maximum gain amplifier ,low noise design for minimum noise figure or wide band design .since our objective is to get best noise performance over the entire wide band(1-6) GHz so the first task would be the selection of transistor from various transistor families that are fulfilling the requirement. so for this purpose various transistors are sorted out ,which have desired minimum noise figure ,but final selection is performed keeping in view the smallest NF with relatively higher gain compared to its counterparts. For this purpose the data sheets are helpful in providing the brief primary information.
2. Biasing of transistor is performed in order to get the biasing point in the mid-range of Ids vsV_{ds} graph. and required Vgs is calculated.
3. Next task is the measurement of s-parameters at the biasing point obtained in the previous step.
4. After measuring s-parameters the transistor is checked for stability at the specified frequency of operation. For wide band design it is checked for both lowest and highest frequency of the band. I.e. (K>1 , $|\Delta|$ <1) as described in detail in the previous section. if the standard stability conditions are met by transistor then next step will be followed otherwise the stability circles will be drawn in order to estimate the stable regions of operations .
5. For unilateral case where S12=0 , standard unilateral formulas will be used to calculate the source ,device and load gains .for bilateral case where S12 ≠0 ,calculation of unilateral Fig of merit is done, if the amount of error U is small enough to be neglected again same unilateral formulas can be applied otherwise for larger errors bilateral expressions will be used for G_s,G_0,G_L .
6. Compute G_s and G_L that are the allocated gain values for input and output matching networks also it is better to calculate the G_0 ,the transistor gain as well .
7. This time plotting of constant gain circles for source and noise figure circles is performed on the same smith chart
8. The points of interception of different gain circles and noise figure circles will be formed after plotting both types of circles on the same chart. At this stage a suitable point of interception is selected on the gain circle that should be either within or at the noise figure circle which is fulfilling the gain and noise figure requirement of the amplifier. .using this point, the matching network is designed for input side. Input and output matching networks are designed according the requirement of the design nature. Since the work design is for best noise performance over the wide band, in this case, from the next step we will narrate the criteria used for obtaining the minimum noise figure.
9. This point represents the of Γ_S i.e. source reflection coefficient. For minimum noise figure design or best noise performance , Γ_S is taken equal to the of Γ_{opt} i.e. the optimum reflection coefficient of the transistor model ,that is usually given in the data sheet .for output matching the objective is to get best VSWR so matching is performed as

$$\Gamma L = \Gamma^* out = (S22 + \frac{S12S21\Gamma opt}{1-S11\Gamma opt})^*$$

Matching g networks can be designed when the values of Γs and ΓL are known.

3.1.1. Transistor Selection

For LNA design the most important and very first task is the transistor selection on the basis of nature of the design like gain, noise performance or wide band achievement. a transistor should exhibit high gain ,low noise figure at the lowest possible current consumption [3]. While preserving relatively simple impedance matching scheme at the desired frequency of operation. Data sheet of the device can be a good starting point for selection process. Since the design needed in this work is for minimum noise performance in wide band,so the chosen transistor is Agilent ATF58143 p-HEMT transistor. Because of its better low noise performance and high linearity makes it most suitable choice for this work [4]. Its model file was downloaded from Avago technologies website.
Since the design focuses on better noise performance, the biasing points selected from the data sheet were at Vds=3 volts and Ids=30 mA having Fmin =1.04 at 6 GHz frequency as shown in the table obtained from the data sheet [5].

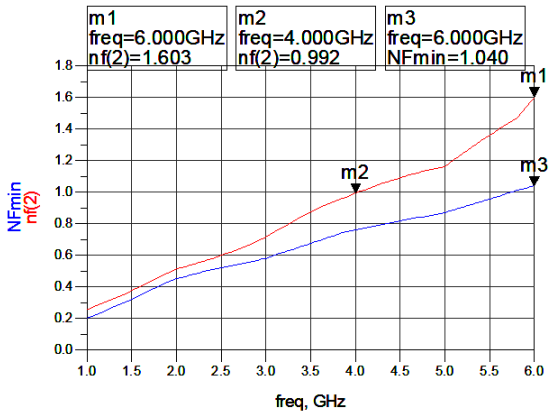

Figure 1: ATF58143 transistor model noise performance to badly matched conditions

Table 1: typical noise parameters of ATF58143 model atVds=3V ,Ids= 30Ma.

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 30 mA

Freq GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	$R_{n/50}$	G_a dB
0.5	0.12	0.39	17.775	0.04	25.33
0.9	0.18	0.37	46.9	0.04	22.26
1.0	0.20	0.36	53.525	0.04	21.54
1.5	0.32	0.32	80	0.04	19.16
1.9	0.43	0.30	101	0.04	17.65
2.0	0.45	0.30	107.7	0.04	17.33
2.4	0.51	0.29	125.2	0.04	16.23
3.0	0.58	0.31	154.475	0.05	14.77
3.9	0.75	0.35	-156.95	0.06	13.39
5.0	0.87	0.42	-120.93	0.09	11.92
5.8	1.01	0.50	-100.83	0.15	11.07
6.0	1.04	0.53	-97.15	0.18	10.93

3.1.2 Finding Bias Conditions

The next step is to calculate s parameters required for the biasing conditions as well as for stability analysis.the bias points must be chosen such that the gain is above that stated in specification whilst the noise figure must be below the specification value [6][7] .S parameter file can also downloaded from Avago website, which contain the measured s –parameter for use in simulations.

In this step the DC bias point of the transistor is checked and analyzed for the design of corresponding DC biased network. Keeping in notice the objectives of this work, the bias points were chosen as Vds=3volts and Ids = 30mA. As this set of values was giving minimum noise figure at 6 GHz ,as stated in the above table adopted from the data sheet of ATA58143 transistor model.

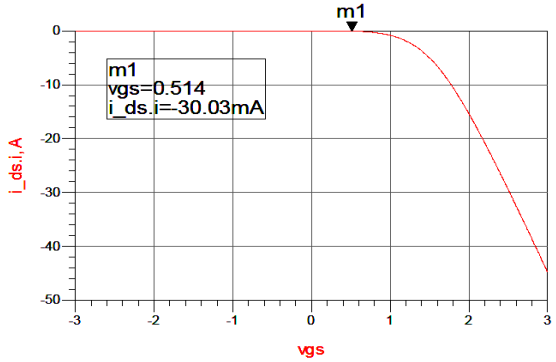

Figure 2: Bias points selection and determination of gate to source voltage

3.1.3 Acquiring S-Parameters for Amplifier

The S-Parameters can be obtained in two different ways. The first option is by using ATF58143 SPICE model to acquire the required s-parameters, but these parameters are not reliable because of their dependence on the bias voltages in the circuit.

The other method which is the better option is to get s-parameters data by using ATF58143 s2p file provided by the Avago and this can be downloaded from Avago website. There are different file components on the website for selected values of Vds and Ids. The file for this work was selected for Ids=30mA and Vds=3 volt. The advantage of using the file is that, it is more accurate because the data comes from physical measurement and ignores the bias condition set [8][9].

S- Parameter analysis made us capable to estimate about the transistor whether it will operate in stable mode or conditional stable mode. Also, noise figure estimation and gain estimations were made on the basis of this analysis. The results of this analysis obtained with the help of ADS are shown in the Fig3. From the analysis it is shown that smith chart and source stability circles have common region, which shows that the circuit is conditionally stable and its stable region of operation is outside the stability circle [10]. Noise figure and source stability circles are plotted together in order to estimate the proper point in the region of operation on which the device may be able to operate on best noise performance.

In order to achieve this point different noise figure circles were drawn by inserting equation in the graph ,these noise figure circles were drawn at 1.3 dB and 1.5 dB close to the minimum noise figure values at 6 GHz as shown in theFig 3.

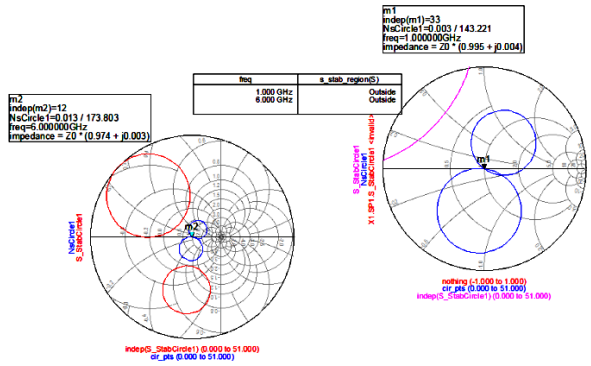

Figure3: Stability Circles and Noise figure Circles at 1 GHz and 6GHz with source stability circle.

Two noise figure circles one at 1.3 db and other at 1.5 db were created and were plotted with source stability circle. In the schematic diagram marker m1 shows the noise figure circle at 1.3 dB, while m3 marker shows the circle at 1.5 dB. Both circles are in the stable region of operation but for wide band the point to be selected is nearer to the centre of the smith chart. In this case noise circle with 1.3 dB was selected for further process in the design of the input and output matching network.

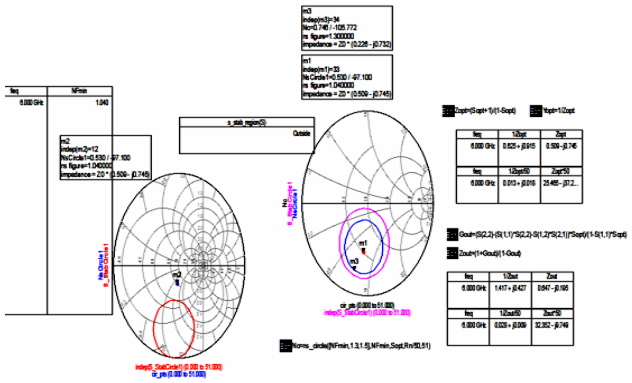

Figure4: Estimation of noise figure by inserting different noise figure circles

3.1.4 Design of Input and Output Matching.

Since the objective of this application is to achieve the better noise performance,the input matching network should be matched for minimum noise while output matching network if conjugately matched will give better VSWR performance with out affecting the noise figure[11]. The following set of equation we employed in the ADS simulator in order to calculate the optimum admittance of the device Y_{opt} and output admittance Y_{out}.Moreover transmission lines are used for both input and output matching of the device[12]. We know that optimum impedance at which the minimum noise figure is obtained is

$$Z_{opt}=(S_{opt}+1)/(1-S_{opt})$$

The location of Y_{opt} or Z_{opt} is quite far from the center of smith chart. Since the value of source impedance which is usually taken 50Ω locates at the center of the smith chart [13]. The optimum noise matching at 6GHz is achieved by rotating the Z_s to transfer it to the Z_{opt}.the normalized value of Z_o=1Ω [14].We can also change it to Y_{opt} which is the reciprocal of Z_{opt} as off set and stub lengths can be easily estimated using admittance smith charts.

For input matching network design, smith charts are used for calculation of input matching network offset length and stub length. For input match, the wavelengths towards the load will be utilized rather than towards the generator. This looking towards the load from the input side is called synthesis usually employed for better noise performance of the amplifying device [15].For output match the transconductance G_{out} is given by

$$G_{out}=(S(2,2)-(S(1,1)*S(2,2)-S(1,2)*S(2,1))*S_{opt})/(1-S(1,1)*S_{opt})$$

And output impedance expression in terms of transconductance is given by

$$Z_{out}=(1+G_{out})/(1-G_{out})$$

And again the reciprocal of equation is Y_{out} i.e. the output admittance. On smith chart this will be conjugately matched to the load, utilizing the wave lengths towards the generator and moving clock wise throughout the smith chart.

The values of Y_{out} and Y_{opt} at 6 GHz , obtained from the s-parameters are shown in the Fig 4. It is then plotted on the admittance smith chart for desired matching network [16][17]. The smith chart plots for length of the stub and offset for both input and output networks are attached in the appendix.

Table 2: input optimum and output admittance for matching network

Eqn Zopt=(Sopt+1)/(1-Sopt) Eqn Yopt=1/Zopt

freq	1/Zopt	Zopt
6.000 GHz	0.625 + j0.915	0.509 - j0.745

freq	1/Zopt/50	Zopt*50
6.000 GHz	0.013 + j0.018	25.465 - j37.250

Eqn Gout=(S(2,2)-(S(1,1)*S(2,2)-S(1,2)*S(2,1))*Sopt)/(1-S(1,1)*Sopt)

Eqn Zout=(1+Gout)/(1-Gout)

freq	1/Zout	Zout
6.000 GHz	1.417 + j0.427	0.647 - j0.195

freq	1/Zout/50	Zout*50
6.000 GHz	0.028 + j0.009	32.352 - j9.749

The stub and off set lengths obtained after plotting the Y_{opt} and Y_{out} on the admittance smith chart the following set of values in terms of transmission line wave length have been calculated below.

For input network
Off Set Length = L_{off}(opt)=0.183 λ
Stub Length =L_{stub}(opt) = 0.35 λ
For output network
Off Set Length = L_{off}(out)=0.155 λ
Stub Length =L_{stub}(out) = 0.074λ

λ is the wave length and W the width of the microstrip transmission line are calculated by using line calculation application in ADS.

From Fig 4, using PTEFE PCB with following specifications

Dielectric constant εr =3.5
Thickness of the di electric H= 0.76mm
Thickness of the conductor T= 35 micro meter
Metal used for micro strip is copper with conductivity Cond =5.8e7
And loss tangent D= 0.0018.
The parameters listed below are called substrate parameters. The wave length λ and width W are determined for full wave length given below
λ = 29.914 mm
W= 1.722 mm
So offset and stub lengths in mili meter (mm) for both input and output matching networks are calculated as

Off Set Length = L_{off}(opt)= 0.183λ =0.183 (29.914) = 5.47mm
Stub Length =L_{stub}(opt) = 0.35 λ = 0.35(29.914) =10.59 mm
For out put network

Off Set Length = L_{off}(out)=0.155 λ =0.155 (29.914) = 4.6mm
Stub Length =L_{stub}(out) = 0.074λ =0.074 (29.914) = 2.21 mm

3.2.5 Line Calculations for Microstrip

The tracks on the PCB acts as a transmission line and when the nature of the design is for high frequencies,then it should be included in the design.PCB length and width of the transmission

line arecalculated in line calculation an easy application in ADS [18].

3.1.5 Amplifier Circuit Design without biasing Circuit

Calculating offsets and stub lengths for both input and output matching networks the amplifier circuit using is constructed in ADS in the new schematic window .the micro wave transmission lines are used for matching network design at both input and out put ends having terminations of magnitude 50 ohm [19].

Matching is performed by inserting single stubs at predetermined off set distances for both matches .the first s para simulations were performed from 1 -6 GHz with a step size of 0.02 GHz with out tuning the matches.The results are shown in

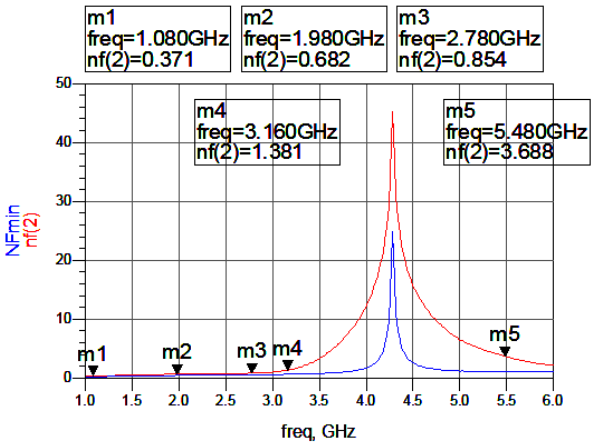

Fig 6for untuned LNA for a step size of 0.02 GHz .the noise performance is excellent from 1- 3.16 GHz band and noise figure of the the amplifier is all around seems comparable with the minimum noise figure of the the transistor but after this, from 3.5- 5.5GHz a drastic rise of the magnitude occurs in both the NFmn and NF of the amlifier.

Figure 6: Noise figure and Fmin plots with out tuning with 0.02 GHz step size

Then the same simulations were run for a step size of 5 GHz wide band and the results were found to be completely smooth through out the entire band from 1-6 GHz.from 1-2.5 GHz the noise figure remained below 1db ,lineary increased through out the band.at this the performance of the design is below what, we were expecting.this may be due to many reasons.

Optimization can also be performed by employing different methods [19]. The first one is to change the variables involved in the componets manually. But usually this is not recommended. Secondly the modification can be achieved by using ADS tuning application which can performs the modificaions automatically and have the ability toupdate the data display. This application is highly recommended [20]. The last option is to use ADS optimization utility for changing the variables .this automatically modies the schematic for the desired outputs.

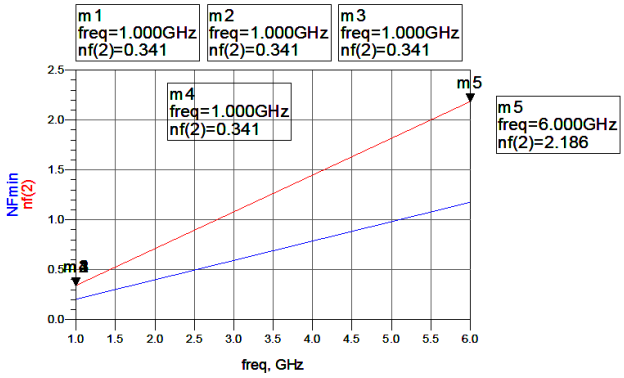

Figure 7Noise figure and Fmin plots with out tuning with 5 GHz step size.

3.1.6 Amplifier Circuit after applying Tuning Application

As discussed above the reasons which force the designer to modify the components variables, tuning application was emplyed to the primary structure and results obtained were far better than the circuit without tune [21][22].Fig below shows the noise performance of the amplifier after modification to its variables.the noise figure remains belw 1db upto 5.3GHz ,which previously went above 1 db before 2.5 GHz.at 6 GHz both NFmin and Noise figure have the same values.

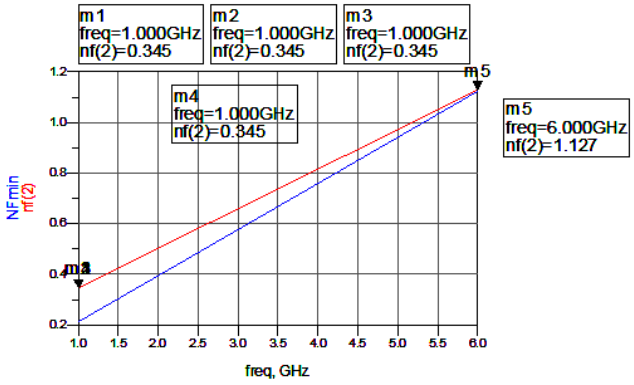

Figure8: Noise figure and Fmin plots obtained after tuning with 5 GHz step size

While gain is good enough through out the entire band.it varies linearly from 20.653 to 10.23 db.

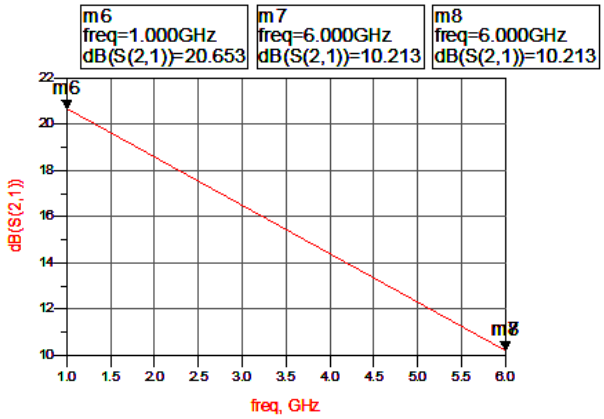

Figure 9: Gain plot with step size of 5 GHz

When the step size is reduced to 0.5GHz ,the optimum noise performance remains better in the lower frequnecy band starting from 1 GHz to 4.2GHz ,achieving close values to the corresponding minimum noise figure values.but on words from 4.2 GHz the noise performance goes lower till the last frquency.

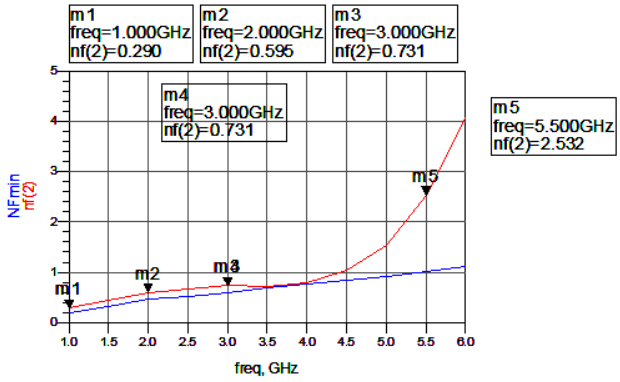

Figure 10: Noise figure after tuning with step size of 0.5 GHz

Fig 10 shows the gain variations in the wide band,which shows that with in the lower frequencies upto 4.5 GHz the gain is above 10dB. Which is reasonable for a typpical antenna system. But frequencies above 4.5 GHz the gain falls rapidly anfd goes down upto 2.446 dB.

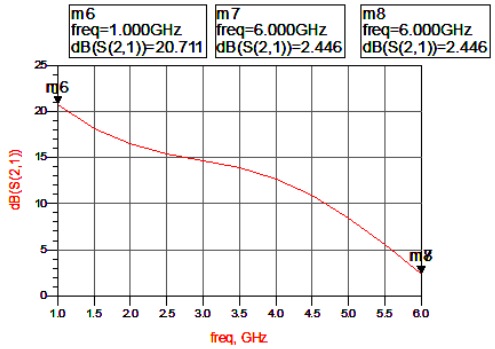

Figure 11: Gain plot obtained after tuning with 0.5GHz step size

3.1.7 LNA Circuit with Biaisng Network Design

This noise figure results are achieved from the LNA circuit with biasing network. The input and output decoupling is not included.from the graph it can be observed that from 1.8-3.8 GHz band the optimum noise performance is achieved successfully. But after 3.8 GHz the noise figure(NF) values goes high upto 3.8dB. While gain performance is better and remained above 10 db through out the band ranging from 1-4.3GHz.

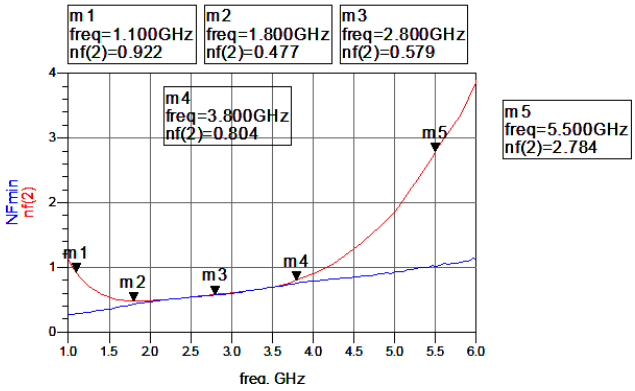

Figure 12: Noise figure obtained from biasing circuit

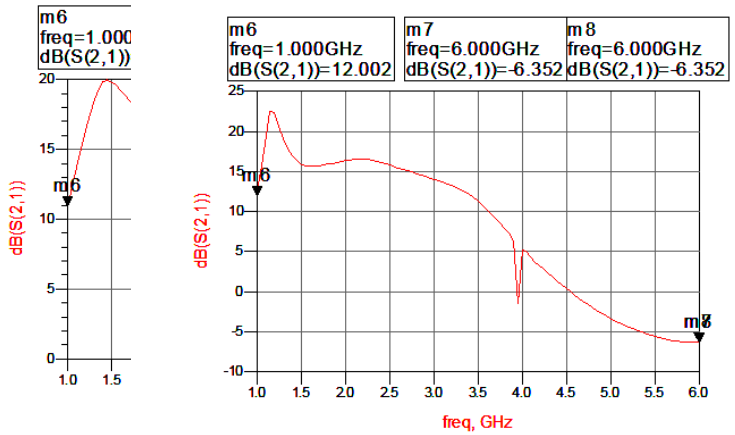

Figure 13:LNA gain obtained after biasing

3.1.8 LNA Circuit with Biasing Network and DC Isolation

DC isolation is achieved by employing DC blocking capacitors at both input and output networks [23]. The output result is shown below. It can be seen that around 4GHz frequency,there exists a discontinuity in both Fmin and NF. A drastic increase in the noise figure occurs. This noise performance can be made better by inserting extra microwave radial stubs at both input and out put DC biasing circuits [24].

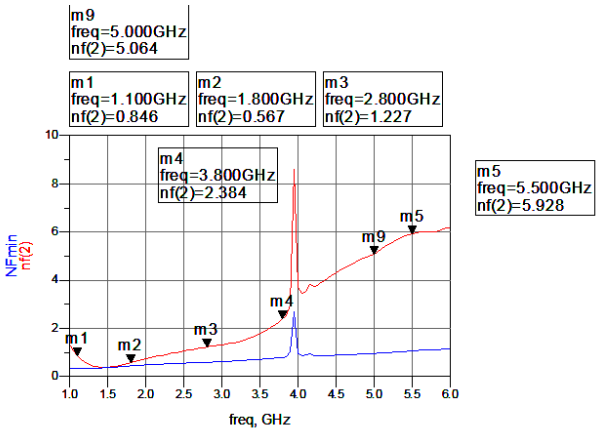

Figure 14: LNA noise figure with baising and coupling capacitor

Figure 15: LNA gain with biasing circuit and decoupling capacitor

3.1.9. LNA Circuit with Double MRSTUBs at the Biasing Network

By employing extra MRSTUB which is basically a capacitor to the Biasing circuit has not only reduced the noise figure but also removed the discontinuiy stated in the previous discussion.also improved the gain as well.

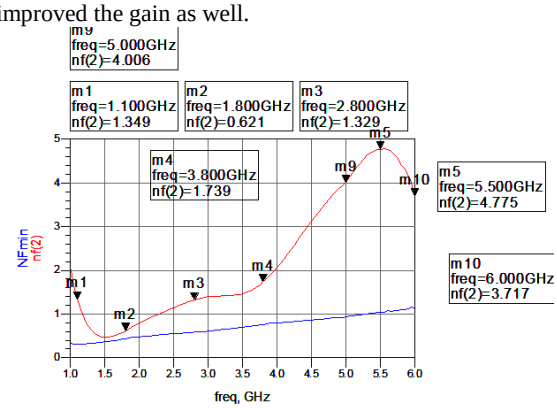

Figure. 16: LNA Noise figure double MRSB before optimization

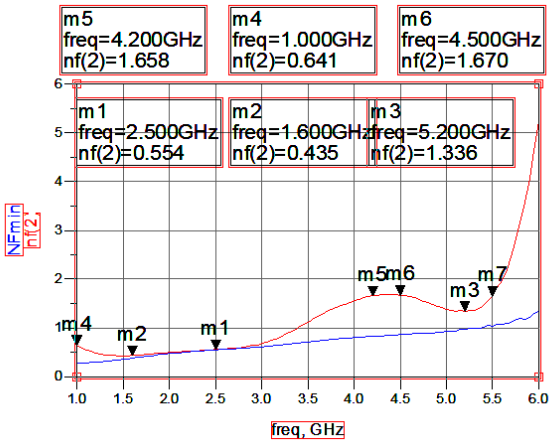

Figure 17 : noise performance of the LNA with double MRSTUB after optimization

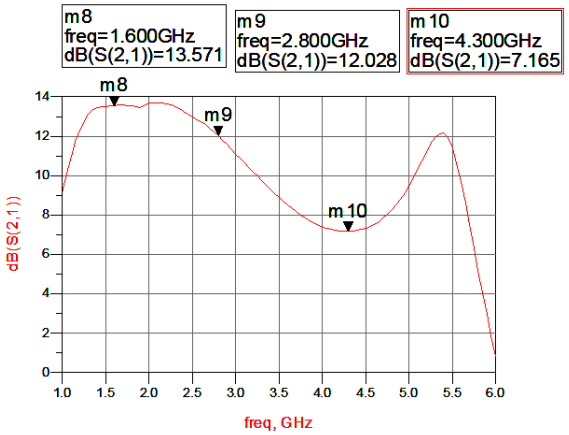

Figure 18: LNA gain with double MRSTUB

4. SUMMARY

The primary objective of this work was to design a wide band low noise amplifier (LNA) for antenna testing system utilizing a frequency band from 1- 6 GHz .since for antenna testing system the main duty of a LNA in its first stage is to offer minimal noise figure at reasonable gain. So the design focus was on optimized noise performance throughout the entire band.

The noise performance was seemed to be poor before optimization. But after tuning the results found were, NF <1 dB from 1- 3.2 GHz while gain remained above 10 dB throughout this band. A discontinuity occurred from 3.9 GHz to 4.2GHz causing the noise figure to shoot high abruptly. To overcome this problem extra microwave radial stubs has been added in the biasing network and this technique brought back the noise figure to a reasonable value after careful optimization. The final noise and gain performance is given 1 - 3.2 GHz optimal noise performance was achieved .3.2 – 5.6 GHz noise figure remained below 2dB. While onward till the end of the band its performance remained poor.

The factors responsible for this are thickness of the di electric substrate, which limits the frequency of operation of decoupling capacitors used in the circuit for DC isolation. Also practical microwave transmission lines are lossy and contribute to the noise .when they are long and narrow, they contribute much to the noise because of their higher resistivity. This is also one of the reasons that contribute to the poor performance at higher frequencies.

5. REFERENCES

[1]AV02-0672EN DS ATF-58143 08Jun2012.indd

[2]S.Y.Yngvesson,microwavesemiconductordevices,Kluwer Academic Publishers,1991.

[3]K. Chang,ed., Handbook of Microwave and optical Components,vol.2,wiley Interscience,N.Y.,1990

[4] Microwave engineering 3rd edition by David M. Pozar

[5]A. Inoue, H. Amasuga, S. Watanabe, S. Goto, and T. Oku "MMIC technologies for MW and MMW applications" IEEE International Workshop on Radio-Frequency Integration Technology, Dec. 2007.

[6]Bal S. Virdee, Avtar S. Virdee, "Broadband Microwave Amplifers", Norwood: Artech House, 2004

[7]A. Tessmann, I. Kallfass, A. Leuther, H. Massler, M. Kuri, M. Riessle, M. Zink, R. Sommer, A. Wahlen, H. Essen, V. Hurm, M. Schlechtweg, and O. Ambacher "Metamorphic HEMT MMICs and Modules for Use in a High-Bandwidth 210 GHz Radar" IEEE Journal Of Solid-State Circuits, Vol. 43, No. 10, October 2008.

[8]J. Sung, R. and S. Kim "Technology and Design Considerations for Millimeter-Wave Circuits" ICSICT 2008.

[9]C. Snowden, "Recent Development in Compound Semiconductor Microwave Power Transistor Technology", IEE Proceedings Circuits, Devices & Systems, Vol. 151, No. 3, June 2004.

[10]Nicholas J. Kolias, Colin S. Whelan, Thomas E. Kazior, and Kurt V. Smith "GaN Technology for Microwave and Millimeter-wave Applications" Raytheon Company, USA, IEEE 2010.

[11] Radio frequency and microwave electronics by Mathew m radmanesh

[12] MarcausEdwell,"Low-Noise Amplifier Design and Optimization", Luleå University of Technology 2008

[13] Agilent ATF58143 data sheet low noise psedomorphic HEMT in a surface mountplastic package,www.alldatasheet.com

[14]Design and simulation of low noise amplifier circuit for 5 to 6GH hose insahoolihzadehAlishirmoradiworld academy of science, engineering and technology 512009.

[15] Technology and design considerations for mili mere wave circuits ,jae sung rieh

[16] Jae-Sung Rieh; Sooyeon Kim, "Technology and design considerations for millimeter-wave circuits," *Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on* , vol., no., pp.1352,1356, 20-23 Oct. 2008

[17] J. D. Mellor and G. J. Linvill, "Synthesis of Interstage Networks ofPrescribed Gain Versus Frequency Slope," *IEEE Transactions onMicrowave Theory and Techniques*, vol. 23, no. 12, pp. 1013 - 1020,Dec. 1975.

[18] Wide band CMOS LNA for UHF applications, MSc dissertation by Ivy Iun lo sub,itted to university of HAWAI

[19]S.B.T Wang ,a sub mWatt 950MHz ultra wide band CMOS LNA,IEEE wireless communication symposium 2004.

[20]16 A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS lownoiseamplifier for 3.1-10.6 GHz wireless receiver," *IEEE J. Solid-StateCircuits*, vol. 39, issue 12, pp. 2259 - 2268, Dec. 2004

[21] R. M. Fano, "Theoretical Limitations on the Broadband Matching ofArbitrary Impedances," Journal of Franklin Institute, Jan. 1950.

[22]*Adriana Serban*, "Ultra-Wideband Low-Noise Amplifier andSix-Port Transceiver for High Speed DataTransmission" 2010

[23] Mohammad AfzalHussain, "low noise amplifier design for densed arrays" ,University of GAVLE

[24]H64RFP course work at moodle.nottingham.edu.my