Design of Low Power Digital FIR Filter based on Bypassing Multiplier

Prabhu E
Assistant Professor, ECE
Amrita schools of Engineering, Coimbatore

Mangalam H
Professor & Head, ECE
Sri Krishna college of Engineering and Technology, Coimbatore

Saranya K
PG Student
Sri Krishna college of Engineering and Technology, Coimbatore

ABSTRACT
Low power design promotes longer battery life in portable applications and reduces heat dissipation in high performance applications. Multiplication is one of the important operations in digital signal processing and their power dissipation is the prime concern. Many earlier multiplier designs were analyzed to reduce the switching transition. Bypassing technique is mainly used to reduce the switching power of the multiplier. Various bypassing multipliers such as Row bypassing, Column bypassing, Two-dimensional bypassing and Row-Column bypassing based multipliers were designed based on the simplification of the incremental adders and half adders instead of full adders in an array multiplier. In these multipliers extra correction circuits are required to obtain accurate results. The extra hardware in conventional design results in more power consumption. So, to overcome the drawback of conventional methods, the proposed low power bypassing based multiplier uses a simplified addition operation to reduce the switching activity and it achieves 38.7% and 25.2% of area and power reduction respectively. By taking the advantage of low power bypassing based multiplier, a digital FIR filter is implemented. The experimental results show that our proposed low power digital FIR filter saves 51% and 7% of area and power reduction respectively by using low power bypassing based multiplier.

General Terms
VLSI design.

Keywords
Bypassing logic, Low power design, FIR filter design, Switching activity reduction.

1. INTRODUCTION
Low power design is necessary to extend the operating time of integrated circuits (ICs) as well as to reduce the packaging and cooling costs [1, 2]. As the scale of integration keeps growing, more and more complex signal processing systems are being implemented on a VLSI chip. These signal processing applications consume considerable amount of energy. The trade-off of performance and area remain to be the two major design factors, high power consumption is critical in today's VLSI system design. The need for low-power VLSI system arises from two main forces. First, Static power dissipation is due to the leakage current. Second, Dynamic power dissipation is due to the transition activity that dominates the total energy dissipation due to charging and discharging of capacitors. Multiplication is a fundamental operation in most signal processing algorithms [3]. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low- power VLSI system design. The processing algorithms performance is generally determined by the performance of the multiplier. Many multiplier design based on the reduction of the switching activities reported in literature. Basically there are many approaches for designing a low-power multiplier [4]; one is by designing a low-power FA in an array multiplier. The second approach is by reducing the partial product computation [6]. The other important approach to reduce the power dissipation is by the architectural modification via bypassing techniques. A finite impulse response (FIR) filter is a type of a signal processing filter whose impulse response is of finite interval, because it settles to zero in finite time [11]. This is in disparity to infinite impulse response (IIR) filters, which have internal feedback and may keep on responding for an indefinite period. Multiplier is one of the basic functional units in FIR filter design which consumes most of the power. So, it is necessary to design low-power multiplier for FIR filters. This paper presents a low power FIR filter based on bypassing multiplier. The rest of this paper is organized as follows. Section 2 reviews the Braun array multiplier design and previous work on multiplier with bypassing methods. Section 3 describes the low power bypassed based multiplier design for digital FIR filter. The Section 4 gives simulation results and discussion. Finally, Section 5 offers a brief conclusion.

2. RELATED WORK

2.1 Braun array Multiplier
The Braun array multiplier [8] consists of three functions: partial-product generation, partial-product accumulation, and final addition. First, partial-product generation requires N×N AND gates of two inputs. Second, partial-product accumulation requires (N−1) rows of carry-save adders, in which every row consists of (N−1) full adders, and the final addition that contains a (N−1) bit ripple-carry adder in the last row is for carry propagation. Therefore, an N×N bits array multiplier requires N× (N−1) full adders. Because Braun array multipliers have higher switching activity, one way to reduce dynamic power, is to avoid redundant switching transitions. The following section describes four bypassing multiplier designs to reduce dynamic power, and explains the area overhead problem in the conventional bypassing multiplier design.

2.2 Braun multiplier with row bypassing
For a low-power row-bypassing Braun multiplier [6] the addition operations in the j-th row can be disabled to reduce the power dissipation if the bit bj in the multiplier is 0. In the multiplier design, each modified FA in the CSA array is attached by three tri-state buffers and two 2-to-1 multiplexers. Because the addition operations of the rightmost FAs in the CSA rows are able to be bypassed, the extra correcting

circuits must be added to correct the multiplication result. The 4X4 Braun multiplier with row bypassing is shown in Fig. 1.

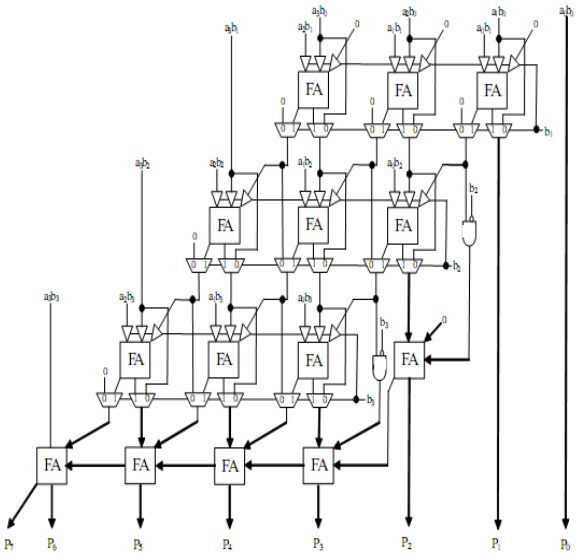

Fig. 1 4x4 Braun multiplier with row bypassing [6]

2.3 Braun multiplier with column bypassing

For a low-power column-bypassing multiplier [5], the addition operations in the (i+1)-th column can be bypassed if the bit, ai, in the multiplicand is 0. In the multiplier design, the modified FA is simpler than that in the row bypassing multiplier. Each modified FA in the CSA array is only attached by two tri-state buffers and one 2-to-1multiplexer. As the bit, ai, in the multiplicand is 0, their inputs in the (i+1)-th column will be disabled and the carry output in the column must be set to be 0 to produce the correct output. Hence, the protecting process can be done by adding an AND gate at the outputs of the last row of CSAs. The 4X4 Braun multiplier with column bypassing is shown in Fig. 2.

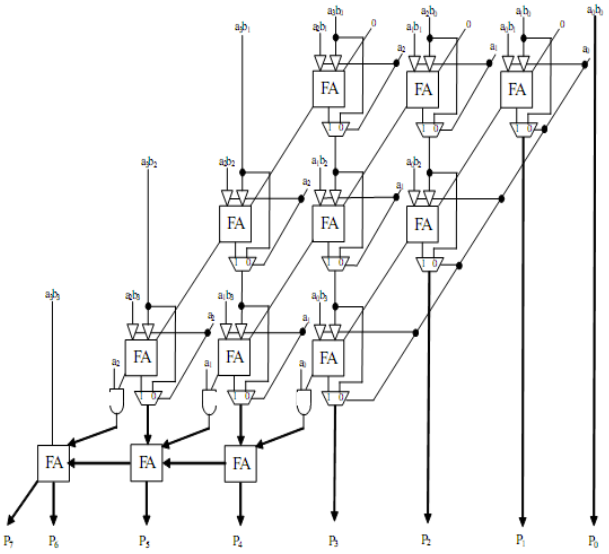

Fig. 2 4x4 Braun multiplier with column bypassing [5]

2.4 Braun multiplier with 2-dimensional bypassing

For a low-power 2-dimensional bypassing-based multiplier [4], it is desired that the addition operations in the (i+1)-th column or the j-th row can be bypassed if the bit, ai, in the multiplicand is 0 or the bit, bj, in the multiplier is 0. To correct the carry propagation in the multiplication result, the carry bit must be considered in the bypassing condition as follows: If the bit, ai and bj, are 0 and the carry bit, ci,j-1, is 1, the addition operations in the (i+1)-th column or the j-th row cannot be bypassed. Hence, the bypassing circuit must be added into the necessary FA to form a correct adder cell (AC). However, the inserted bypassing circuit in AC is so complicated that the ability of the power reduction is decreased. The 4x4 Braun multiplier with 2-dimensional bypassing is shown in Fig. 3.

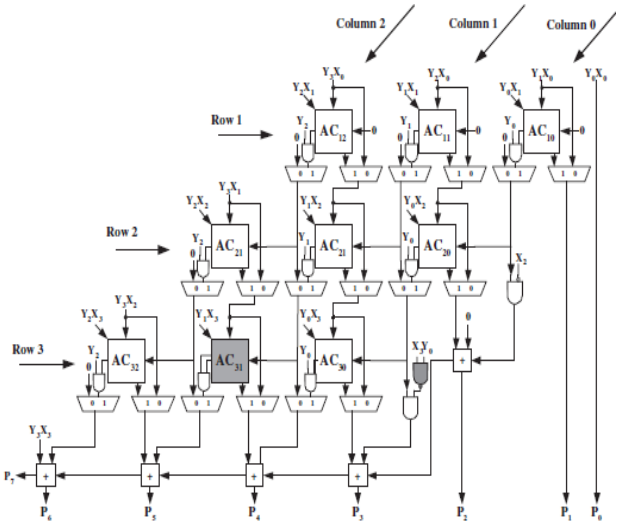

Fig. 3 4x4 Braun multiplier with 2-dimensional bypassing [4]

2.5 Braun multiplier with row and column bypassing

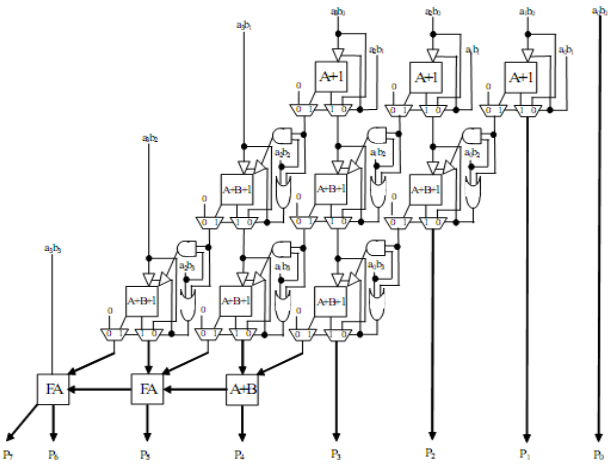

Fig. 4 4x4 Braun multiplier with row and column bypassing [3]

According to the bypassing features in the previous Braun array with row or column bypassing multipliers [3], the addition operations in the (i+1)-th column or the j-th row can be bypassed for the power reduction if the bit, ai, in the

multiplicand is 0 or the bit, bj, in the multiplier is 0.But in row and column bypassing based multiplier, the addition operation in the (i+1, j) FA can be bypassed if the product, aibj, is 0and the carry bit, ci,j-1, is 0, that is, as the product, aibj, is 1 or the bit, ci,j-1, is 1, the addition operation in the (i+1, j) FA can be executed. It is known that the (i+1, j) FA only executes the A+1addition as the product, aibj, is 1 and the bit, ci,j-1, is 0, or the product, aibj, is 0 and the bit, ci,j-1, is 1. On the other hand, the (i+1, j) FA only executes the A+2 addition as the product, aibj, is 1 and the bit, ci, j-1, is 1.The 4X4 Braun multiplier with row and column bypassing [3] shown in Fig. 4.

3. PROPOSED DESIGN

A Low power multiplier based on bypassing technique for digital filter is based on 2-dimensional bypassing feature, the addition operations in the (i+1)-th column or the j-th row can be bypassed for the power reduction if the bit, ai, in the multiplicand is 0 or the bit, bj, in the multiplier is 0. On the other hand, to correct the carry propagation in the multiplication result, the carry bit in the previous row must be considered in 2-dimensional bypassing condition. In our proposed low-power bypassing-based multiplier, the addition operation in the (i+1, j)-th FA can be bypassed if the product, aibj, is equal to the carry bit, ci,j-1, that is, as the product, aibj, is not equal to the bit, ci,j-1, the addition operation in the (i+1, j)-th FA must be executed. Hence, the control signal in the bypassing condition can be obtained by the XOR result of the product, aibj, and the carry bit, ci, j-1.

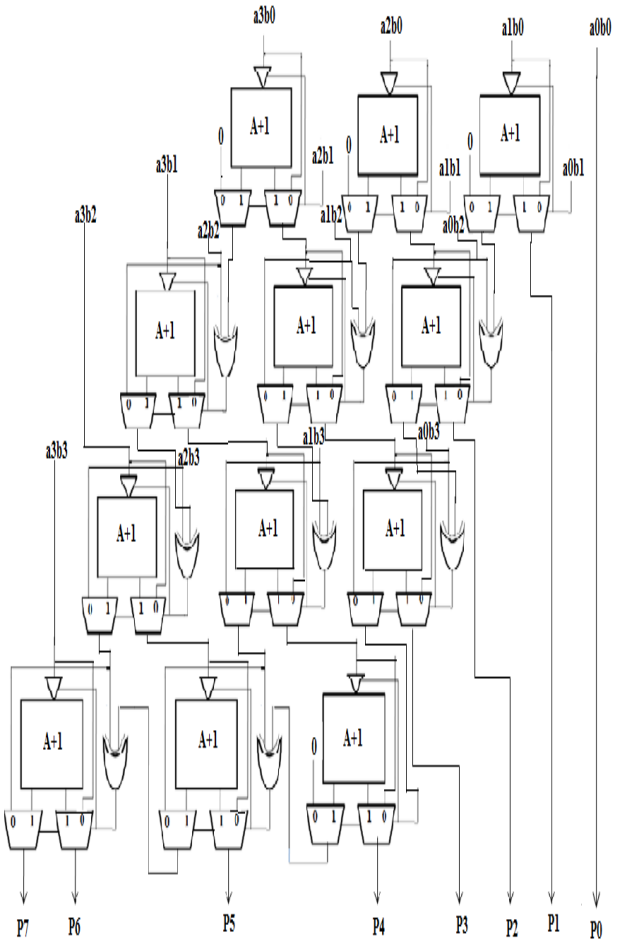

Fig. 5 4x4 low power bypassing-based multiplier

According to the proposed bypassing condition, it is known that the (i+1, j)-th FA only executes the A+1 addition as the product, aibj, is not equal to the carry bit, ci,j-1. On the other hand, as the product, aibj, is equal to the carry bit, ci,j-1, the addition result in the (i+1, j)-th FA will be obtained by adding 2 or 0. Therefore, the resultant carry bit, ci+1, j, in the (i+1, j)-th FA can be bypassed from the previous carry bit, ci, j-1, and the (i+1, j)-th FA can be replaced with a low-cost incremental adder, A+1. Besides that, each simplified adder, A+1, in the CSA array is only attached by one tri-state buffer and two 2-to-1 multiplexers. Similarly, a HA can be also replaced with a low-cost incremental adder, A+1, with the bypassing condition as aibj=0. By using the bypassing-based design of a half adder and a full adder, a 4x4 low-power bypassing-based multiplier can be designed. The 4x4 low power bypassing based multiplier, as shown in Fig. 5.

For a discrete-time FIR filter, the output is a weighted sum of the current and a finite number of previous values of the input [11]. The operation is described by the following equation(1), which defines the output sequence y[n] in terms of its input sequence x[n]:

$$y[n] = \sum_{i=0}^{n-1} a_i x(n-1) \qquad (1)$$

Where,

x[n] is the input signal, y[n] is the output signal, bi are the filter coefficients, also known as tap weights, that make up the impulse response, N is the filter order, an Nth-order filter has (N + 1) terms on the right-hand side. Here, x [n-i] in these terms are commonly referred to as taps. A 4 tap FIR filter show in Fig. 6, for low power bypassing based multiplier.

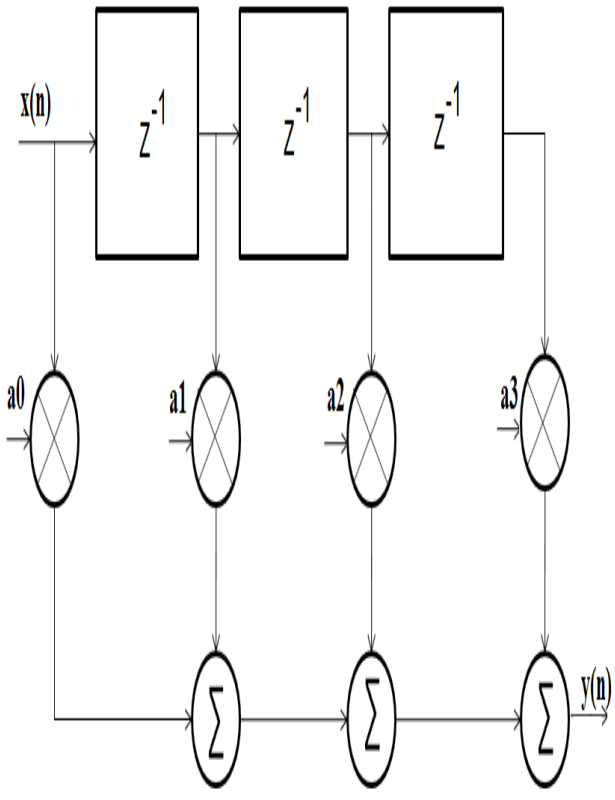

Fig. 6 Four tap digital FIR filter based on low power bypassing based multiplier.

4. SIMULATION RESULTS AND DISCUSSION

The simulation results for the bypassing based multipliers are shown in Table 1. The XILINX ISE 9.2i with Spartan2E as target device is used to synthesis the program and ModelSim DE 6.5e to simulate the results. The building blocks are coded in VHDL. The XILINX ISE 9.2i with Spartan2E as target device is used to analyze the total estimated power consumed by the bypassing techniques. The area analyses of bypassing based multipliers are carried out using XILINX ISE 9.2i. Performance of the proposed FIR filter using low power consumption multiplier by comparing with the different conventional multipliers is given blow.

Table 1. Comparison of area and power of FIR filter

S.NO.	FIR ARCHITECTURES	GATE COUNT	POWER (mW)
1	FIR using Braun Multiplier	1828	174
2	FIR using Row Bypassing multiplier	1930	174
3	FIR using Column Bypassing multiplier	1714	170
4	FIR using Two-dimensional Bypassing-based multiplier	1945	180
5	FIR using Row and Column Bypassing multiplier	1870	171
6	FIR using Low power bypassing-based multiplier	895	162

The simulation results show that the row-bypassing design and the 2-dimensional bypassing design actually consume more area and power due to the extra circuits and the proposed design reduces 51% and 7% of the area and power dissipation respectively. The number of gates and the power consumption utilized by low power bypassing based multiplier is proven to be less when compared with other multipliers and it achieves 38.7% and 25.2% of area and power reduction respectively. The low power bypassing based multiplier reduces the adders required for its operation and extra correction circuits are avoided, thus making a visible reduction in the gate count and power consumption.

5. CONCLUSION

The design approach of an optimized FIR filter using different bypassing multipliers is discussed. Compared to other bypassing multipliers a new methodology for designing of high-level optimization technique based on the simplification of the addition operations in a low-power bypassing-based multiplier for FIR filter is proposed to reduce the switching activity. The simulation result shows that the proposed low power FIR filter using bypassing multiplier achieves higher power reduction with lower hardware cost than the other conventional FIR filter using different multipliers.

6. REFERENCES

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