A Novel Ripple/Carry Look Ahead Hybrid Carry Select Adder Architecture

Lakshmesha J
Department of E and C
R V college of Engineering
Bangalore 560059 India

K R Usha Rani
Department of E and C
R V college of Engineering
Bangalore 560059 India

ABSTRACT

In this paper, two general architectures of Carry Select Adder (CSA) have been introduced for high speed addition. These CSA architectures utilize the hybridized structure of Carry Lookahead Adder (CLA) and Ripple Carry Adder (RCA). In these architectures the critical path delay has been reduced by reducing the number of multiplexer stages. The proposed designs are compared with regular CSA based on RCA. The second architecture showed 11.3%, 3.9% improvement in delay and an overhead of 13% in area.

General Terms

Adder, Arithmetic circuits. Data path components.

Keywords

Carry Select Adder; Carry Lookahead Adder, Ripple Carry Adder, hybrid Adder.

1. INTRODUCTION

Addition is one of basic arithmetic operation extensively used in data path design of DSP's and ACSIC's. Adder's initial design was based on very slow RCA architecture with low real estate. Weinberger and Smith [1] reported the novel CLA concept .They showed that by separating the sum and carry logic (carry lookahead logic) higher speed can be achieved, at the cost of increased complexity .As the number of bits increases, fan-out requirement dramatically increases. Hence CLA is limited to groups of four bits. Ladner and fishner [3], Kogge and Stone [4] and Han and Carlson [5] further expanded the CLA concept to prefix adders. Prefix adder are high speed adders, requiring substantial overhead in wiring. O J Bedrij [2] introduced the CSA (based on RCA), in which the critical path delay has been greatly reduced.

Many variants and optimizations of CSA (based on CLA) have been reported.,in [6] Tyagi has proposes a method to generate carry that can be applied even to CSA and prefix adders. In comparison to carry skip adder, this method reduced delay by 24.3% at an area overhead of 7%. Yuke Wang [7] presents general 56-bit high speed architecture of CSA based on CLA. A group generate and propagate logic are used to reduce the critical path delay by 2/3 of the classical CSA. Ruiz [9] optimization method used compact multi-output CLA. His 32-bit adder circuit resulted in maximum improvement of 25% area and 35% power over other counterparts.

Optimizations of CSA based on RCA have also been reported. Kim [8] proposed a multiplexer based add one circuit with 42% fewer transistors against conventional CSA. Yajuan [10] shows an improvement over Kim's design. Rajkumar [11], used Binary to Excess one Converter (BEC) logic to reduce both area and power, at the cost of increased delay.

CSA based on both CLA and RCA designs and their optimizations have been proposed. There has been no effort to integrate both CLA and RCA together into a single CSA design. In this paper we introduce two such general hybrid architectures of CSA that combine CLA and RCA. In these structures variable adder length have been achieved to reduce the number of mux stages and hence the critical path.

2. DESIGN OF ADDERS

2.1 The Hybrid Ripple Carry Lookahead Adder (HRCLA) Architecture

Hybridization has been achieved by rippling the 3rd carry of a 4-bit CLA, through a full adder as in Figure 1. This method resulted in reduction of real estate but at the cost of increased critical path delay. Further, the concept has been extended to have two and three full adders rippled in the same manner.

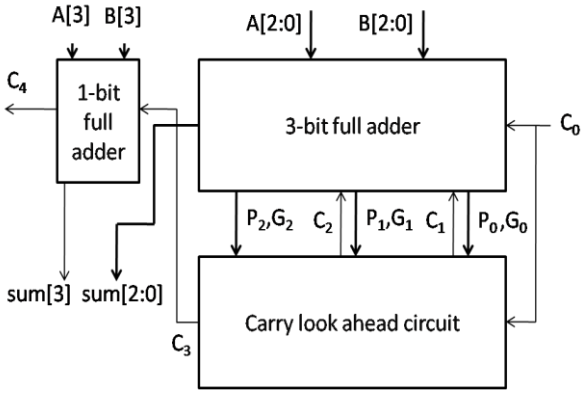

Fig 1: The HRCLA showing one ripple adder and three bit CLA

2.2 The Conventional CSA using CLA

CSA shown in Figure 3 is uses 4 bit CLA blocks. Since the size of the CLA blocks cannot be increased, variable length cannot be achieved. Hence this is not a square root CSA design [11].

2.3 Proposed hybrid architecture I

The main problem in CSA using CLA is, the number of bits computed per stage is limited to four bits. In these new hybrid architectures the number of bits computed per MUX stage can be increased. As shown in Figure 3 CLA is used in initial stages, HRCLA is used in 4 stages. In Later stages this method helps to reduce the adding components, containing only ripple adders. By using ripple adders, the bits computed per MUX stage can be increased linearly, leading to increased speed.

2.4 Proposed hybrid architecture II

The second architecture is based on the hybridization of CSA by using both RCA and CLA as in Figure 4. In this

architecture the 4-bit CLA has been retained in each stage. RCA is cascaded cumulatively by one bit to the CLA in each stage (hybrid structure). The number of stages of mux can be reduced further, when compared to the architecture I, hence the critical path delay has been further reduced.

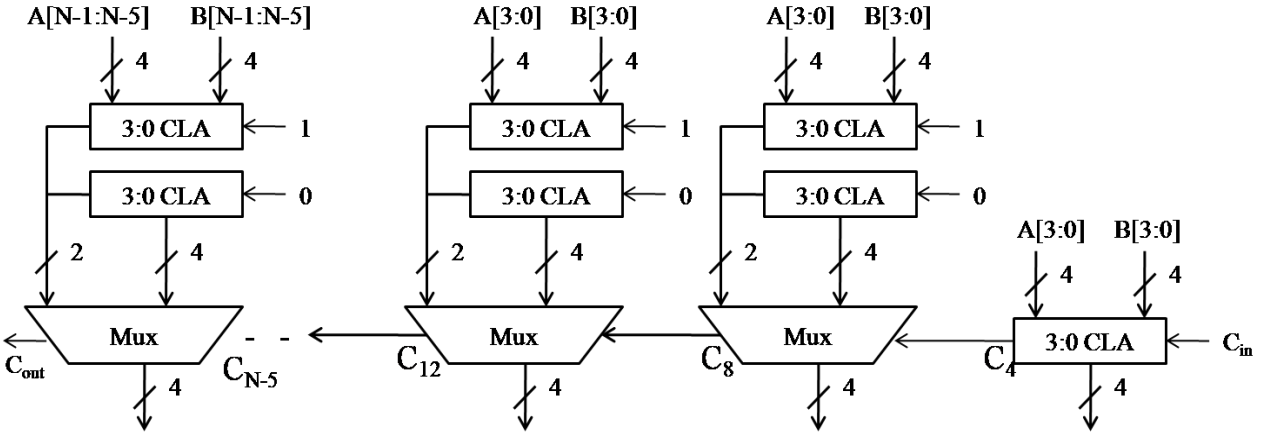

Fig 1: N-bit Conventional Carry Select Adder using CLA

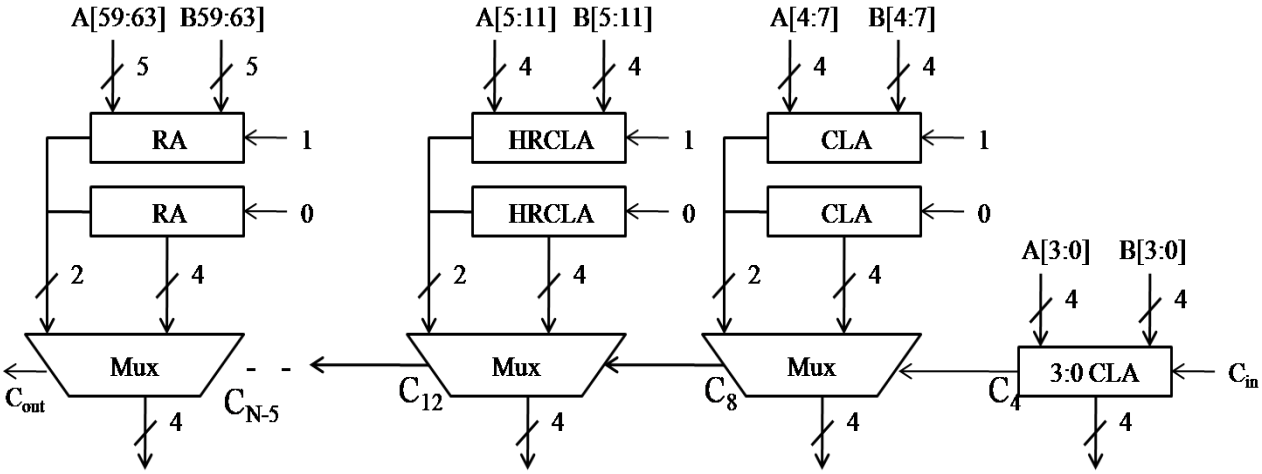

Fig 3: 64-bit CSA architecture I

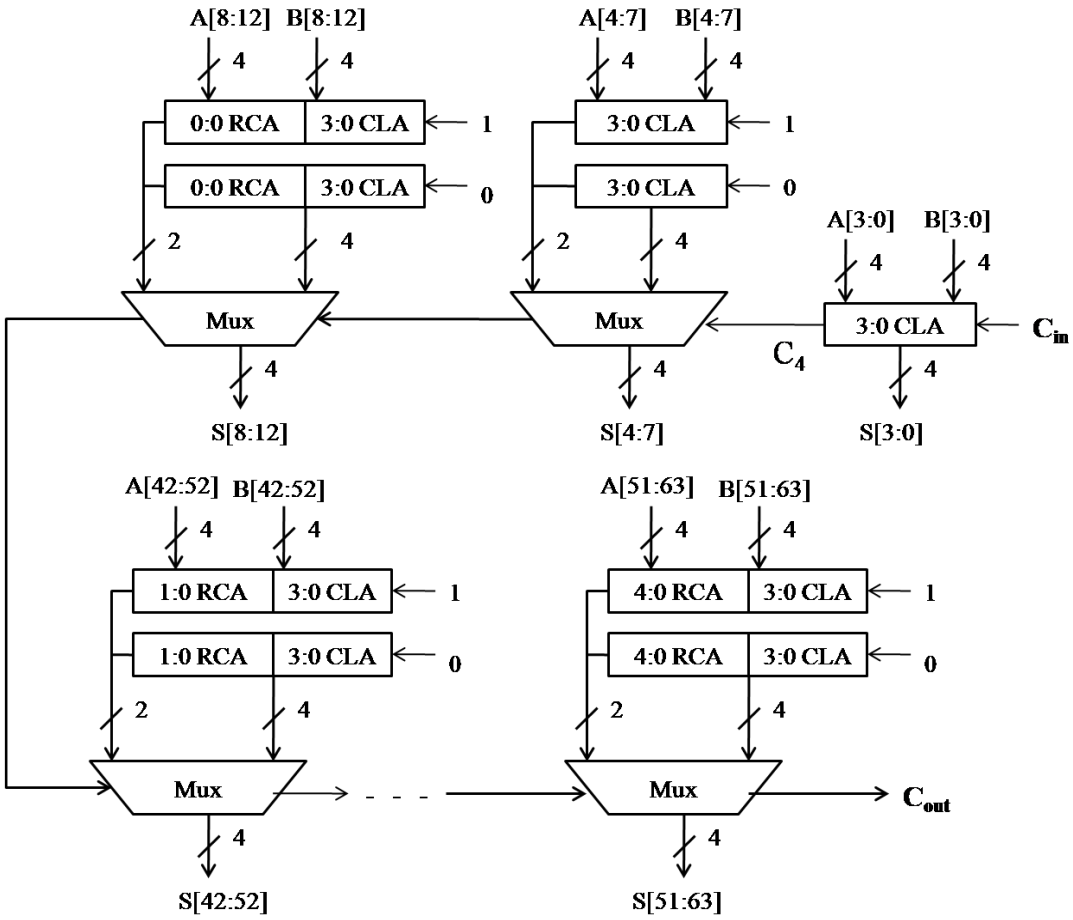

Fig 2: 64-bit CSA architecture II

3. RESULTS AND ANALYSIS

Place The designs were developed in Verilog HDL and synthesized using TSMC .18um library. The library has been characterized at conditions: temperature: 125 Celsius; Voltage: 1.62 V. From the area variation curve shown in figure 5, there is no substantial advantage in the area for both design architecture I and architecture II. For 64 bit adder architecture I showed 3.51% improvement, where as architecture II showed .23% degradation in area.

The power curve shown in figure 7 depicts the main problem in both design architecture I and II, the increase in power consumption. There are two reasons for this, one is the synthesis (mapping) process and other is increase in switching activity. For 64 bit adder design I and II showed a degradation of 42% 33% respectively.

The delay characteristics in figure 8 clearly show the improvement architecture I and architecture II. The reason for this improvement is reduction in multiplexer stages. For a 64 bit adder design I showed an improvement of 15%, where as design II showed 26% improvement.

Table 1. Performance comparison of 64-bit adder architectures

	Regular CSA based on CLA	**Regular CSA based on RCA [11]**	**Proposed CSA architecture I**	**Proposed CSA architecture II**
Average Power(nW)	1725918=x	1.50x	1.43x	1.33x
Area (um^2)	10022.44=y	.85y	0.96y	1.0023y
Worst case delay(ps)	3600.7=z	.76z	0.84z	0.73z
Power delay product(10^{-12} Ws)	6.215=w	1.14w	1.20w	1.011w

Summarizing, the performance comparison of the 64-bit conventional CSA using CLA and the proposed CSA is tabulated in Table 1; clearly the critical path delay has

substantially reduced. Area is marginally saved but the power has increased substantially, as the number of bits increases area and delay improvement is also more (architecture I) as in seen in the Figures 5 and 7, but the power of proposed CSA design also increases for both architectures, as observed from the Figure 6.

4. CONCLUSION

The two architectures CSA are designed using the hybridized structure of both RCA and CLA. The hybrid architecture has been designed in Verilog HDL. The comparative study of proposed and existing adder designs have been verified and synthesized in cadence (using TSMC 180nm technology library).

The intention of this paper is to present two architectures at higher abstraction level (RTL) and support its practical use for high speed application. Amongst the two new architectures presented, the second has overall better attributes. These structures have intermediate characteristics of CSA based on RCA and CLA. These architectures are general in nature; further optimizations can done; by using other variants of CLA and RCA.

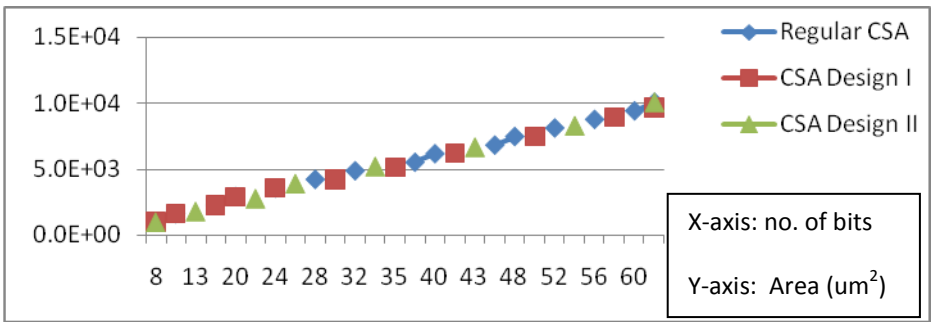

Fig 3: Variation of area against number of bits

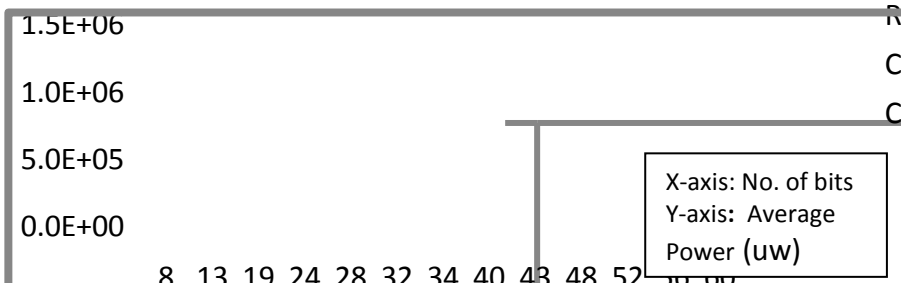

Fig 4: Variation of power against number of bits

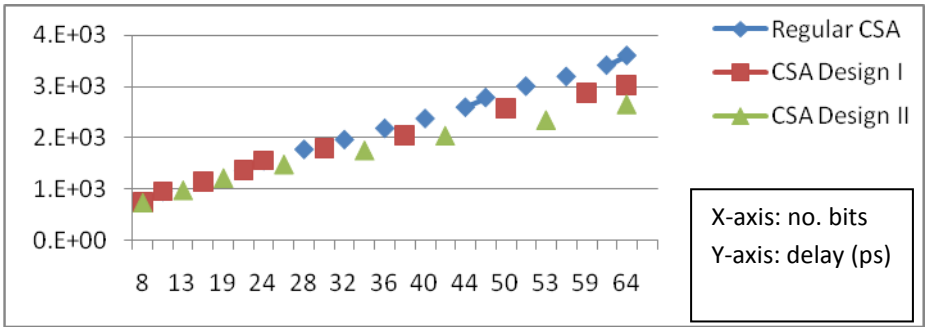

Fig 5: Variation of delay

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