

Comparative Study of Different Low Power Design Techniques for Reduction of Leakage Power in CMOS VLSI Circuits

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ABSTRACT

Scaling of transistor features sizes has improves performance, increase transistor density and reduces the power consumption. A chip's maximum power consumption depends on its technology as well as its implementation. As technology scales down and CMOS circuits are powered by lower supply voltages, standby leakage current becomes significant. As the threshold voltage is reduced due to scaling, it leads to increase in sub threshold leakage current and hence increase in static power dissipation. This paper presents performance analysis of inverter using conventional CMOS, stack and dual threshold transistor stacking, sleepy stack, sleepy keeper technique etc. The performance analyses of inverter were analyzed in 90nm technology using Virtuoso software (cadence). In order to reduce the static power dissipation, one has to sacrifice circuit performance and area. This paper presents the comparative study of all the approaches. The sleepy stack and variable body biasing approach shows improved results in terms of static power.

General Terms

Low power design, leakage power

Keywords

CMOS inverter, cadence, static power, sleepy keeper, threshold voltage, transistor stacking.

1. INTRODUCTION

The power is emerging as the most critical and vital issues in system on chip design today and management of power in every category of design is becoming an increasingly urgent problem. In early 1970's, providing high speed operation with minimum area were main aim of design. Many design tools are concentrated to achieve these goals.

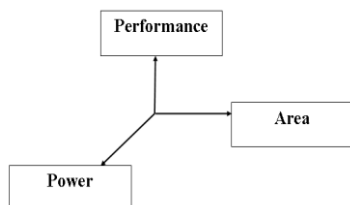


Fig 1: Design Parameters

However, introducing the third parameter of power dissipation made the designers to change the flow as shown fig 1. In CMOS VLSI circuits, power dissipation is basically due to the

three important and major components: dynamic, static and short circuit. The switching activity is given by [8].

$$P(\text{switching}) = C_{pd} \times V \times F_i \quad (1)$$

Where F_i is input signal frequency, C_{pd} dynamic power dissipation capacitance, V is the supply voltage.

Due to the growing demand of battery operated devices, the power consumption has become a vital and major problem of integrated circuit designer. Scaling has result exponential increase in the leakage current [8]. The subthreshold leakage current $I_{leakage}$ can be given as

$$I_{leakage} = I_0 e^{(V_{gs} - V_{th})/\eta VT} \quad (2)$$

Where

$$I_0 = \mu_0 c_{ox} \left(\frac{W}{L}\right) V_T^2 e^{1.8},$$

C_{ox} is the gate oxide capacitance, (W/L) is the width to length ratio of the MOS device, μ_0 is the zero bias mobility, V_{gs} is the gate to source voltage, V_T is the thermal voltage and η is the sub threshold coefficient. Several techniques have been proposed to reduce leakage power. One important thing in CMOS VLSI circuit design is to lower the power dissipation while maintaining the high performance of the circuit to maintain the performance of the circuit. To maintain the circuit performance it is needed to scale the threshold voltage. For low threshold age transistors which are fast have high threshold leakage current are used to implement the logic. High threshold which are slow and have low sub threshold leakage current. The propagation delay is given by [8]

$$T\alpha \frac{C_L V_{dd}}{(V_{dd} - V_x - V_t)^\alpha} \quad (3)$$

Where C is the total load capacitance V_{dd} is the supply voltage, V_t is the threshold voltage and α model short channel effect.

ITRS reported that leakage power consumption may come to dominate total chip power consumption as technology feature size shrinks [6, 8]. It can observe be that static consumption tends to increase over the year as dynamic power consumption [11]. The increasing prominence of portable systems and the need to limit power consumption in very high

density ULSI chips have lead to rapid and innovative development in low power design. Due to power sensitive portable devices, low power is very important requirement of all high performance application where power is one of the important design constraints.

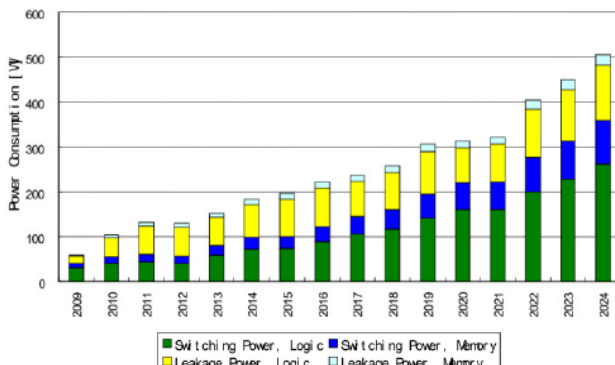


Fig. 2: Power consumption prediction by the ITRS 2009[8].

In today's era of VLSI, power consumption control and management has become a key challenge and critical issue in electronics industry. The advancement in VLSI technology allows integrating a complete system on chip (SoC) providing facility to develop a portable system. Power dissipation is a critical parameter in battery operated portable device. The limited battery Lifetime typically imposed very strict demands on the overall power consumption of the portable systems. Power consumption is one of the important factors of VLSI circuit design for CMOS is the primary technology. The power consumption has become a fundamental problem in VLSI circuit design. Therefore, reducing the power consumption of integrated circuits through design improvement is a major challenge in portable system design. To solve the power consumption problem, many different techniques from circuit level to device level and above have been proposed by researchers. However, there is no straight forward ways to meet the tradeoff between power, delay and area. The designers are required to choose appropriate techniques that satisfy the application and product needs [3]. Reducing power dissipation varies from application to application. The key objective in reducing power consumption is to reduce the overall cost the product. One of the most challenging problem is to find out new and effective circuit design technique to reduce the overall power dissipation without compromising the performance of the device. Scaling advanced CMOS technology improves high performance and high transistor density. The power dissipation of a chip depends not only on its technology but also on its implementation i.e on size, circuit style, operating frequency and so on. Because of this technology trends transistor leakage power has increased exponentially supply voltage scaling increases sub-threshold leakage current, increases leakage power and pose numerous leakage in the VLSI design. Therefore static power has become a significant portion of the total power consumption. There are several VLSI techniques to reduce leakage power. Different techniques provide an efficient way to reduce leakage power, but disadvantages of each technique limit the application of

each technique. In this paper an efficient sub-threshold leakage current reduction and optimization methods are presented and result are given for 90nm generic process design kit technology using virtuoso schematic editor.

2. SUBTHRESHOLD LEAKAGE POWER REDUCTION TECHNIQUES

Fig [3] shows that sub threshold leakage current (power) is becoming the primary source of power dissipation is CMOS below 90nm. At smaller geometries, management of leakage current can greatly impact design and implementation choices [9]. Till now, primary concerned were improving the performance of design and reducing silicon area to lower the cost. Now power is replacing performance as the key metric for VLSI design.

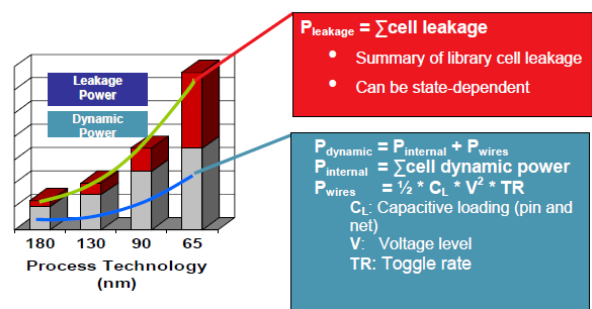


Fig. 3: Process technology vs. leakage and dynamic power [8].

2.1 Conventional CMOS Technique

Fig. 4. shows the block diagram of digital circuit using conventional CMOS techniques. In this technique, a fully complementary CMOS circuit has an nMOS pull down network to connect the output to '0' (GND) and pMOS pull up network to connect the output to '1' (VDD).

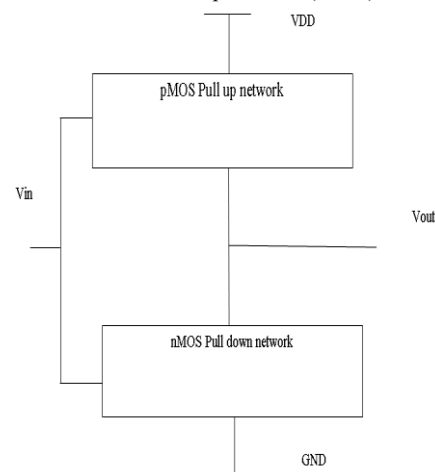


Fig. 4: Base case (conventional CMOS) circuit structure.

2.2 Stack Technique

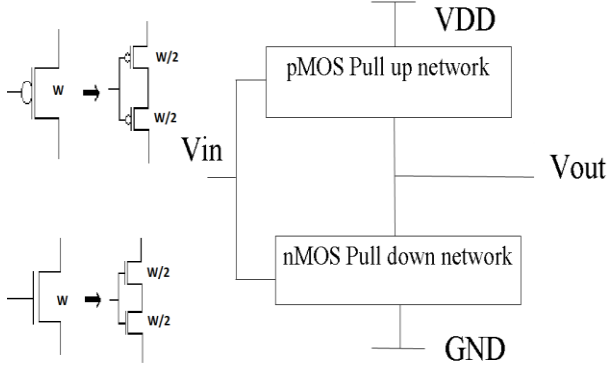


Fig. 5: Stack Technique circuit structure.

This technique is based on the fact that natural stacking of MOS-FET helps in achieving leakage current. The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect [4]. An effective way to reduce leakage power in active mode is stacking of transistor [1].

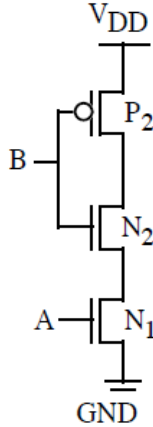


Fig. 6: Circuit schematic of Forced stack technique [6].

The subthreshold leakage is exponentially related to the threshold voltage of the device and threshold voltage changes due to body effect. The source of the nMOS device N1 is connected to ground. Transistor N2 source is connected to drain of N1. The source of N2 is not grounded and it can acquire voltages close to Vdd while its substrate is connected to ground. Therefore the condition $V_{sb}=0$ will not hold in bias cases for transistor N2. The device N1 will experience higher V_{th} due to the difference in the voltage between the source and body. The voltage between drain and source also decreased since the intermediate node has a voltage above the ground resulting reduction in DIBL affect and hence effective saving of leakage power. For turned off the single transistor, leakage current I_{sub0} can be expressed as follows [3,8]:

$$I_{sub0} = Ae \frac{1}{nV\theta} (V_{gs0} - V_{th0} - \gamma V_{sbo} + \eta V_{dso}) \left(1 - e^{-\frac{V_{dso}}{V\theta}}\right) \quad (4)$$

$$= Ae \frac{1}{nV\theta} (-V_{th0} + \eta V_{dd}) \quad (5)$$

$$A = \mu_0 C_{ox} (W/L_{eff}) V_{\theta}^2 e^{1.8} \quad (6)$$

n =sub-threshold coefficient V =thermal voltage V_{gs0} , V_{th0} , V_{bs0} and V_{ds0} are the gate-to-source voltage, the zero-bias threshold voltage, the base -to-source voltage and the drain-to-source voltage respectively. γ is the body-bias effect coefficient, and η is the Drain Induced Barrier Lowering (DIBL) coefficient. μ is zero-bias mobility, C_{ox} is the gate-oxide capacitance, W is the width of the transistor, and L_{eff} is the effective channel length. Two transistor are turned off together ($M1=M2$). So,

$$I_{sub1} = Ae \frac{1}{nV\theta} (V_{gs1} - V_{th0} - \gamma V_{sb1} + \eta V_{ds1}) \left(1 - e^{-\frac{V_{ds1}}{V\theta}}\right) \\ = Ae \frac{1}{nV\theta} (-V_x - V_{th0} - \gamma V_x + \eta (V_{dd} - V_x)) \quad (7)$$

$$I_{sub2} = Ae \frac{1}{nV\theta} (V_{gs2} - V_{th0} - \gamma V_{sb2} + \eta V_{ds2}) \left(1 - e^{-\frac{V_{ds2}}{V\theta}}\right)$$

$$= Ae \frac{1}{nV\theta} (-V_{th0} + \gamma V_x) \left(1 - e^{-V_x/V\theta}\right) \quad (8)$$

Where V_x is the voltage at the node between M1 and M2. Now consider X is the factor of I_{sub0} and I_{sub1} ($=I_{sub2}$)

$$X = \frac{I_{sub0}}{I_{sub1}} = \frac{Ae \frac{1}{nV\theta} (-V_{th0} + \eta V_{dd})}{Ae \frac{1}{nV\theta} (-V_x - V_{th0} - \gamma V_x + \eta (V_{dd} - V_x))} = e^{\frac{V_x}{V\theta} (1 + \gamma + \eta)} \quad (9)$$

If $I_{sub1}=I_{sub2}$ the from equation (9) can be written as

$$1 = e^{\frac{1}{nV\theta} (\eta V_{dd} - V_x (1 + 2\eta + \gamma))} + e^{-\frac{V_x}{V\theta}} \quad (10)$$

The threshold voltage can be controlled by body bias effect.

$$V_{th} = V_{t0} + \gamma (\sqrt{V_{sb}}) \quad (11)$$

Changing the substrate voltage causes the threshold voltage to change. So the different kind of effect is arises for changing the substrate voltage like Zero-Body Bias, Reverse-Body Bias and Forward-Body Bias. This Phenomenon is frequently used for controlling the threshold voltage. γ Constant dependent on the transistor parameter and the technology feature size. By controlling body biasing effect with changing the constant term can easily control the leakage power [3,7].

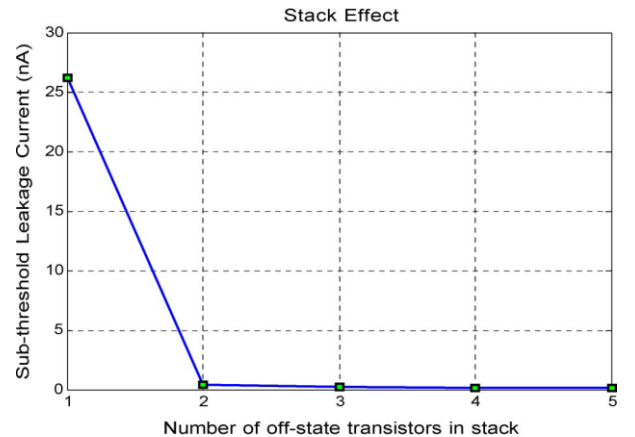


Fig. 7: Leakage current decrease with an increasing number of off transistors in stack technique [8].

Fig. 7 shows the leakage current trends of each stacked transistor as a function of number of stacked transistor.

2.3 Sleep Transistor Technique

This technique uses the sleep transistor between both VDD and the pull up network and between GND and pull down

network [3]. The sleep transistor turn off the circuit by cutting off the power rails in idle mode thus can reduce leakage power effectively.

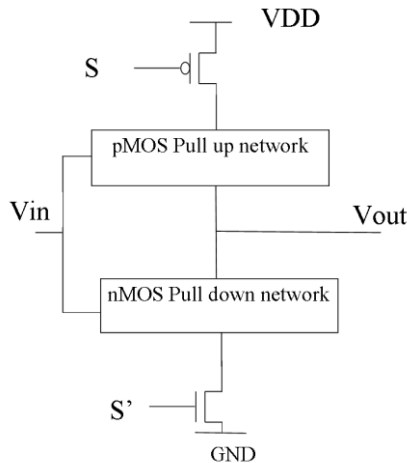


Fig. 8: Sleep Transistor Technique structure

In this technique we have floating values and thus will lose state during sleep mode. The Wakeup time and energy of the sleep technique have significant impact [3]. The technique in which high V_{th} sleep transistor are used called Multi-threshold voltage CMOS (MTCMOS) proposed by Motoh et al. [3].

2.4 Dual threshold transistor stacking technique.

This new technique called dual threshold transistor stacking hybrid version of stack and MTCMOS. It takes the advantage of both techniques i.e sleep transistors are redesigned with stack effect. The size of sleep transistor is reduced. The sleep transistors are designed as a high threshold voltage [1]. Fig. 9 shows the circuit schematic of dual threshold transistor stacking technique

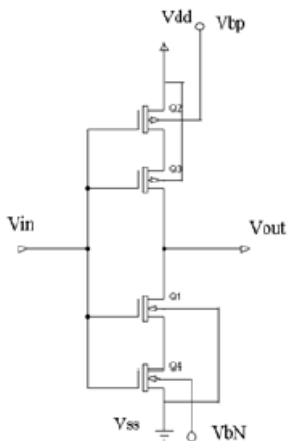


Fig. 9: Dual threshold Transistor stacking Technique structure

2.5 Sleepy Stack Transistor Technique

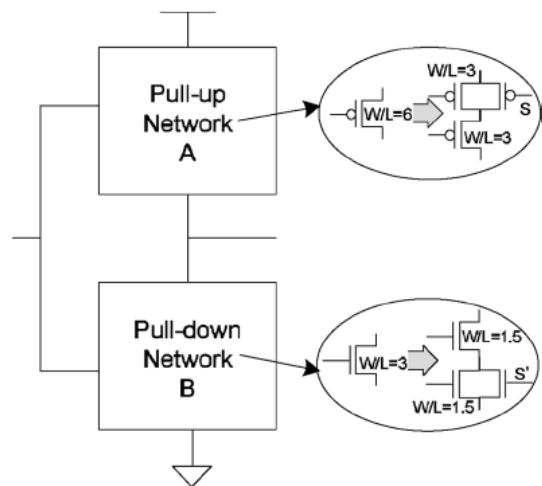


Fig. 10: Sleepy Stack Technique structure [3].

The forced stack and the sleep transistor techniques are combined to get the sleepy stack structure. The function of sleep transistors in sleepy stack is same as of the sleep transistor in sleep transistor technique. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current [3][9]. The drawback of this technique is increase in area.

2.6 Sleepy Keeper Approach

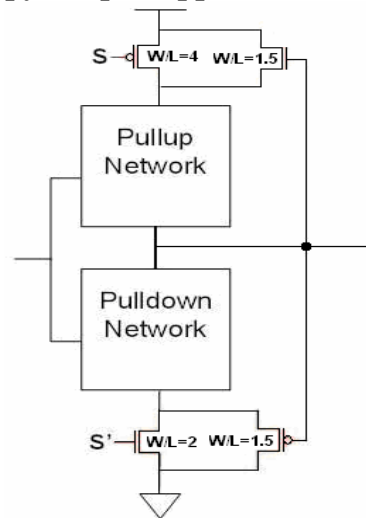


Fig. 11: Sleepy Keeper structure

Sleepy keeper uses leakage feedback technique [9]. PMOS transistors are not efficient at passing GND and NMOS transistors are not efficient at passing VDD.

In this technique, a PMOS transistor is placed in parallel to the sleep transistor (s) and a NMOS transistor is placed parallel to the sleep transistor (s'). The sleep transistors are turned off during sleep mode and transistor in parallel to sleep transistor keep the contact with the appropriate power rail [9].

2.7 Variable body biasing technique

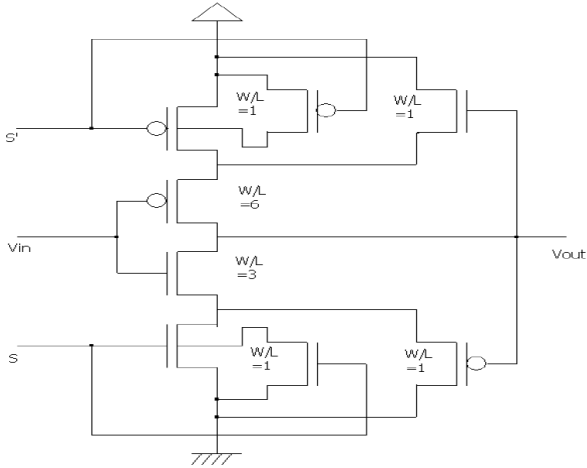


Fig. 12: Structure of variable body biasing technique

The body to source voltage of the sleep transistor is increase in sleep mode to reduce the leakage current. For this in sleepy keeper technique a PMOS and NMOS is added. During sleep mode PMOS is OFF so the body to source voltage of the pull up PMOS is higher than in the active mode. From equation (7), the leakage current decreases as V_{sbl} increases. The body effect, v_{th} also increases due to which performance gets degrade [9]. As shown in fig 12, this technique uses two parallel sleep transistors in pull up network and two parallel sleep transistors in pull down network. For body biasing effect, the source of one of the PMOS sleep transistor is connected to the body of the other PMOS sleep transistor. On the other hand the source of the NMOS sleep transistor is connected to the body of other NMOS sleep transistor. The variable body biasing techniques uses PMOS transistor in GND and NMOS transistor in VDD, both are in paralleled to the sleep transistor for maintaining exact logic state during the sleep mode [9].

3. SIMULATION & DISCUSSION

Simulations have been performed using virtuoso (cadence) in 90 nanometer (nm) gpdk CMOS technology with supply voltage 1.2V to estimate power consumption. The static power consumption, dynamic power consumption and propagation delay measured for different design techniques. Fig. 13 to Fig. 24 shows the resulting schematic diagram, input-output waveforms of each technique. Fig 23 shows the static power consumption, Fig. 25 shows the dynamic power consumption and Fig. 26 shows the propagation delay comparison chart. The static power consumption, dynamic power dissipation, propagation delay for chain of inverter are shown in Fig. 32, Fig. 33 and Fig. 34 respectively.

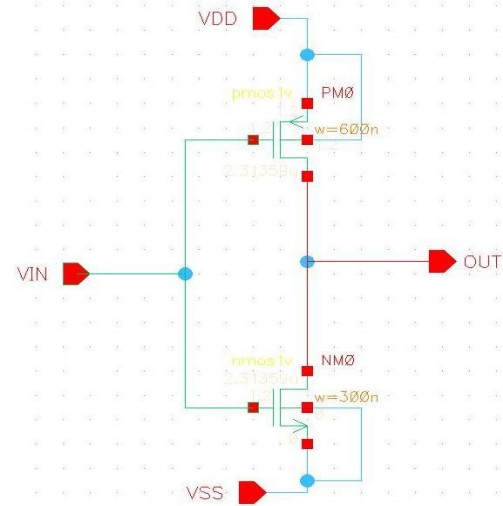


Fig.13: Inverter with Conventional technique.

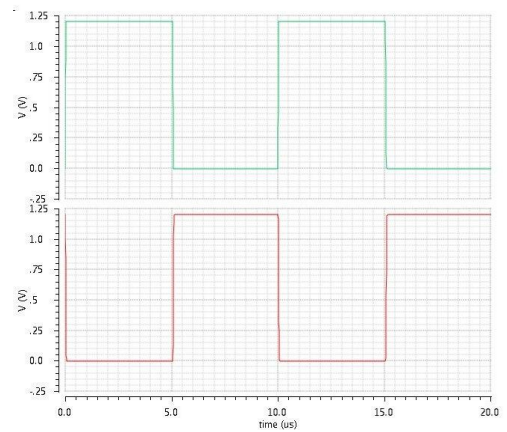


Fig. 14: Input and Output waveform of Inverter with Conventional technique.

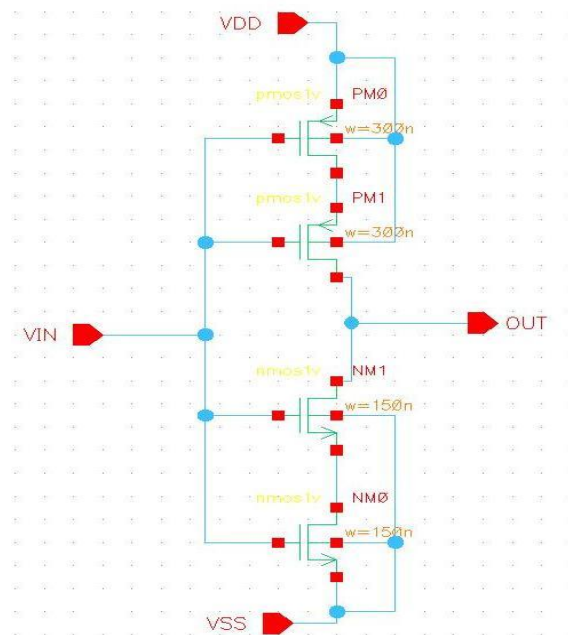


Fig.15: Inverter with stack technique.

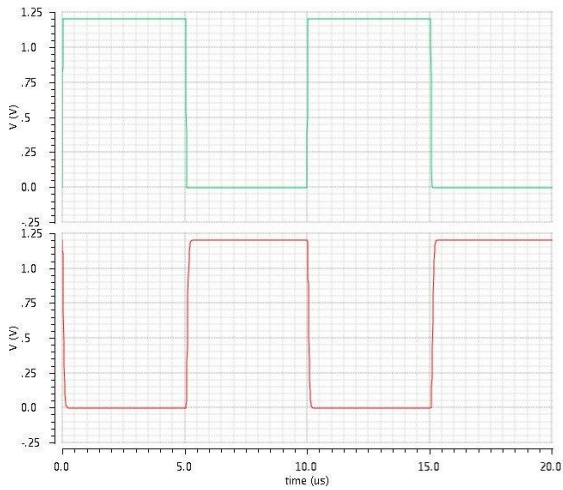


Fig.16: Input and output waveform of Inverter with stack technique.

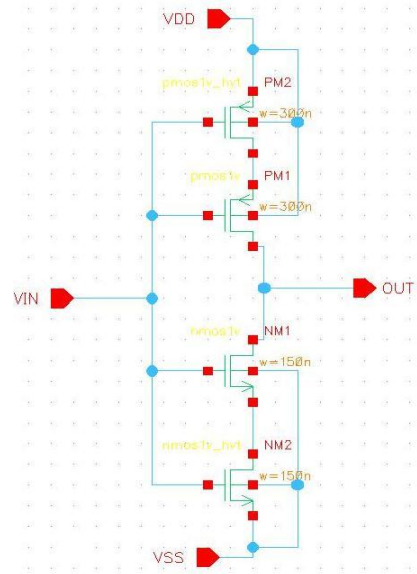


Fig. 19: Inverter with Dual threshold stack transistor technique

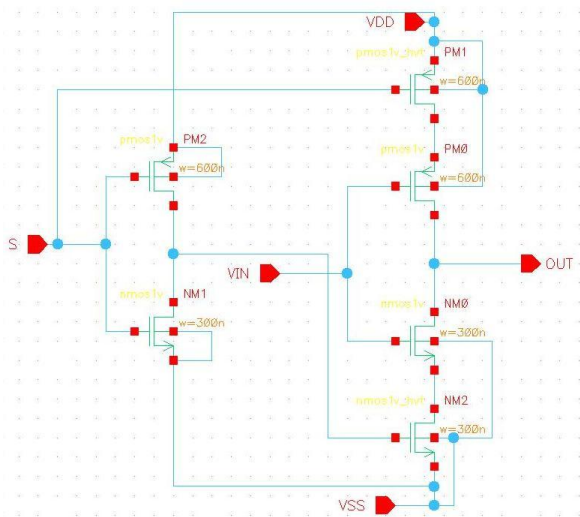


Fig. 17: Inverter with Sleep Transistor Technique.

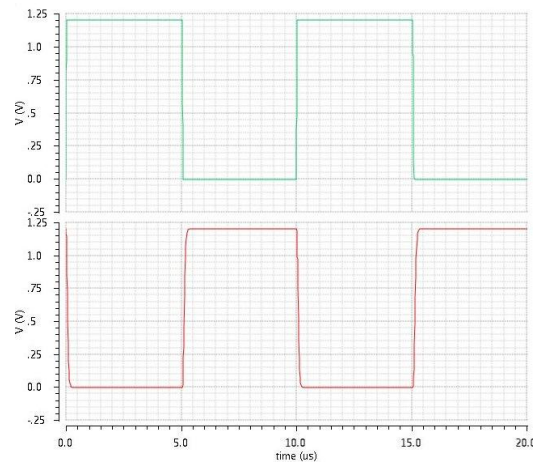


Fig.20: Input and Output waveform of Inverter with dual threshold stack transistor technique.

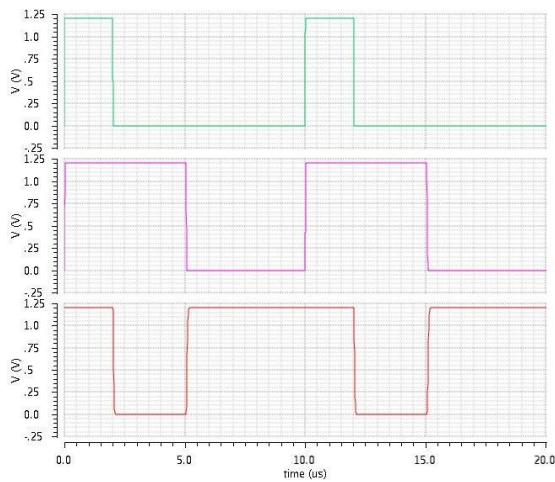


Fig.18: Input and Output waveform of Inverter with Sleep Transistor Technique.

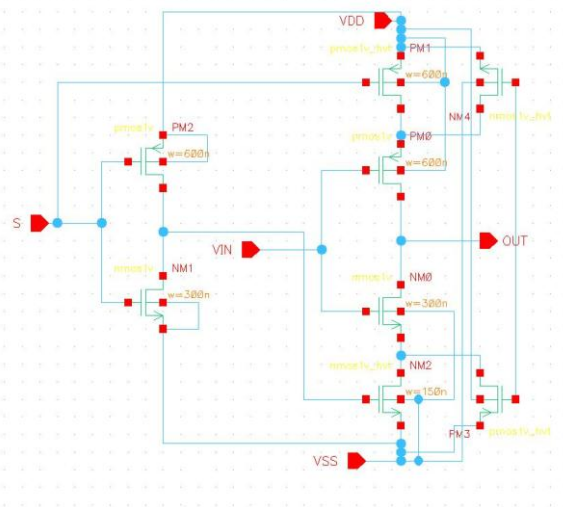


Fig. 21: Inverter with sleepy keeper technique

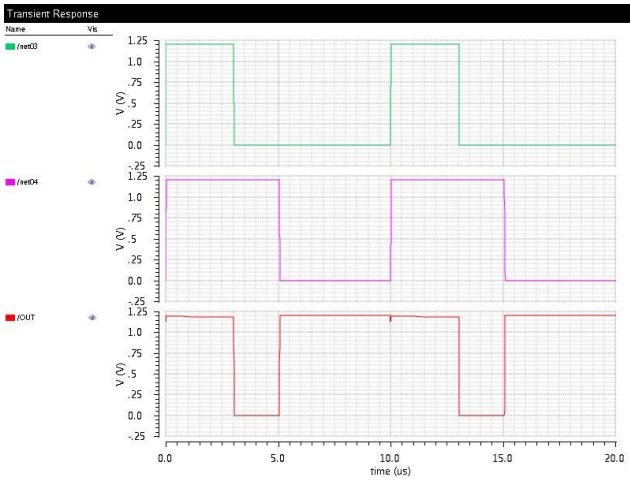


Fig. 22: Input and output waveform of inverter with sleep keeper technique

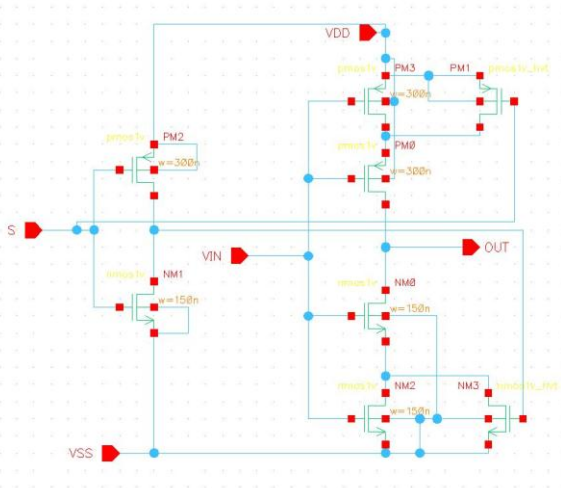


Fig. 23: Inverter with Sleepy Stack Technique

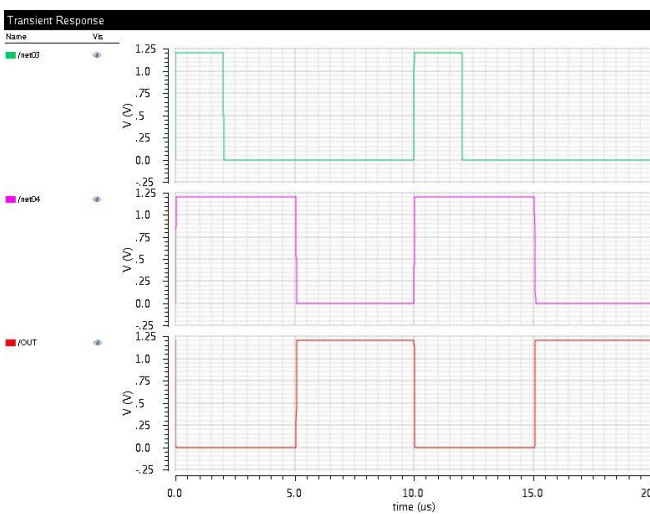


Fig.24: Input and output waveform of Inverter with Sleepy Stack Technique

Table 1: Simulation result for power dissipation and delay

Technique	Dynamic Power	Static Power	Delay
Base Case	8.34E-07	3.20E-09	1.75E-06
Stack	7.33E-07	2.80E-09	1.93E-06
DTTS	7.26E-07	9.78E-10	1.53E-06
Sleep Technique	9.34E-07	1.27E-09	1.75E-06
sleepy stack	1.90E-07	6.53E-10	1.81E-06
sleepy keeper	3.17E-07	1.21E-09	1.63E-06
forced sleep	1.86E-07	1.21E-09	1.40E-06

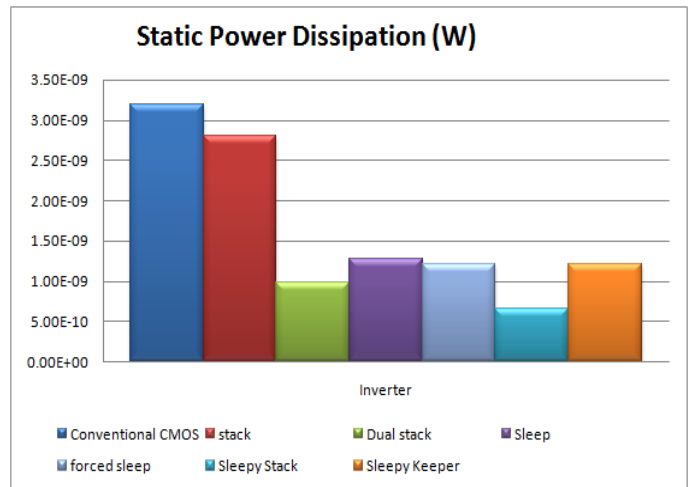


Fig.25: Static Power Comparison.

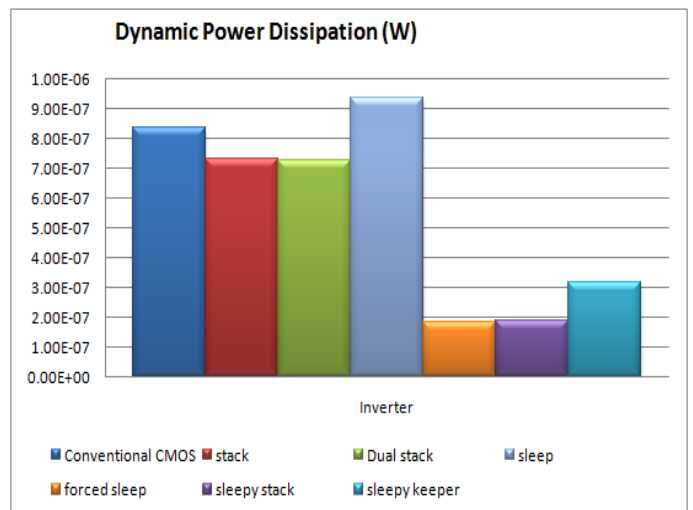


Fig.26: Dynamic Power Comparison.

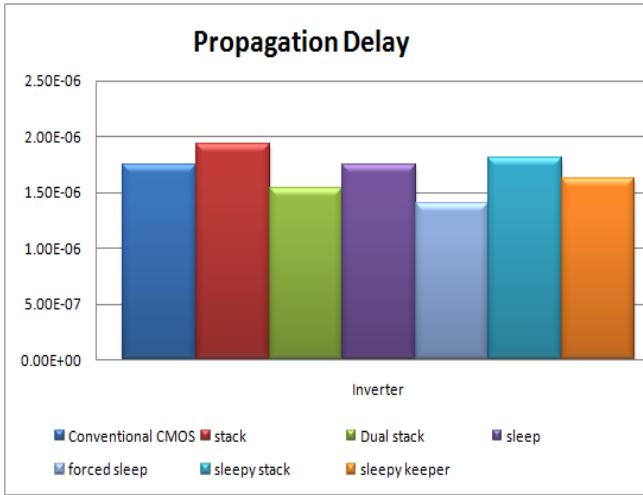


Fig. 27: Propagation Delay Comparison.

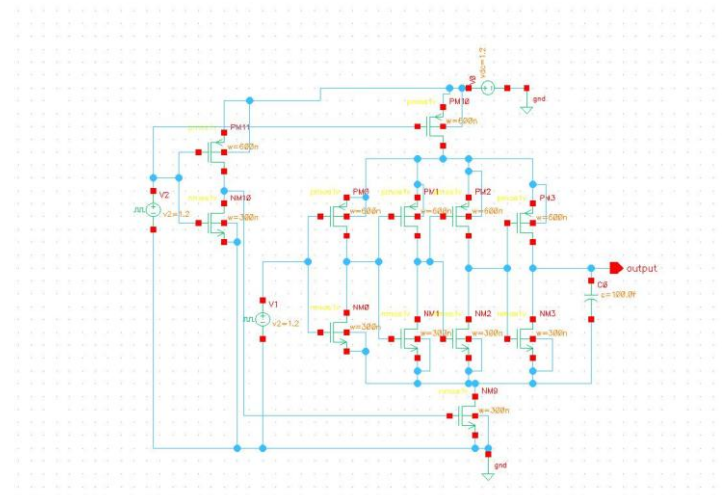


Fig. 30: Chain of Inverter with Sleep Transistor Technique.

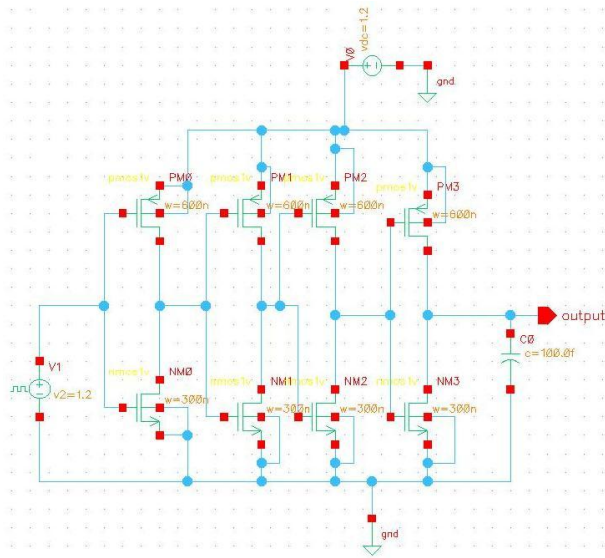


Fig. 28: Chain of Inverter with base case approach.

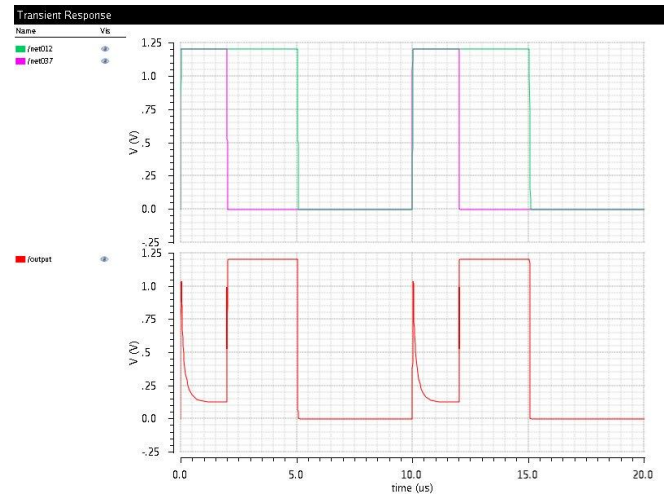


Fig. 31: Input and Output waveform of Chain of Inverter with Sleep Transistor Technique.

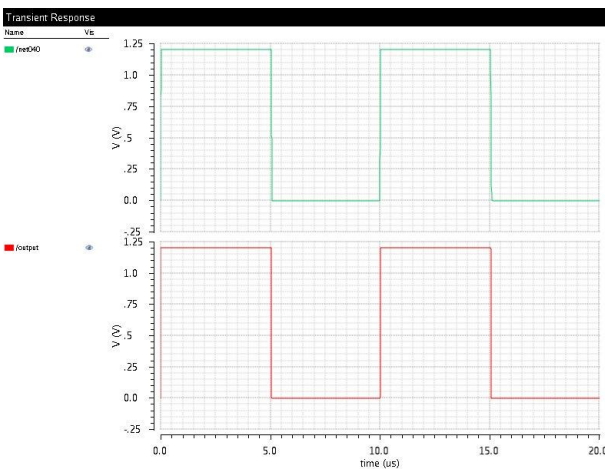


Fig. 29 :Input and Output Waveform of Chain of Inverter with base case approach.

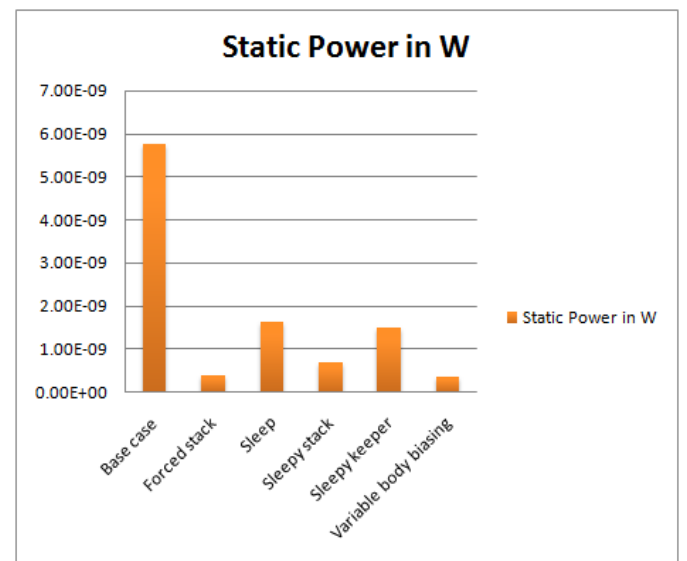


Fig. 32: Static power dissipation chart (chain of inverters)

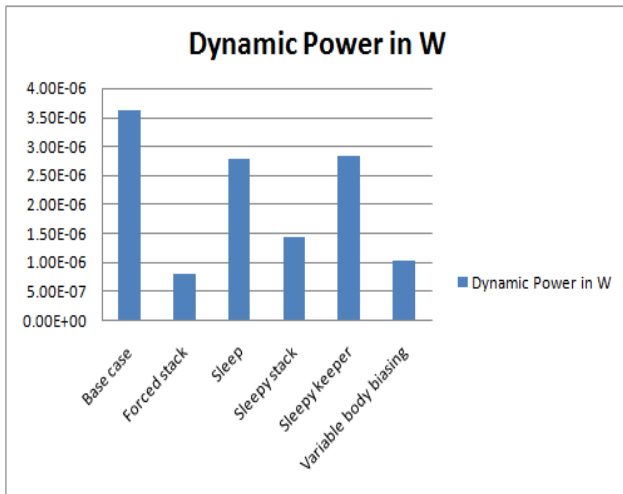


Fig. 33: Dynamic power dissipation chart (chain of inverters)

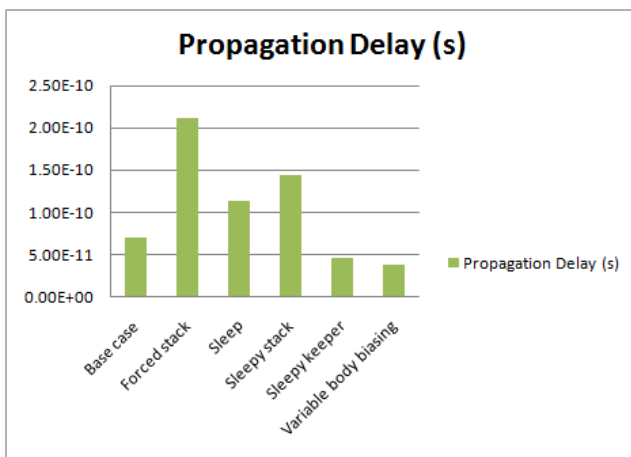


Fig. 34: Propagation delay (Chain of inverters)

4. CONCLUSION

The CMOS inverter is most important and used in all digital as well as analog applications. The optimization of the inverter becomes very important. The leakage power is of great concern for designs in nanometer technologies. As the technology scaling goes below 90nm, the standby leakage power dissipation has become a critical issue. While designing low power circuit different points such as technology, logic implemented and trade off must be taken into consideration. This paper presents a comparative study of different low power design techniques. The variable body biasing technique is a viable solution for designer in designing CMOS VLSI circuit more efficiently.

5. FUTURE WORK

Area of the various approaches using layout and design of various combinational and sequentially circuits using proposed method is to be estimated. The different techniques can be implemented in low power CMOS VLSI circuit to save the power dissipation increasing the battery life.

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