Analysis of Modified Feed-Through Logic with Improved Power Delay Product

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ABSTRACT
A modified approach for Feed-Through logic (FTL) is developed in this paper to provide improved power delay product (PDP). FTL is examined against proposed approach, by analysis through computer simulation. It is shown that the modified FTL has low power consumption and high speed over existing FTL. Based on the performance the given approach is found very efficient for high speed arithmetic or pipelining circuit. Furthermore, the sensitivity of both the approaches is investigated against power supply and capacitive load. Investigation suggests that the given approach has improved delay product over FTL.

General Terms
High speed digital circuit

Keywords
Dynamic Logic Circuit, Feed-Through Logic (FTL), Logic Families, Modified Feed-Through Logic, Partial-Evaluation, Power Delay Product (PDP), Threshold Stability.

1. INTRODUCTION
Recently, FTL are extensively being researched due to its high speed over standard CMOS circuit [1]. It provides high performance operation for delay critical circuit like arithmetic or pipelining circuit [2], [3]. The basic principle of FTL is domino logic but with an additional feature of pre-evaluation of output before all input is valid. This pre- evaluation of output increases the speed of a digital circuit. Moreover, FTL overcomes the shortcomings of domino logic like inability to provide non inverting logic, problem of charge sharing, monotonic nature of output and need of extra inverter at output, with reduced chip area [4], [5].

FTL has numerous applications like direct cascading of dynamic CMOS, to produce differential output, to design iterative networks. This paper presents a modified approach in FTL which results in reduced delay and power consumption as compared to the conventional design. This paper is organized as follows: Section 2 briefly describe the principle of operation for FTL. In Section 3 modified FTL is presented, Section 4 provides analysis of modified FTL and FTL for inverter circuit, Section 5 gives performance analysis of RCA and chain of 3-inverters. Finally, Section 6 gives conclusion.

PRINCIPLE OF FTL
FTL, given in Figure 1, works in two phases, Reset phase and Evaluation phase [1], [2]. It can be shown, when clock is 'HIGH', the output node is pulled to zero value because transistor *Tr* is 'ON' and transistor T_P is 'OFF'. When clock goes 'LOW', reset transistor *Tr* is turned 'OFF' and T_p becomes 'ON' resulting in charging or discharging of output node with respect to input. Reset Transistor T_r always provide 0->1 transition, initially in evaluation phase, therefore outperforms the dynamic CMOS in cascading structure. When dynamic CMOS is cascaded, produced result may be false due to 1-> 0 transition in evaluation phase.

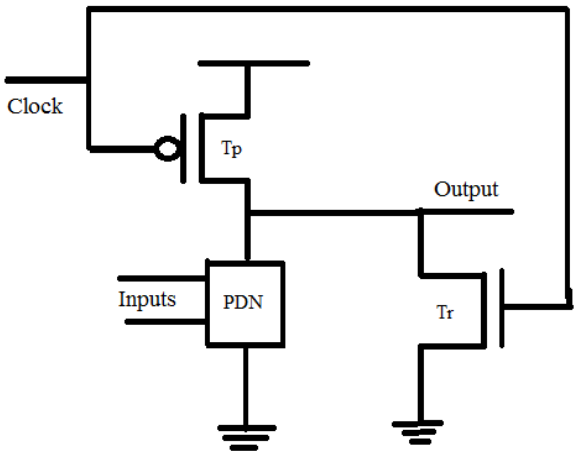

Figure 1: FTL

In Figure 2 cascading of dynamic circuit is shown. When the clock signal falls, the output of a cascaded gate begins to rise up to the threshold voltage V_{TH} of the next gate. At this point all the gates in the circuit are in high gain. This high gain characteristic distinguishes FTL from other logic families. At this point, small variation in input produces large variation in output as compared to other logic families where output changes when input cross the threshold voltage [6]. Therefore, in FTL, with valid inputs, output takes transition either from V_{TH} to V_{OH} or from V_{TH} to V_{OL}. This phenomenon makes FTL fast. In FTL based cascaded system, special care must be taken to avoid dissimilar capacitive load at different output nodes. The effect of dissimilar capacitive load is shown in Figure 3 for a chain of 10-inverters with 1fF capacitive load.

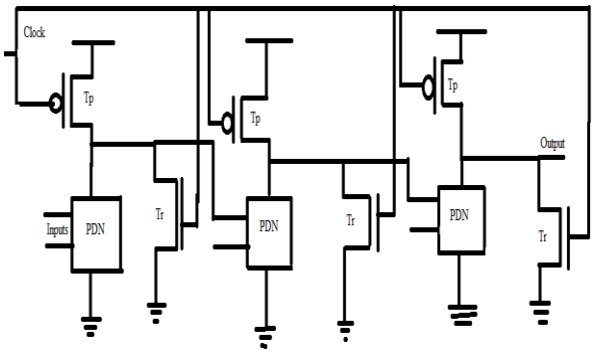

Figure 2: Cascading of FTL logic

2. PROPOSED MODIFIED FTL

Figure 4 presents the modified FTL. Modified FTL is similar to the FTL with an additional NMOS transistor T_a in PDN. The gate of NMOS is driven by V_{DD} as Vgs. The principle of operation of modified FTL is as follows: When clock goes 'HIGH', output is pulled to 'LOW' through reset transistor *Tr*. when clock goes 'LOW', the output is generated according to the given set of inputs with additional transistor T_a always 'ON'.

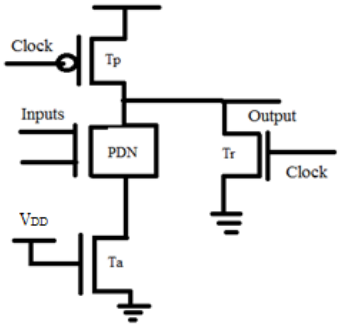

Figure 4: Modified FTL

In this approach, the role of additional transistor T_a is to increases the dynamic resistance of the PDN. Due to which the output node discharges up to V_{OL} value greater than the V_{OL} of FTL. The trade-off in V_{OL} results for less high to low propagation delay from V_{TH} to V_{OL}. In addition to the reduced delay in modified FTL, power consumption also reduces because of increased value of V_{OL}. The dynamic power consumption of a digital circuit is given by

$$P_{dynamic} = \alpha.C_L.V_{DD}.V(x).f_{max} \qquad [5]$$

Here, α is switching activity, C_L is the load capacitance, V_{DD} is supply voltage, f_{max} is the maximum operating frequency and V(x) is the power delivered by the source during low to high transition. Increased value of V_{OL} reduces V(x) in modified FTL. Therefore, modified FTL has lower power consumption than in FTL.

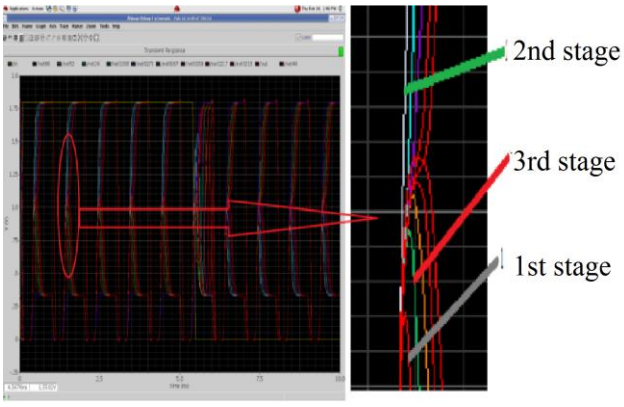

Figure3: Effect of dissimilar capacitive load

(Picture taken by using Cadence Virtuoso tool for 10 stage inverter chain)

4. ANALYSIS OF MODIFIED FTL AND FTL

4.1 Results for inverter

In performance analysis of modified FTL against FTL, we have used 180 nm CMOS process technology model library from UMC, using the parameters for typical process corner at 25 ^oC. Power supply V_{DD} is taken 1.8 V throughout the simulations. Circuits are simulated using Cadence Spectre tool. In this section the performance of inverters based on both approaches is compared. The FTL and modified FTL inverters are shown in Figure 5 and Figure 6 respectively. 1fF capacitive load is taken in the analysis. The values obtained for various performance metrics like propagation delay, power dissipation and power delay product (PDP) are summarized in Table 1.

Table 1: Comparison of FTL and Modified FTL

LOGIC	DELAY (ps)	POWER (µW)	PDP (ps*µW)
FTL	18.6	38.90	723.54
Modified FTL	9.81	38.38	376.50

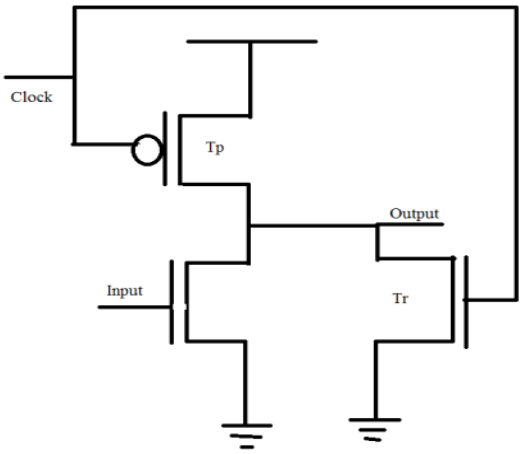

Figure 5: FTL inverter

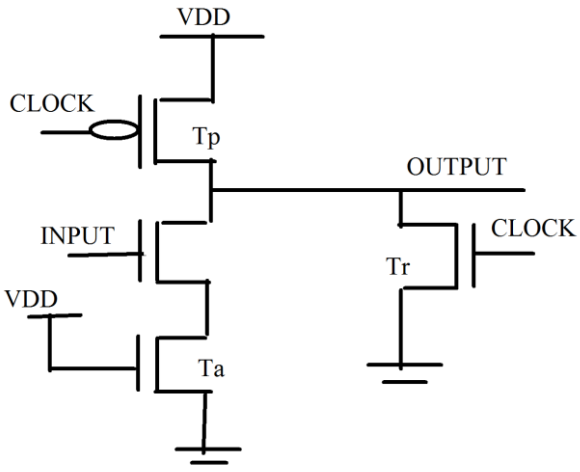

Figure 6: Modified FTL inverter

Hence, the analysis based on results validate the faster operation of Modified FTL than FTL, The Modified FTL is well suited to the applications where the critical paths are made up of cascaded gates such as adders, multipliers, filters and pipelined circuits. The results in Table 1 also confirm less power consumption in Modified FTL as compared to FTL. Furthermore, the reduction in PDP is 47.9% in case of inverter. In addition Modified FTL is well suited to high fan out and high switching frequency applications. PDP of two approaches are compared in Figure 7.

4.2 Sensitivity Analysis of Modified FTL against FTL

This section investigates Sensitivity of Modified FTL and FTL with variation in load capacitance and supply voltage VDD. The respective investigated results are given in Figure 8(a), 8(b) and 8(c). From figure 8(a), It is apparent that irrespective of value of the load capacitance, delay of Modified FTL is lesser than that of FTL. Figure 8(b) shows that irrespective of the capacitive load, Modified FTL always has smaller power consumption as compared to FTL. Figure 8(c) shows variation of delay with supply voltage. The investigation in Figure 8(c) shows that the delay of Modified FTL starts increasing by decreasing supply voltage below .9V. This phenomenon occurs due to high dynamic resistance value offered by Ta at lower VDD. Reader are advised to follow [5, figure 3.27].

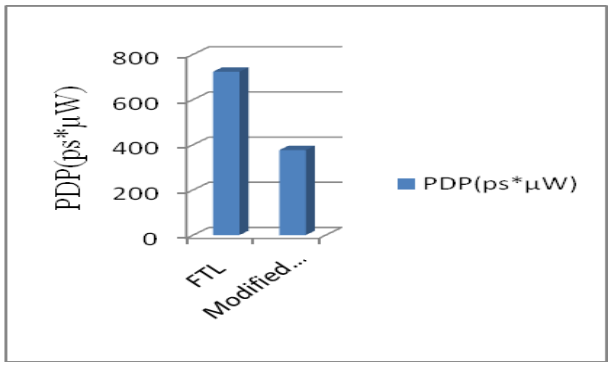

Figure 7: PDP comparison of FTL and Modified FTL logic

For high value of V_{DD}, the resistance becomes independent of V_{DD} and the value of resistance offered is very small but as the value of V_{DD} approaches V_{TH}, the resistance increases exponentially. As a result, the resistance of PDN increases in Modified FTL than in FTL causing higher delay.

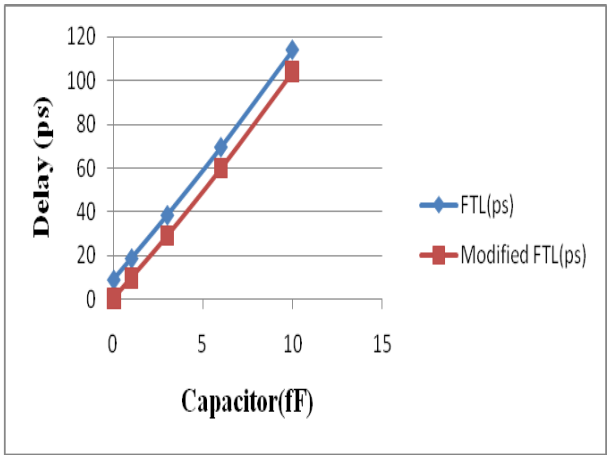

Figure 8(a): Comparison of delay with variation in capacitor load

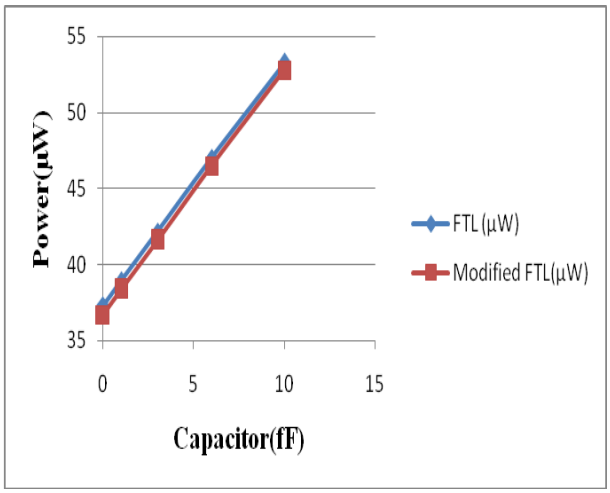

Figure 8(b): Comparison of power with variation in capacitor load

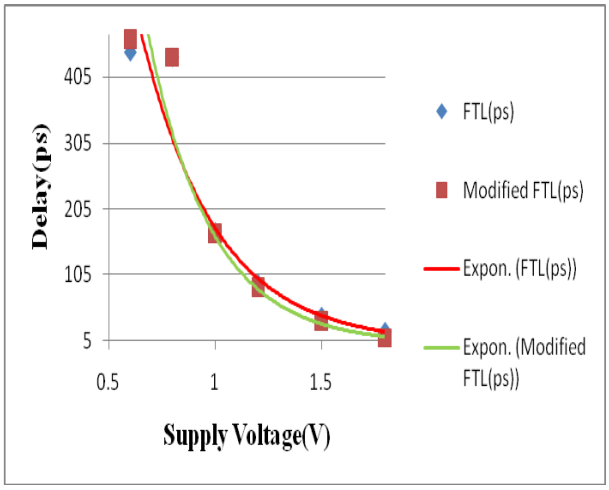

Figure 8(c): Comparison of delay with variation in supply voltage

5. ANALYSIS OF 3-STAGE INVERTER AND 1-BIT RCA

This section compares the results of 3-stage inverter and 1-bit full adder with 1fF capacitive load. To manage the effect of dissimilar capacitive load, 1 fF capacitive load is used at output node. Capacitance of appropriate value at output node also avoids the problem of glitch in dynamic circuit. Circuit diagram considered for the full adder in the analysis can be found in [2, figure 4].The values obtained for various performance metrics like propagation delay, power dissipation and power delay product (PDP) are summarized in Table 2 and 3.

Table 2: Comparing Modified FTL and FTL for 3-stage inverter

LOGIC	DELAY (ps)	POWER (µW)	PDP (ps*µW)
FTL	184.6	116.42	21491
Modified FTL	170.14	115.89	19717.7

Table 3: Comparing Modified FTL and FTL for 1-bit RCA

LOGIC	DELAY (ps)	POWER (µW)	PDP (ps*µW)
FTL	205.416	90.34	18557.28
Modified FTL	168.6	88.59	14939.22

Results in Table 2 clearly verify that the Modified FTL provides lesser delay, lower power consumption and improved PDP for both 3-stage inverter and 1-bit full adder. The reduction in delay for 3-stage inverter is 5.47% with improved PDP by 8.255% whereas for 1-bit full adder delay is reduced by 18.215% and PDP is improved by 19.496%. Figure 9 shows propagation delay versus number of adder bits which also verify faster operation of Modified FTL for different configurations of full adder.

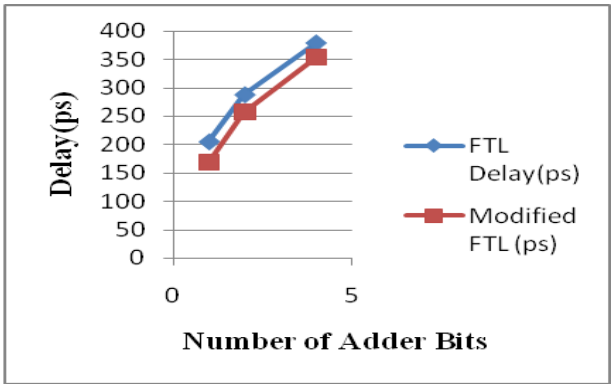

Figure 9: Variation of delay with number of adder bits for FTL and Modified FTL

6. CONCLUSION

In the era of high speed digital circuits FTL gives advantage of having lesser delay and smaller power consumption compared to any other logic families in literature. This paper presented a Modified FTL based on partial evaluation concept. According to the result in tables, Modified FTL is suitable for high speed arithmetic, pipelining and filter circuit design over FTL. Modified FTL also has lesser delay, reduced power consumption and improved PDP.

7. REFERENCES

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