# VHDL IMPLEMENTATION OF MAC BASED DSSS-CDMA PROTOCOL FOR SOLVING NEAR FAR EFFECT IN Ad-hoc NETWORK

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# ABSTRACT

In telecommunications, direct-sequence spread spectrum (DSSS) is a modulation technique like other spread spectrum technologies; transmitted signal takes up additional bandwidth than the data signal which modulates the carrier frequency. DS-CDMA is beneficial for Ad hoc network because it eliminates the requirement for any frequency or time-slot coordination. The main issue in DS-CDMA (Ad hoc network) is the hindrance of a near-far problem. There are two solutions available for reducing this near far effect, first is Power control and second is Medium access problem. In this paper, we focus on medium access problem, for this, we design multiple access interference (MAI) at the protocol level. The aim is that, use "VHDL implementation" for MAC Based DSSS CDMA design, which consist transmitter & receiver with MAC protocol of a Ad-hoc network, which prevent fast degradation of network throughput. In this design, used DPSK modulation technique is non-coherent and has higher BER performance than BPSK. VHSIC Hardware Description Language (HDL) was used for committal to writing of the design. Model Sim Edition 10.2 C was used for functional simulation and logic verification. The Xilinx Synthesis Technology (XST) 14.1 of Xilinx ISE tool was used for synthesis of this project.

# **Keywords**

VHDL, MAC protocol, DBPSK modulator & demodulator, Gold sequence Generator, Direct Sequence Spread Spectrum.

# **1. INTRODUCTION**

Code division multiple access (CDMA) is a channel access methodology utilize by various radio communication technology. One of the ideas in data communication is that the plan of allowing many transmitter to send data at the same time over single line. This enables many users to share a same band of frequency. This idea is termed as multiple accesses [1].

DS-CDMA (Direct-sequence code-division multiple-access) ad hoc networks are accomplished by using direct-sequence spread spectrum modulation whereas the mobiles or nodes of multiple users simultaneously transmit signals within the same frequency band. All signals use the whole allotted spectrum, however the spreading sequences are differ. DS-CDMA is advantageous for ad hoc networks because it eliminates the requirement for any frequency or time-slot coordination [3]. Ad hoc networks have recently been the subject of intensive analysis. The interest in such networks stems from their ability to provide a temporary wireless networking capability in situations wherever fixed infrastructures are lacking and are costly or impracticable to deploy. An ad hoc network is a collection of wireless nodes which are dynamically be started anywhere and anytime while not using any pre-existing network infrastructure [1] .One among the fundamental challenges in Ad hoc networks analysis is the way to increase the overall network throughput whereas maintaining low energy consumption for packet process and communications. The low output is attributed to the harsh characteristics of the radio channel, combined with the contention-based nature of medium access control (MAC) protocols normally utilized in Ad hoc networks [8]. The main focus of this paper is, on raising the network throughput of a Ad hoc networks by means that of a code division multiple access (CDMA) primarily based MAC protocol. Our MAC protocol is shown to achieve a significant increase in network throughput for identical or less energy consumption per delivered packet [2].

VHDL implementation of MAC based DS-CDMA Protocol for ad hoc network has been proposed Paper. In this paper we tend to designed Pilot channel, Synch channel, paging Channel. Traffic channel with MAC frame in forward link of DS-CDMA and recover traffic channel data in receiver end. In this project we use pseudo noise code is generated by gold Code signal is totally different termed as chip signal. Chips modulated by the carrier using a digital modulation technique DPSK. The carrier is generated by using the technique DDFS (direct digital frequency synthesizer). DS CDMA base stations should be able to discriminate this different code sequence, by which separation of transmission can be done [2] .At the receiver end demodulation of the data is done by DBPSK demodulator, after that traffic channel information and detecting original data will be recover from the transmitted data

# 2. LITERATURE SURVEY

The world's 1st cellular networks were introduced in the early Nineteen Eighties, using analog radio transmission technologies like AMPS (Advanced mobile phone System) [7]. The first CDMA networks were commercially launched in 1995, and provided roughly ten times more capacity than analog networks - much more than other multiple access technique. Since then, DS CDMA has become the earliergrowing of all wireless technologies, with over a hundred million subscribers worldwide. This is consistently CDMA technology fits in. CDMA systematically provides better capacity for voice and data communications than other commercial mobile technologies [16].

Several CDMA-based MAC protocols for Ad hoc networks are proposed in past. These protocols, in general, are based on random channel access mechanism, where a terminal with a packet to transmit will proceed directly with its transmission, regardless of the state of the channel [10]. We have a tendency to discuss with such schemes as DS SS CDMA. Under appropriate code assignment and spreading-code schemes, DS-CDMA protocols are absolute to be freed from primary collisions [4]. However, the nonzero crosscorrelations between different CDMA codes will induce MAI (multi-access interference), resulting in secondary collisions at a receiver (collisions between two or more transmissions that use different CDMA codes) [13-19]. This drawback is known as the near-far effect. This will cause a significant reduction in network throughput, and to be overcome this problem designing CDMA-based MAC protocols for ad-hoc network is suggest by author [2].

For the integration of CDMA with ad hoc design various proposal were made in past.

In [1] authors proposed the direct sequence spread spectrum principle based code division multiple access (CDMA) transmitter and receiver is implemented in VHDL language for FPGA. The transmitter section mainly consists of data generator, PN sequence generator, DDFS (direct digital frequency synthesizer), BPSK modulator blocks. The receiver modular mainly consists of BPSK demodulator, PN sequence generator, and matched filters [1].

In [5] author proposed the Implementation of DSCDMA transmitter using Field Programmable Gate Array (FPGA) in this paper. It explains the design for pseudo random PN coding and a direct sequence principle based wireless transmitter. The circuit for the transmitter is comprised of basic digital components, PN sequence code and a BPSK modulation technique. This design was used Verilog Hardware Description Language (HDL) for coding [3].

In all the above protocols, the authors assume perfect orthogonality between spreading codes, i.e., they ignore the near-far drawback.

# **3. PROPOSED PROTOCOL**

### 3.1 **Problem Description**

In this design main drawback with applying DS SS is that the therefore known as near –Far effect. This can be describing by below example [1]. In below figure this result is present when an interfering transmitter is much closer to the receiver than the intended and B is very low, the correlation &collision between the received signal from the interfering transmitter and code A can be higher than the correlation between the received signal from the interfering transmitter and code A. The result's that correct information detection is not possible [2].



## Fig 1: Near Far Effect. 3.2 Reason for Uses Our Protocol

The near far effect is formed within the transmission of DS SS CDMA when a combination of open- and closed-loop power control that ensures that every terminal generates an equivalent signal power at the base station[5]. The base station monitors the received signal power from every terminal and instructs distant terminals to extend their signal powers and nearby terminals to decrease theirs [7]. A below

example shown the power control alone is not enough to reduce the near-far drawback in DS SS CDMA Ad-hoc Network [12].

Example:-

Let dj denote the gap between nodes i and j. suppose that P desires to communicate with Q using a given code and R wants to communicate with S using a completely different code. Suppose that  $dPQ \approx dRS$ ,  $dQR \ll dPQ$ , and  $dPS \ll dRS$ . Then, the MAI caused by R makes it not possible for Q to receive P transmission. Similarly, the MAI caused by P makes it not possible for S to receive R transmission. it is necessary to note that the two transmissions cannot occur at the same time, irrespective of what transmission powers are selected if an increase its power to combat the MAI at Q, then this increased power will destroy the reception at S.[2].



#### Fig 2: Example shown the power control alone is not enough to reduce the near–far drawback in DS SS CDMA Ad-hoc Network

The above Fig. unveils types of varieties of problems [8].

1. Medium access problem: - the use of two different spreading codes to occur at an equivalent time is not possible for two transmissions, this drawback is named medium access problem [2].

2. Power control problem: - if the terminals adjust their signal powers then two transmissions will occur at an equivalent time so the interference caused by one transmission is not large enough to demolish packet reception at different terminals. This is a power control problem [2].

So the solution to the near-far drawback needs to have both elements: power control and medium access. It is necessary here to differentiate between the spreading code protocol and the Medium access control protocol. The former decides which Pseudo noise sequence code is used to spread the signal, but does not solve the contention on the medium [8].

# 4. FPGA DESIGN IMPLEMENTATION

In this paper, uses the VHDL Implementation on Xilinx 14.1 and Model sim Xilinx Edition 10.1C (MXE) tool will be used for functional simulation and logic verification at each block level and system level. The Xilinx Synthesis Technology (XST) of Xilinx ISE tool will be used for synthesis of transmitter and receiver on FPGA.

In DS CDMA transmission user data is spreaded by a PN sequence then modulated using DPSK modulation. Then the modulated signals from different users are combined and transmitted..In the receiver end we demodulated the data using DPSK demodulator then recover the traffic channel information and detecting original data.

In Our project, the following specifications are considered for design and implementation of the MAC Based DS SS CDMA Forward link Tx. & Rx frame for Ad hoc network.

User Data rate	9600 bps
Coding Rate	1/2
PN Chips coded bit	64
PN Chips rate	1.2288 mcps
Modulation symbol rate	19.2 Kbps
Type of PN Sequence	Gold code
Type of Modulation	DBPSK
Walsh code	64×64 matrix
Threshold type	Constant
Ambient temp	25 C
Front end design entity	VHDL
Back end synthesis	Spartan 6
Synthesis software	Xilinx 14.1
Simulation	Modelsim10.2C

### Table 1: following specification consideration for design & Implementation for MAC based DS SS CDMA Forward link for Ad-hoc Network

The main blocks of MAC based CDMA forward link Tx & Rx for Ad hoc network are listed below

- A. Convolution Coder
- B. Symbol repeater
- C. Interleaver & de Interleaver
- D. Long code PN sequence generator-
- E. Decimator
- F. Walsh code
- G. DBPSK modulator & de modulator
- H. Veterbi decoder
- I. MAC frame concept

#### A. Convolution coder

Convolution coding is an alternative to block coding of digital massage. It can offer higher vcoding gain for both hard and soft kind of decoding [15].

Code generation – It is generated by combining the output of a k shift register through the employment of v exclusive or logic summer.



Fig 3: Principal of convolution coder

Consider the convolution coder. It is a rate 1/2encoder with  $V_1 = S_1 \bigoplus S_3$ ,

# $V2 = S1 \oplus S2 \oplus S3$

In any clock k interval the o/p v1 and v2 depends on the bit moved into the encoder at the start of that interval and depends also on the part history. Which the encoder has experienced on the sequence of earlier I/P bits. Past history is recorded in the content of memory bits M1 and M2 [23].

#### **B.** Symbol repetition

For paging and traffic channel repetition depends on the data rate of each channel .A low data rate needs more repeats in order to make up the modulation symbol rate of 19.2 Kbps [14].

#### C. Interleaver

The purpose of using block interleaving is to try to avoid burst errors while sending the data through a multipath fading environment [14].

The interleaving process scatters the bit order of each frame so that if a segment of data is lost during fading .its bit are dispersed throughout the reorganized frame. The missing bits are often recovered during the decoding process.Inetrleving provide effective protection against rapidly changing channel. The below figure shown the interleaver and de interleaver process working [24]. Received Data



Fig 4: Concept of Interleaving and de interleaving process

## D. Long code PN sequence generator

The PN Sequence Generator block generates a sequence of pseudorandom binary numbers using a LFSR. This block implements LFSR using a simple shift register generator. A PN sequence can be used in a pseudorandom scrambler and descrambler. It can also be used in a direct-sequence spread-spectrum system. The long code generator provides privacy by scrambling the message data [18].

## Gold code sequence

M sequence are easy to generate and very use full for FHSS and DSSS system not used for CDMA .for DSSS CDMA M sequence are not optimal for CDMA. for CDMA we need to construct a family of spreading sequence one for each users, in which the code have well-defined cross correlation properties In general M sequence do not satisfy the criterion. One popular set of sequence that does is gold sequence. It is attractive because only simple circuitry is needed to generate a large number of unique codes [21].

A below Figure shown the concept of gold code generator



## Fig 5: Concept of Gold code sequence Generator

Mathematical concept of gold code generator

Suppose we have take M sequence represented by a binary vector[a] of length N, and generated a new seq. [a'].by sampling every qth symbol of [a].we use multiple copies of [a] until we have enough sample to produce a generate sequence of [a']of length N.

The sequence [a'] is said to be a decimation of the sequence [a] and written as [18]

a' = a[q]

For the gold code sequence we meet following condition 1. n mod 4  $\neq 0$ ,

that is all n except 0,4,8,12,16

2. q is odd and  $q = (2^k + 1)$  or  $q = (2^{2k} - 2^k + 1)$  for some k.

3. gcd  $(n, k) = \{1 \text{ for } n \text{ odd},$ 

 $\{2 \text{ for } n \mod 4 = 2\}$ 

For shift register of length n, the cross correlation of the gold sequence produced by preferred pair is bounced by  $|\mathbf{R}| \le 2^{(n+1)/2} + 1$  for n odd and  $|\mathbf{R}| \le 2^{(n+2)/2} + 1$  for n even [21].

### E. Walsh code

Walsh code are most common orthogonal codes used in CDMA application .A set of Walsh code of length n consist of n row of an  $n \times n$  Walsh matrix. That is there are n codes, each of length n.This matrix is defined recursively as follows

W1 = (0) W2n = 
$$\begin{pmatrix} Wn & Wn \\ & & \\ Wn & Wn' \end{pmatrix}$$

Where n is the dimension of the matrix and the over score denotes the logical NOT of the bits in the matrix .the Walsh matrix has the property that every row is orthogonal to every other row and to the logical NOT of every other row [22]. In each case the first row consist entirely of 0s and each of the other rows contain s n0s and n 1s.Recall that to compute the cross correlation, we replace 1 with +1 and 0 with -1[18].In this project used  $64 \times 64$  Walsh matrix.



Fig 6: Physical layer structure MAC based DS SS CDMA Forward link for Ad-hoc Network

# F. Decimator

The decimation is accomplished by essentially using every sixty-fourth bit out of the long code data frame. A 64 time's decimation reduces the data rate of the long code from 1.2288 Mbps to 19.2 Kbps [14].



Figure.7 Concept of Decimator 64:1 &24:1 working

#### G. DBPSK Modulator & De-modulator

in DBPSK system one previous bit used to decided the phase shift of next bit and change in output occurs only if input bit is at logic '1'and no other change occurs if input bit is at logic'0'.therefore one previous bit is always used to define the phase shift in next bit there the symbol is said to have two Differential PSK is a non coherent form of phase shift keying which avoid the need for a coherent reference signal at the receiver. Non coherent receivers are easy and cheap to build and hence are widely used in wireless communication. In DPSK System the input binary sequence is first differentially encoded and then modulated using a BPSK modulator [24].



Fig 8: Block Diagram of DPSK Transmitter & Receiver

bits. The output is passed through a product modulator to obtain the DPSK signal. At the receiver end, the original sequence is recovered from the demodulated differentially encoded signal through a complementary process [25].

A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using a code. There are other algorithms for decoding a convolutionally encoded stream. The Viterbi algorithm is the resource-consuming [24].Viterbi decoders are provided three function : one for variable data rate signals with trail bits; one for fixed data rate signals followed by trail bits; and, one for signals without trail bits. The forward traffic channel Viterbi decoder is designed for decoding and detecting the data rate in forward traffic channel. The reverse traffic channel Viterbi decoder is designed for decoding and detecting the data rate in reverse traffic channel [22].

## I. MAC (medium access control) Protocol

A medium access control (MAC) protocol moderates access to the shared medium by process rules that allow these devices to communicate with each other in an orderly and economical manner [10]. MAC protocols so play an important role in enabling this paradigm by ensuring efficient and fair sharing of the scare wireless bandwidth.



Fig 9: Working principal diagram of MAC

In the RTS/CTS algorithm, the node which wants to send frames sends a RTS frame to the destination node first, and after the destination node responds with a CTS frame immediately. It is when the source node receives the CTS transmitted from destination node accurately; the source node is allowed to transmit frames. Whenever the source node receives the CTS, it initiates the transmission of data. In order to face the unreliability of the channel, the MAC protocol [20] adds a positive acknowledgement (ACK) upon the reception of a data packet [9].

# 5. SIMULATION & RESULT

### 5.1 Synthesis report

This section studies the device utilization on Virtex4 FPGA for different designs. After the designs were compiled, the report option of Xilinx synthesis tool determines preliminary device utilization and performance. The device utilization results for all three designs are depicted in below table. In below table shown the synthesis report project status & device utilization summary.

Receiver1cdma Project Status (04/15/2013 - 17:40:11)					
Project	newcode.xis	Darsor Errors	No Errors		
File:	e	raiser Enois.	NO EIIOIS		
Module	receiver2cd	Implementatio	Placed and		
Name:	ma	n State:	Routed		
Target	xc6slx4-	Errora	No Errora		
Device:	3tqg144	EII0IS.	NO EIIOIS		
Family	Spartan 6	Top level	ны		
Panny	Spartan	source type	IIDL		
Product	ISE 1/1 1	Warnings	No		
Version:	101 14.1	wannigs.	Warnings		

Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	All Constraints Met
Environm ent:	System Settings	Peak Memory Usage:	143 MB

#### Table 6.2.1: Project status in design & Implementation for MAC based DS SS CDMA Forward link for Ad-hoc Network

In this below table show the device utilization in our VHDL implementation On MAC based DS CDMA protocol for Ad-hoc network. In this below table shown, no. of utilization component in our implementation.

Device Utilization Summary					
Slice Logic Utilization	Used	Slice Logic Utilization	Used		
Number of Slice Registers	43	Number of LUT Flip Flop pairs used	102		
Number used as Flip Flops	40	Number with an unused Flip Flop	64		
Number used as Latches	3	Number with an unused LUT	3		
Number of Slice LUTs	99	Number of fully used LUT-FF pairs	35		
Number used as logic	99	Number of unique control sets	11		
Number using O6 output only	85	Number of slice register sites lost to control set restrictions	53		
Number of occupied Slices	30	Number of bonded IOBs	10		
Average Fan-out of Non-Clock Nets	5.18				

Table 6.2.3: Device utilization summary in design & Implementation for MAC based DS SS CDMA Forward link for Ad-hoc Network

# 5.2 Simulation Result

In this design, use the VHDL Implementation on Xilinx 14.1 and Model sim Xilinx Edition 10.1C (MXE) tool will be used for functional simulation and logic verification at each block level and system level. After that, the generated schematic can be verified using simulation software which shows the waveforms of inputs and outputs of the circuit after generating the appropriate test bench.

After simulation VHDL implementation produce the RTL schematic of the desired circuit. After that, the generated schematic can be verified using simulation software which shows the waveforms of inputs and outputs of the circuit after generating the appropriate test bench.



#### Fig 11: RTL Internal view of MAC based DS SS-CDMA Forward link

An RTL description is usually converted to a gate-level description of the circuit by a logic synthesis tool. The synthesis results are then used by placement and routing tools to create a physical layout



Fig 11: RTL top level modelling view of MAC based DS SS-CDMA Forward link

In below simulation result is shown in gold code sequence. In this design gold sequence is constructed by the X-OR of two M bit sequence (generated by two shift register (shift1 & shift2)) with the same clock rate as shown in figure (clk signal), and then two M bit sequences are bitwise X-OR ed giving the resultant of gold code sequence (gold seq signal).



Fig 12: Simulation result of gold code sequence in MAC based CDMA



# Fig 13: Simulation result of DBPSK Modulator in MAC based DS SS-CDMA Forward link

In this waveform of DPSK modulator used at transmitting end is shown in above fig 13. In this wave form the output signal is shown by mod op signal. If incoming bit is high, the output is same as carrier; if it is low, the output is 180 phase shifted version of the carrier signal.



Fig 14: Simulation result of DBPSK Demodulator in MAC based DS SS-CDMA Forward link

In the result window shown the received modulated sample is shown in (Fig 14) the "modop" signal now as for the digital bit received the complete waveform of 64 samples is obtained, question remains that how to detect the signal whether it is '1' or '0' it actually depends on the phase of the received waveform. The phase of the received waveform is detected by comparing the signal with the delayed form of the same signal. "modop" delayed result is obtained in "modop1" and "modop1" delayed signal is obtained in "modop1", comparing the "modop" with "modop1" and "modop1" is compared with "modop2" to yield the phase recognition result for the obtained waveform if the comparative result shows a negative output it means the waveform is moving towards the negative quadrant and if the comparative result shows a positive output it means the waveform is moving in the positive quadrant hence depicting the respective phase angles of the signal and hence providing the bit information.



Fig 15: Simulation result of near far effect in DS SS-CDMA Forward link for Ad-hoc network

As indicated through simulation result in the fig-15 receiver is in the receiving range of Tx (modulator C1 and modulator C2). The intended transmitter that should transmit the data to the receiver must be the modulator C1. But due to the near far problem and increase in power capability of the modulator C2, receiver start receiving the data from the non intended modulator C2. This effect is shown in the simulation results and hence the problem persist in the design of the CDMA system.





In Fig-16, the proposed MAC based DS CDMA solution provides a methodology in which after receiving the MAC ID from the transmitters the receiver firstly checks for the destination MAC in the received signal and if the ID matches with the self ID of the receiver it will allow the transmitter to send the data further. This will always restrict the non intended transmitter to transmit the data to the non intended receiver by providing the transmitter the information to reduce its power for transmission if the MAC ID comparison match fails. This result is also shown.

As the code is developed in VHDL language and design is simulated on Xilinx software we are merging up both transmitters in the receiver module to demonstrate the near far problem. Model simulation results in perfect demonstration of the Near Far Problem and the MAC solution shows the comparison of the MAC ID with received MAC and then reception of the correct and intended data from intended transmitter.



Fig 16: Xilinx ISE 14.1 Power analyzer report for MAC based DS SS-CDMA Forward link for Ad-hoc network

These results could further be verified on a FPGA Hardware in digital domain to show the MAC solution working perfectly for the transmission and reception of intended units only. As the simulation results are verified the hardware results will work accordingly.



The obtained result tabulated in the sheet is derived from the samples of the resultant output of receiver. The output 1 show resultant samples of MAC based output whereas Output 2 shows resultant output of the non MAC based output samples plotting and comparing them on time reference will provide the achieved accuracy and correction graph between the both .clearly MAC results is far better than the non MAC result.

# 6. CONCLUSION

In this paper implemented a DS SS CDMA-based medium access protocol with transmitter & receiver for ad- hoc networks using VHDL language. Project design has been tested by Modelsim 10.2C. For FPGA implementation design has been synthesised on Xilinx ISE 14.1, Spartan 6 device. We found that it adjusts the desired transmission for data packets to permit for interference-limited simultaneous transmissions, so that receiver terminal gets the data only due to intended Tx. In this design used DPSK modulation & de modulation, which avoids the need for a coherent reference carrier signal at the receiver. It reduces the receiver complexity & half bandwidth requirement as compared to BPSK modulation for same bit rate. This protocol reduces the energy consumption along with successfully delivery to a packet from the source to the destination. Also this protocol is providing a solution to the near-far drawback in DS SS CDMA ad hoc systems at the protocol level & at the same time also increases the throughput of network and reduce the hidden and exposed terminal drawback.

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