Design of High Performance and Power Efficient 16-bit Square Root Carry Select Adder using Hybrid PTL/CMOS Logic

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ABSTRACT
In today's techno-savvy world the need of the hour is to develop devices which are power efficient as well as occupy very less area. VLSI circuits have proved to be the vital choice for most of the design engineers in order to reduce power consumption in any device. The most basic operation in any processor circuitry involves addition. Carry Select Adder (CSA) is a high speed adder and its structure reveals that there exists a possibility of reducing area and power dissipation of the circuit. This paper presents power and delay analysis of 16-Bit Square Root CSA implemented through Hybrid PTL/CMOS logic .It examines the performance of the proposed design in terms of area, delay, power in 90nm CMOS process technology. The result shows that proposed Square Root CSA structure is better in terms of area, power and Power Delay Product (PDP) than others.

Keywords
Power dissipation; PDP; adders; hybrid PTL/CMOS

1. INTRODUCTION
An arithmetic operation carried out at a high speed has always been the native requirement of high performing processors. In digital framework, speed of addition is always restricted by the time taken to propagate the carry through the adder. The output sum for each position of the adder is generated after the bit positions of the previous adder has been summed and carry propagated into the next stage. In order to overcome this problem of carry propagation delay, CSA is used which makes use of multiple pairs of Ripple Carry Adder to generate sum and carry by using carry input and hence the final sum and carry are selected through the multiplexer using carry of the previous stage as select line. To overcome the disadvantage of duplication of hardware in CSA, Square Root CSA is used in which lower set of Ripple Carry Adders are replaced by Binary to Excess-1 code converters(BEC) thereby improving speed of addition and lower power dissipation. The advantage of BEC is that it uses less number of logic gates in comparison to Full adder. The proposed structure is implemented using Hybrid PTL/CMOS logic style thereby attaining better results in terms of area, power, delay and PDP.

2. BASIC FUNCTION AND STRUCTURE OF BEC LOGIC
The basic aim is to use Binary to Excess-1 code converter (BEC-1) instead of Ripple Carry Adder (RCA) with Carry initial (Cin) equal to 1 as in case of CSA. BEC logic is implemented because it makes use of lesser number of logic gates than RCA thereby circuit consume less power and has lower area. A (n+1)-bit BEC is required for the corresponding n- bit RCA. BEC logic is explained below

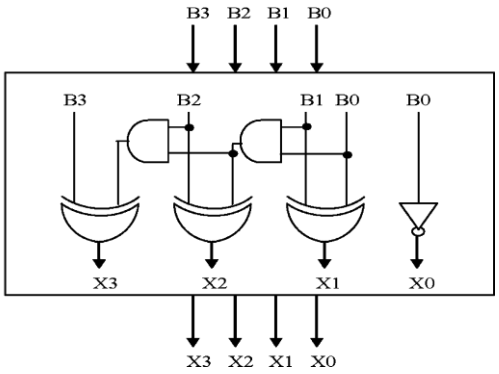

Figure 1: 4 bit Binary to Excess -1 converter [1], [2]

Following are the Boolean equations of the 4-bit BEC converter. Note the Boolean symbols (~ representing NOT, ^ representing XOR, & representing AND)

X0 = ~B0
X1 = B0^B1

X2 = B2^ (B0 & B1)
X3 = B3^ (B0 & B1 & B2)

Table 1. Truth Table of 4-bit BEC logic [1], [2]

B[3:0]	X[3:0]
0000	0001
0001	0010
|	|
	|
1110	1111
1111	0000

3. STRUCTURE OF REGULAR 16-BIT SQUARE ROOT CSA

A 16-bit CSA can be implemented using variable block size concept or using uniform block size concept. A 16-bit CSA using uniform block size has a delay of 4 full adders and 3 multiplexers while using variable block size has a delay of 2 full adders and 4 multiplexers. Therefore we make use of variable block size to implement Square Root CSA using Hybrid PTL/CMOS logic. A CSA makes use of RCA in order to generate sum and carry using initial carry as 0 and 1 respectively .Every CSA stage is divided into 2 sections with upper RCA fed with Cin=0 while lower RCA fed with Cin=1.The carry from the previous adder is used to select the sum and carry output of its next stage. If the previous carry is zero then sum and carry of the upper RCA is selected while if the previous carry is one then sum and carry of lower RCA is selected. It is done with the help of multiplexer. Each RCA pair in CSA is used to compute the value of sum before the previous carry comes in. Hence the delay gets considerably reduced in case of Square root CSA.

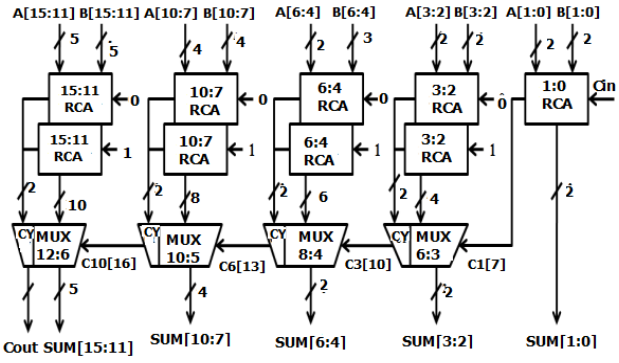

Figure 2: Structure of regular 16-bit square root CSA [1]

4. HYBRID PTL/CMOS LOGIC STYLE

Pass transistor logic (PTL) style is considered to be better than CMOS logic style because it makes use of less number of gates thereby resulting in less delay and hence less power dissipation [3],[4],[5],[6],[7].Restoring logic is required to obtain full swing output thereby resulting in increase in the power dissipation of the circuit. As CMOS and PTL have their respective merits and demerits therefore a combination of both that is HYBRID PTL/CMOS would give best results in terms of power, area, PDP. Logic functions in Hybrid PTL/CMOS are represented through BDD (Binary Decision Diagram) [5], [6].

5. STRUCTURE OF MODIFIED 16-BIT SQUARE ROOT CSA

Modified 16-bit Square Root CSA structure involves replacing lower n-bit RCA in Regular 16-bit Square Root CSA with (n+1)-bit BEC. Implementation of the modified structure has been done using CMOS logic style, PTL logic \style and Hybrid PTL/CMOS logic style. Figure 3 depicts the modified structure. While implementing HYBRID PTL/CMOS logic in the below structure PTL logic is used to implement bitonic circuits like XOR, Multiplexer etc while CMOS logic is used to implement monotonic circuits like AND,OR,NOT etc.

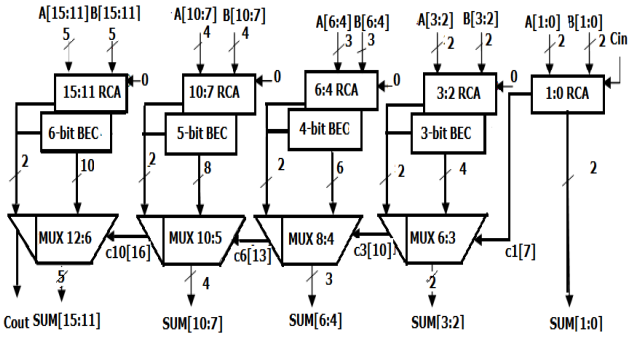

Figure 3: Structure of Modified 16-bit Square Root CSA which has been implemented through Hybrid PTL/CMOS logic style [1], [8].

It has been found that structure shown in Figure 3 gives least power dissipation and PDP when implemented through Hybrid PTL/CMOS logic style.

6. SIMULATION RESULTS

Implementation of 16-bit Square Root CSA is done on Predictive Model Beta Version 90nm CMOS technology. PDP comparison graph has been shown in Figure 4 while Power Dissipation comparison graph has been shown in Figure 5.The result have been obtained over various supply voltage (V_{dd}) .Table 2 depicts simulation results of power dissipation and PDP.

7. CONCLUSION

Integrated Circuit design which involves minimum number of logic gates and minimal power dissipation is considered to be good for the overall design. Hence implementation of modified 16 -bit Square Root CSA using Hybrid PTL/CMOS logic style gives least power dissipation, least PDP and uses less number of logic gates in comparison to when implemented though static CMOS logic style and PTL style. Thus reduction in the number of gates results in reduction in the overall area of the circuit. The comparison result shows that power dissipation of the modified Square Root CSA when implemented through Hybrid PTL/CMOS gets reduced by 17.3 to 32.9 % while PDP gets reduced by 17 to 32.6% in comparison to when implemented through CMOS and PTL logic style.

Carry Select Adders	**Power Dissipation(Watts)**					**Powers Delay Product (Watts.sec)**				
	Supply Voltage (V_{dd})									
	0.8v	1.5v	2v	2.5v	3v	0.8v	1.5v	2v	2.5v	3v
CMOS Style	1.869E -05	1.748E -04	6.806E -04	8.174E -04	2.402E -03	1.756E -13	7.456E -14	7.427E -12	9.064E -12	2.643E -11
PTL Style	1.650E -05	1.540E -04	4.242E -04	9.135E -04	1.736E -03	1.679E -13	3.546E -14	3.313E -12	1.014E -11	1.914E -11
Hybrid PTL/CMOS Style	1.405E -05	1.379E -04	3.753E -04	7.993E -04	1.504E -03	1.456E -13	1.518E -12	4.155E -12	8.842E -12	1.779E -11

Table.2 Power Dissipation and PDP comparison of CSA's implemented using various logic styles over supply voltage range.

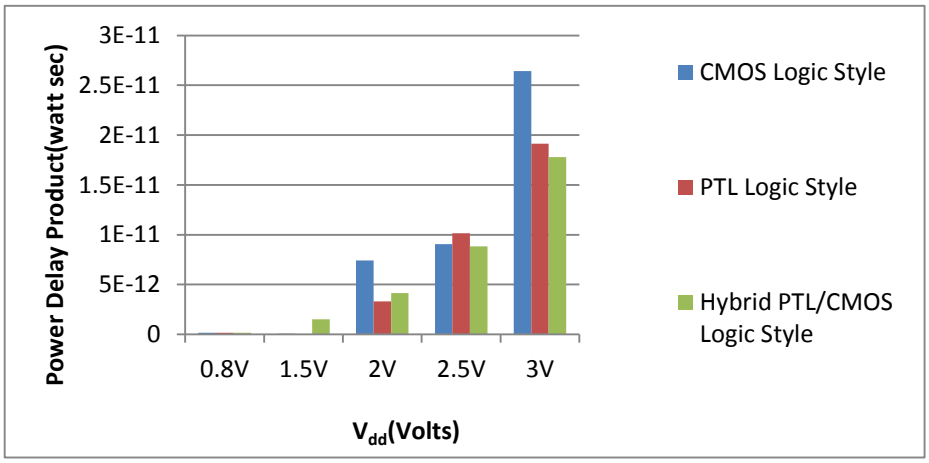

Figure 4: PDP comparison of modified 16-bit Square Root CSA using 3 logic styles.

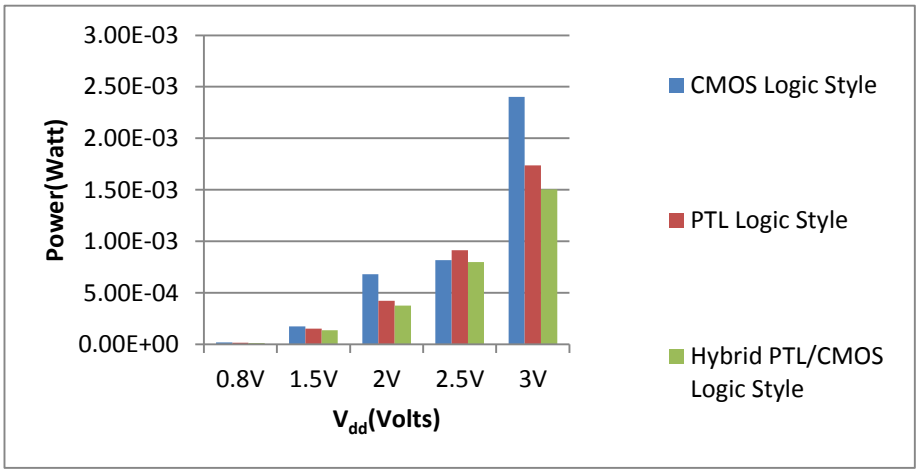

Figure 5: Power Dissipation comparison of modified 16-bit Square Root CSA using 3 logic styles.

8. ACKNOWLEDGMENT

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