Area Efficient High Speed and Low Power MAC Unit

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ABSTRACT

With the growing importance of electronic products in day-to-day life, the need for portable electronic products with low power consumption largely increases. In this paper, an area efficient high speed and low power Multiply Accumulator unit (MAC) with carry look-ahead adder (CLA) as final adder is being designed. In the same MAC architecture design in final adder stage of partial product unit the carry save adder(CSA), carry select adder(CSLA) and carry skip adder(CSKPA) are also used instead of CLA to compare the power and performance. These MAC designs were simulated and synthesized using Xilinx 8.1. The simulation result shows that the MAC design with CLA has area reducing by 16.7%, speed increase by 1.95% and the consumed power reducing by 0.5%.

Key words: Low power, Multiplier and Accumulator, Carry Save Adder, Carry Look-ahead Adder, Carry Select Adder, Carry Skip Adder.

1. INTRODUCTION

Now-a-days, there is a huge demand for portable electronic products. The electronic products with low power consumption like cellular mobiles, laptops and other portable communication devices would surely lead the market trend [1]. The MAC operation is the main computational operation in all digital designs. The speed of the processor mainly depends on the speed of the MAC unit. Development of high speed and low power MAC structure is thus very important for any real time processing application.

The basic MAC structure consists of a partial product bit generation unit, a partial product bit compression unit and a final adder. Both the partial product reduction network and the accumulator unit require an addition operation that involves a long path for carry propagation. In the final addition operation of MAC structures, if carry propagation adder is used, the delay is increased. Since carry propagation is a time-consuming operation.

To reduce this delay, a carry save adder is used instead of a carry propagation adder. But the power consumed by a carry save adder is equal to that of the carry propagation adder. In order to reduce the power consumption, different adder designs are used. In this work the final adder stage of the partial product unit is implemented using four types of adders like the carry skip adder, carry save adder, carry select adder and carry look-ahead adder are compared in terms of area, power and speed. The simulation results revealed that the MAC structure with CLA adder has the minimum area, reduced power and increased speed compared to other designs.

1.1 Related Work

In [1], a high speed energy efficient two cycle MAC architecture is used and it achieves 31% improvement in speed and 32% reduction in energy. In [2], a high speed Booth encoded parallel multiplier design is presented and it achieves 25% improvement in speed and average delay reduces by 8%, compared to binary-tree based conditional-sum adder. In [3], a reduced area multiplier is made use of which requires 3 to 8% lesser area than equivalent Wallace multiplier, and 15 to 25% lesser area than equivalent Dadda multiplier. In [4], a high speed area efficient MAC unit is presented and the area reduced by 6.25%, 3.2% and 2.5% and speeds increased by 14%, 16% and 19% for 8bit, 16bit and 32bit MAC unit respectively, compared to previous merged MAC design [5]. In [6], a 64x64 bit iterative multiplier is utilized and a carry save adder is used to accumulate partial products which reduces area and is fabricated in a 1.6µm CMOS process. In [7], the conventional modified Booth and Baugh-Wooley array multiplication algorithms are applied to the implementation of asynchronous parallel multiply accumulate arithmetic architecture. In [8], speed optimized parallel multiplier algorithm generation is presented and in this algorithm partial product reduction is achieved by vertical compression slice (VCS). In [9], improvement of speed of parallel decimal multiplication using double BCD multiple computation approach, for partial product generation is presented. In [10], high speed multiplication algorithm is presented in which both multiplicand and multiplier are redundant binary integers used to generate partial products. In [11], multiplexer based pipelined array multiplier is presented. In [12], radix2 modified Booth algorithmic approach is implemented in parallel multiplier accumulator where CSA is used as final adder. In this paper, the MAC design with CLA adder offers improvement in all the three key parameters, i.e., reduction in area, increased speed and less power consumption.

The rest of the paper is organized as follows. In section 2, a brief about carry skip adder[13], carry save adder, carry select adder[13] and carry look-ahead adder are given. In the same section general structure of MAC unit is also given. Also the same MAC structure with all above said four adder used for comparison. Section 3 provides the results obtained. Section 4 concludes the paper.

2. MAC UNIT

The general MAC operation can be shown by the equation

$$Z=A \times B + Z$$

where A is the multiplier and B is the multiplicand. A and B each having ‘n’ number of bits. Addend Z has (2n+1) bits. The MAC unit comprises of multipliers and an accumulator. Multipliers consists of three blocks namely the partial product(PP) generation, summation tree and the final adder [1] as shown in Fig 1. The total power consumption of MAC

unit varies with the type of summation network used and the type of adder used in final adder stage.

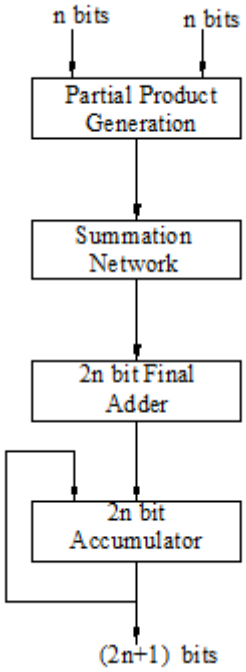

Fig 1 : General Block diagram of MAC unit

Carry chains form the critical path in any full adder circuit. Various architectures have been reported in literature to optimize the average power. These architectures vary in performance and power consumption. Hence in this work, an attempt is made to design MAC units with four types of adders namely carry skip adder, and carry save adder, carry select adder and carry look-ahead adder in the final adder stage of partial product unit and their area, power and delay are compared.

2.1 Carry Skip Adder

The structure of carry skip adder is as shown in Fig 2. Carry Skip Adder divides the word to be added into groups of equal size bits. Carry propagation P_i signals may be used within a group of bits to accelerate the carry propagation. If all the P_i signals within group are P_i=1, the carry bypasses the entire group as in Fig 2. Power consumption and combined path delay are more than all the other three adders.

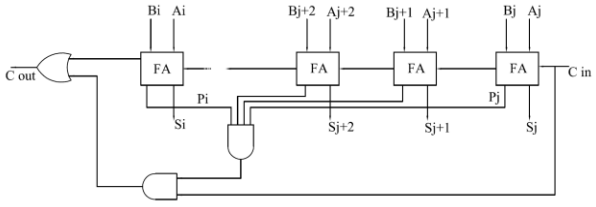

Fig 2: Carry Skip adder

2.2 Carry Save Adder

The structure of carry save adder is as shown in Fig 3.Functionally CSA is identical to full adder. The critical delay path in adders is carry chain. Hence the adder design must be with less carry chain path. But in CSA there are more than single carry chain paths. CSA is normally implemented with full adders having three inputs, sum and carry outputs in each stage. Carry propagates diagonally through the array of adder cells as in Fig 3.

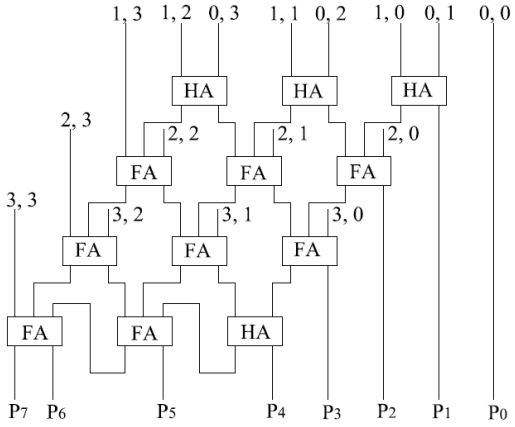

Fig 3 : Carry Save Adder

2.3 Carry Select Adder

The structure of carry select adder is as shown in Fig 4. This adder comes under the category of conditional sum adder. Sum and carry are calculated by assuming the input carry as 1 and 0, prior to the occurrence of the input carry. When the actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The conventional Carry Select Adder consists of k/2 bit adders for the lower half of the bits, and for the most significant bits 2k/2 bit adders are present. In most significant bit adders, one adder assumes carry input as 1 for performing addition, and another assumes carry input as 0. The carry out calculated from the last stage is used to select the actual calculated values of sum and carry. The selection is done using a multiplexer. Even though path delay is less than other adders, due to more power consumption power delay product is more than CLA adder.

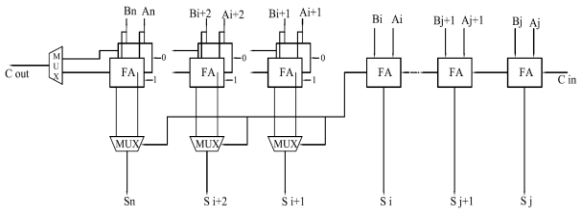

Fig 4 : Carry Select Adder

2.4 Carry Look Ahead Adder

The CLA adder, as shown in Fig 5(a), is one of the high speed adder used for the addition of two numbers. As in the figure, modified full adders are used for each bit position and the look-ahead modules produce group carry generate (G) and group carry propagate (P) outputs independently, which indicates that a carry is generated within the group or that an incoming carry would propagate across the group accordingly.

This adder has two logic blocks namely partially full adder (PFA) and Carry Look Ahead logic (CLA logic) . PFA does not involve carry propagation path while CLA logic has carry propagation path. In CLA logic OR gate and one of the AND gates from each of the full adders are removed to form the ripple carry path. There are two outputs P_i and G_i from each PFA to the ripple carry path, and one carry input C_i from the carry path to each PFA. The propagate function is given by $P_i = A_i$ XOR B_i, and whenever P_i is equal to 1, an incoming

carry is propagated through the bit position from C_i to C_{i+1}. For P_i equal to 0, carry propagation is blocked. The generate function is given by $G_i=A_i$ AND B_i, and whenever G_i is equal to 1, the carry output from the position is 1, regardless of the value of P_i. So, a carry has been generated in the position. When G_i is 0, carry is not generated, so that C_{i+1} is 0 if the carry propagated through the position from C_i is also 0. The P_i and G_i functions controls the values in the ripple carry path. Comparatively power consumption is less than all other three adders and power delay product is also less. Gate count is also reduced compared to other adders providing a reduction in area also.

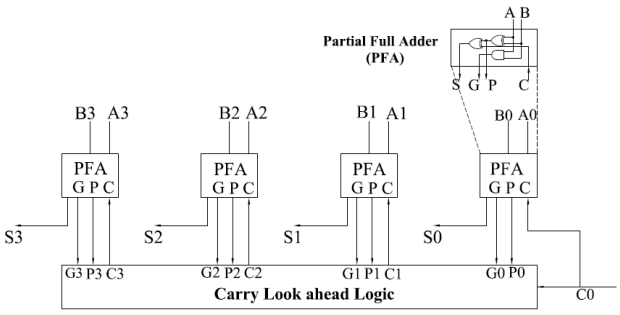

Fig 5(a) : Carry Look Ahead Adder

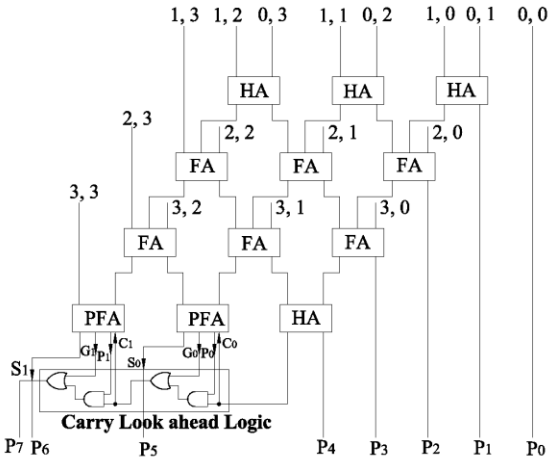

Fig 5(b) : Carry Look Ahead Adder in final adder stage of PP unit

3. SIMULATION RESULTS & DISCUSSIONS

The circuits are simulated using Xilinx ISE tool. Figure 6 to 9 shows the simulation result of the MAC unit with different types of adders. Table 1 and Chart 1 gives the average power, delay and area of MAC units with different adders. It can be noted that the average power consumption is lowest in MAC unit with CLA and highest in MAC unit with CSLA. But delay is reduced in MAC unit with CSLA compared to MAC unit with CLA. However power delay product is lowest in MAC unit with CLA and reduction in gate count also. MAC unit with CLA provides a reduction in power delay product of 6% compared to MAC unit with CSKPA, 2.4% compared to MAC unit with CSA, 0.06% compared to MAC unit with CSLA. MAC unit with CLA provides a reduction in area in terms of gate count of 9.2% compared to MAC unit with CSKPA, 16.7% compared to MAC unit with CSLA.

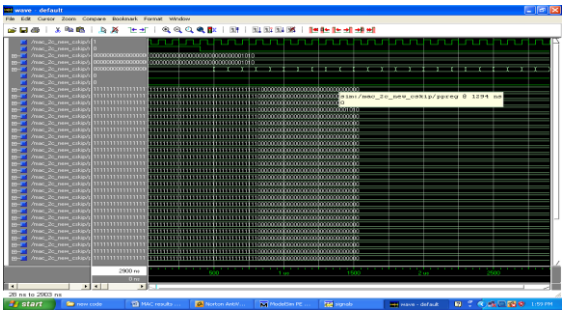

Fig 6 : Simulation result of MAC unit with CSKPA

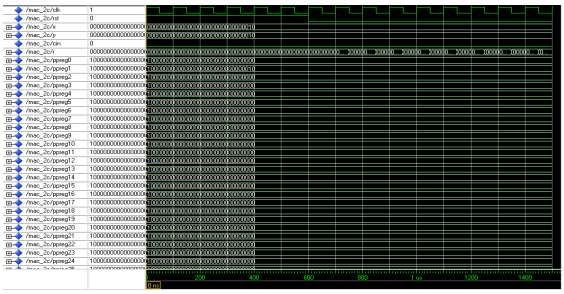

Fig 7 : Simulation result of MAC unit with CSA

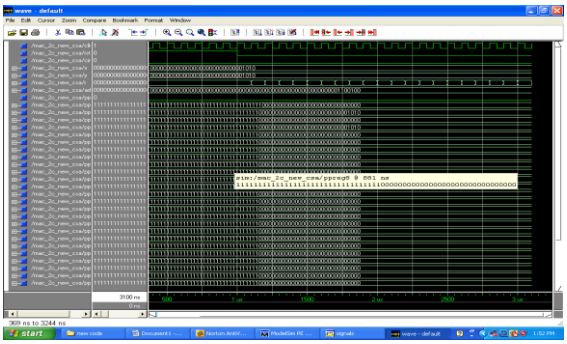

Fig 8 : Simulation result of MAC unit with CSLA

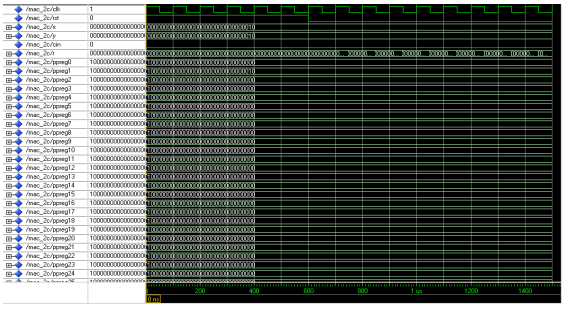

Fig 9 : Simulation result of MAC unit with CLA

Table 1 : Average Power, Combined path delay, Power-Delay product and gate count of MAC units with different adders

MAC design	Average Power (mW)	Combined path delay(nS)	Power-Delay product (nJ)	Total gate count
MAC with CSKPA	1203	160.19	192.7	46692
MAC with CSA	1182	157.13	185.7	50928
MAC with CSLA	1209	149.93	181.3	45957
MAC with CLA	1176	154.06	181.2	42410

Chart 1 : Average Power, Combined path delay, Power-Delay product and gate count of MAC units with different adders

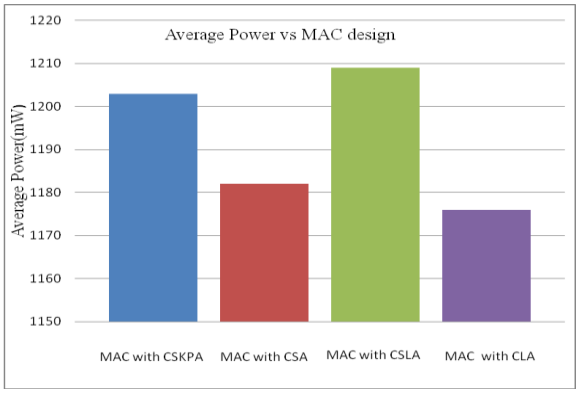

Chart 1a : Average Power vs MAC design

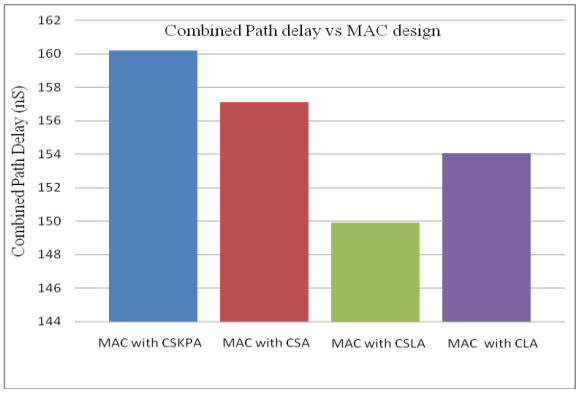

Chart 1b : Combined Path delay vs MAC design

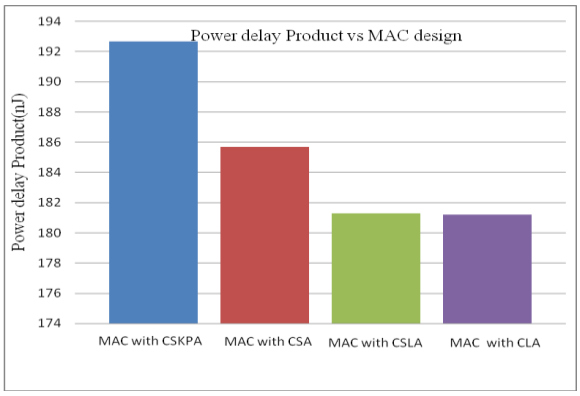

Chart 1c : Power delay Product vs MAC design

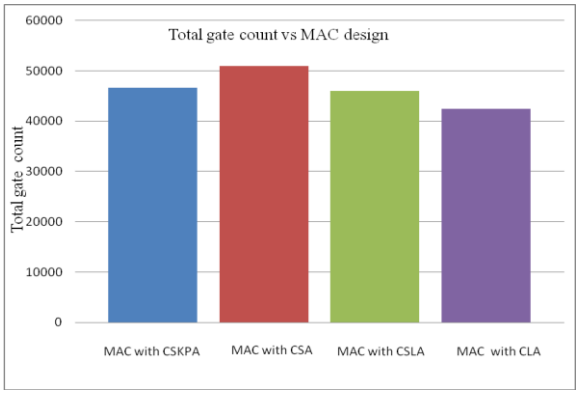

Chart 1d : Total gate count vs MAC design

4. CONCLUSION

In this paper, a design of a low power MAC structure is presented. The performance of the MAC unit with adders like carry skip, carry save, carry select and carry look ahead adder are compared. The overall power delay product and area of the MAC structure with CLA adder is found to be less than the MAC unit with the other three adders.

5. REFERENCES

[1] Tung Thanh Hoang, Magnus Själander, and Per Larsson-Edefors, "A High-Speed, Energy-Efficient Two-Cycle Multiply-Accumulate (MAC) Architecture and Its Application to a Double-Throughput MAC Unit," IEEE transactions on circuits and systems vol.57, no.12,pp. 3073 - 3081,2010.

[2] Wen-Chang Yeh and Chein-Wei Jen, "High-Speed Booth Encoded Parallel Multiplier Design," in IEEE transactions on computers vol.49, no.7,pp.692-701,2000.

[3] K A n h C. Bickerstaff, Michael Schulte and Earl E. Swartz,lander, Jr., "Reduced Area Multipliers," in International Conference on Application-Specific Array Processors, pp. 478-489.

[4] A. Abdelgawad and Magdy Bayoumi, "High Speed and Area-Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications," in IEEE, pp. 3199-3202, 2007.

[5] H.Murakami, et al. " A multiplier-accumulator macro for a 45 MIPS embedded RISC processor," IEEE J. Solid – State Circuits, vol. 31, pp. 1067-1071, July 1996.

[6] Mark R.Santoro And Mark A. Horowitz , "SPIM: A Pipelined 64 x 64-bit Iterative Multiplier," in IEEE journal of solid-state circuits, vol. 24, no. 2, pp.487-493, 1989.

[7] Vishwas M. Rao and Elehrouz Nowirouzian, "Design and Implementation of Asynchronous Parallel Multiply-Accumulate Arithmetic Architectures," in IEEE, pp. 761 - 764, 1996.

[8] Vojin *G.* Oklobdzija David Villeger, and Simon *S.* Liu "Method for Speed Optimized Partial Product Reduction and Generation of Fast Parallel Multipliers Using an Algorithmic Approach," IEEE transactions on computers, vol. 45, no. 3, pp.294-306, 1996.

[9] Ghassem Jaberipur and Amir Kaivan, "Improving the Speed of Parallel Decimal Multiplication," in IEEE transactions on computers, vol. 58, no. 11, pp. 1539-1552, 2009.

[10] Naofumi Takagi, Hiroto Yasuura And Shuzo Yajima, "High-Speed VLSI Multiplication Algorithm with a Redundant Binary Addition Tree," IEEE transactions on computers, vol. no. 9,pp.789-796 ,1985

[11] Kiamal Z. Pekmestzi, "Multiplexer-Based Array Multipliers," IEEE transactions on computers, vol. 48, no. 1, pp.15-23, Oct. 1999.

[12] Young-Ho Seo and Dong-Wook Kim, "A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm," IEEE transactions on very large scale integration (VLSI) systems, vol. 18, no. 2,pp 201 – 208, 2010

[13] Padma Devi, Ashima Girdher, Balwinder Singh "Improved Carry Select Adder with Reduced Area and Low Power Consumption," International Journal of Computer Applications Volume 3 – No.4, June 2010, pp.14 – 18, 2010.