

High-Speed 64-Bit Binary Comparator using Two Different Logic Styles

Anjuli (Student Member IEEE)
E&CE Department
FET-MITS (Deemed University)
Lakshmangarh, Sikar,
Rajasthan (India)

Satyajit Anand
E&CE Department
FET-MITS (Deemed University)
Lakshmangarh, Sikar,
Rajasthan (India)

ABSTRACT

High-speed 64-bit binary comparator using two different logic styles is proposed in this brief. Comparison is most basic arithmetic operation that determines if one number is greater than, equal to, or less than the other number. Comparator is most fundamental component that performs comparison operation. This brief presents comparison of modified and existing 64-bit binary comparator designs concentrating on delay. Means some modifications have been done in existing 64-bit binary comparator design to improve the speed of the circuit. Comparison between modified and existing 64-bit binary comparator designs is calculated by simulation that is performed at 90nm technology in Tanner EDA Tool.

Keywords:

Binary comparator, digital arithmetic, high-speed.

1. INTRODUCTION

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number [1]. So comparator is used for this purpose. Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes (Fig.1). The outcome of comparison is specified by three binary variables that indicate whether $A > B$, $A = B$, or $A < B$. The circuit, for comparing two n-bit numbers, has 2n inputs & 2^{2n} entries in the truth table. For 2-bit numbers, 4-inputs & 16-rows in the truth table, similarly, for 3-bit numbers 6-inputs & 64-rows in the truth table [1].



Fig 1: Block Diagram of n-Bit Magnitude Comparator

In recent year, high speed & low power device designs have emerged as principal theme in electronic industry due to increasing demand of portable devices. This tremendous demand is due to popularity of battery operated portable equipments such as personal computing devices, wireless communication, medical applications etc. Demand & popularity of portable electronic devices are driving the designers to strive for higher speed, smaller power consumption and smaller area.

The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit [2]. Circuit size depends on the number of transistors and their sizes and on the wiring complexity [3]. The wiring complexity is

determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance [4].

In order to differentiate both the designs existing and modified, simulations are carried out for delay and power consumption with 1 volt input voltage (and supply voltage), 30°C temperature and 50MHz frequency at 90nm technology in Tanner EDA Tool.

2. 64-BIT BINARY COMPARATOR

64-bit binary comparator compares two numbers each having 64 bits (A_{63} to A_0 & B_{63} to B_0). For this arrangement truth table has 128 inputs & 2^{128} entries. By using comparator of minimum number of bits, a comparator of maximum number of bits can be design [5], [6], [7] with the help of tree-based structure logic [8] and also with other useful logic styles.

3. EXISTING 64-BIT BINARY COMPARATOR DESIGN

64-bit comparator in reference [8], [9], [10] represents tree-based structure which is inspired by fact that G (generate) and P (propagate) signal can be defined for binary comparisons, similar to G (generate) and P (propagate) signals for binary additions.

Two number (each having 2-bits: A_1, A_0 & B_1, B_0) comparison can be realized by:

$$B_{Big} = \overline{A_1} B_1 + (\overline{A_1 \oplus B_1}) \cdot (\overline{A_0} B_0) \quad (1)$$

$$EQ = (\overline{A_1 \oplus B_1}) \cdot (\overline{A_0 \oplus B_0}) \quad (2)$$

For $A < B$, “ B_{Big} , EQ” is “1,0”. For $A = B$, “ B_{Big} , EQ” is “0,1”. Hence, for $A > B$, “ B_{Big} , EQ” is “0,0”. Where B_{Big} is defined as output A less than B (A_LT_B). A closer look at equation (1) reveals that it is analogous to the carry signal generated in binary additions. Consider the following carry generation:

$$C_{out} = AB + (A \oplus B) \cdot C_{in} \\ = G + P \cdot C_{in} \quad (3)$$

Where A & B are binary inputs C_{in} is carry input, C_{out} is carry output, and G & P are generate & propagate signals, respectively.

After comparing equations (1) & (3):

$$G_1 = \overline{A_1} B_1 \quad (4)$$

$$EQ_1 = (\overline{A_1 \oplus B_1}) \quad (5)$$

$$C_{in} = \overline{A_0} B_0 \quad (6)$$

C_{in} can be considered as G_0 . Since for static logic, equation (1) requires tall transistor stack height, hence, an encoding scheme is employed to solve this problem. For this, encoding equation is given as:

$$G_{[i]} = \overline{A_{[i]}} B_{[i]} \quad (7)$$

$$EQ_{[i]} = (A_{[i]} \oplus B_{[i]}) \quad (8)$$

Where $i = 0 \dots \dots \dots 63$.

Put these two values from equations (7) & (8) in equations (1) & (2).

$$B_{Big [2j+1: 2j]} = G_{[2j+1]} + EQ_{[2j+1]} \cdot G_{[2j]} \quad (9)$$

$$EQ_{[2j+1: 2j]} = EQ_{[2j+1]} \cdot EQ_{[2j]} \quad (10)$$

Where $j = 0 \dots \dots \dots 31$.

G & P signals can be further combined to form group G & P signals.

$$B_{Big [3:0]} = \overline{A_3} B_3 + (\overline{A_3 \oplus B_3}) \cdot (\overline{A_2} B_2) + (\overline{A_3 \oplus B_3}) \cdot (\overline{A_2 \oplus B_2}) \cdot (\overline{A_1} B_1) + (\overline{A_3 \oplus B_3}) \cdot (\overline{A_2 \oplus B_2}) \cdot (\overline{A_1 \oplus B_1}) \cdot (\overline{A_0} B_0)$$

$$B_{Big [3:0]} = \overline{A_3} B_3 + (\overline{A_3 \oplus B_3}) \cdot [\overline{A_2} B_2 + (\overline{A_2 \oplus B_2}) \cdot \{ \overline{A_1} B_1 + (\overline{A_1 \oplus B_1}) \cdot (\overline{A_0} B_0) \}]$$

$$B_{Big [3:0]} = G_3 + EQ_3 \cdot \{ G_2 + EQ_2 \cdot (G_1 + EQ_1 \cdot G_0) \}$$

$$B_{Big [3:0]} = B_{Big [3:2]} + EQ_{[3:2]} \cdot B_{Big [1:0]} \quad (11)$$

$$EQ_{[3:0]} = EQ_{[3:2]} \cdot EQ_{[1:0]} \quad (12)$$

Similarly, for 64-bit comparator, B_{Big} & EQ can be computed as:

$$B_{Big [63:0]} = G_{63} + \sum_{k=0}^{62} \left(G_k \cdot \prod_{m=k+1}^{63} EQ_m \right) \quad (13)$$

$$EQ_{[63:0]} = \prod_{m=0}^{63} EQ_m \quad (14)$$

Fig. 2 shows 8-bit version of existing tree-based comparator structure and Fig. 3 -Fig. 5 shows corresponding circuit schematics for each logic block of each stage. Pre-encoding circuitry is aimed to minimize the number of transistors. Hence, modified pass transistor logic style is employed to reduce the number of transistors up to 9. In above 8-bit example circuitry, the first stage comparison circuit implements equations (9 & 10) for $j = 0 \dots 3$, whereas the second stage generates $B_{Big[3:0]}$, $B_{Big[7:4]}$ and $EQ_{[3:0]}$, $EQ_{[7:4]}$ according to equations (11 & 12). Finally, $B_{Big[7:0]}$ and $EQ_{[7:0]}$ are computed in third stage according to equations (13 & 14).

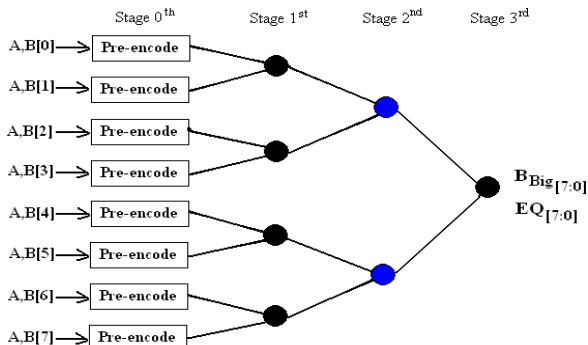


Fig 2: Tree-Diagram of 8-Bit Binary Comparator

Stage 0th is implemented using modified pass transistor logic style giving output in actual form, Stage 1st is implemented using CMOS logic style giving output in inverse form, Stage 2nd is also implemented using CMOS logic style but giving output in actual form.

64-bit comparator is here designed by using 7 stages (from 0th to 6th). In stage 0th, modified pass transistor logic style circuitry (as in Fig. 3) is employed to produce “less than” & “equal to” outputs. Outputs of stage 0th act as inputs of stage 1st. In stage 1st, CMOS circuitry (as in Fig. 4) is employed to produce inverse inputs for stage 2nd. In stage 2nd, again CMOS circuitry (as in Fig. 5) is employed to produce actual inputs for stage 3rd. Now, according to tree structure given in Fig. 2, again circuitry of stage 1st is used for stage 3rd. Similarly, for stage 4th, circuitry of stage 2nd is employed. For stage 5th circuitry of stage 1st is employed. For stage 6th circuitry of stage 2nd is employed. Description of this design is given in tabular form in Table 1.

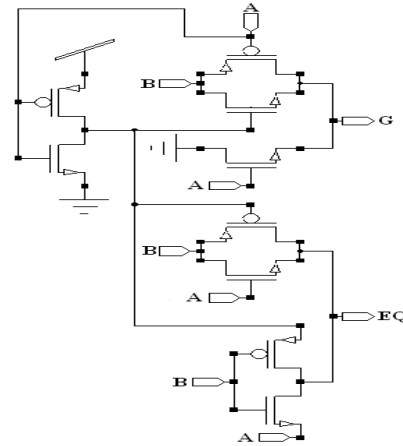


Fig 3: Schematic of Stage 0th of Existing 64-Bit Binary Comparator

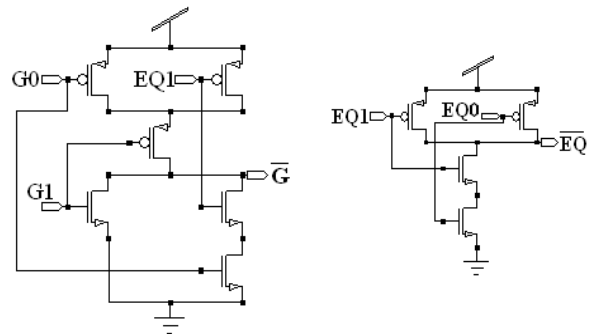


Fig 4: Schematic of Stage 1st of Existing 64-Bit Binary Comparator

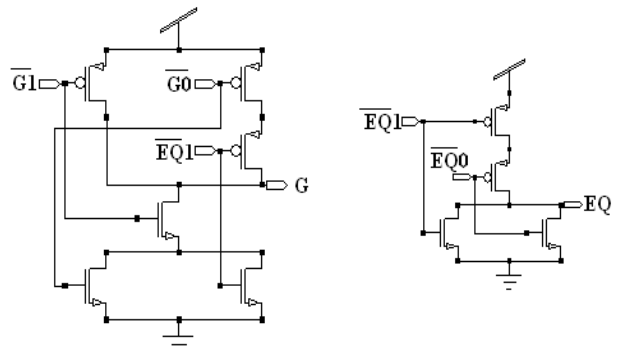


Fig 5: Schematic of Stage 2nd of Existing 64-Bit Binary Comparator

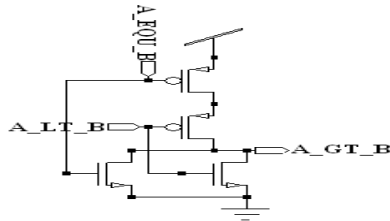


Fig 6: Schematic of NOR gate

According to [8] existing design is having two outputs (“A less than B” & “A equal to B”). This research work also represents here two outputs but they are “A less than B” and “A greater than B”. Means “A greater than B” output is here calculated in place of “A equal to B” output. For this arrangement, an extra circuitry of NOR gate (which is shown in Fig. 6) is included at the end of schematic of existing 64-bit binary comparator design. Outputs of “A less than B” & “A equal to B” are given to two inputs of NOR gate that produces “A greater than B” output. Existing design requires 1210 transistor count for 64-bit binary comparator. Accordingly schematic of Existing 64-bit binary comparator is drawn and shown in Fig. 7.

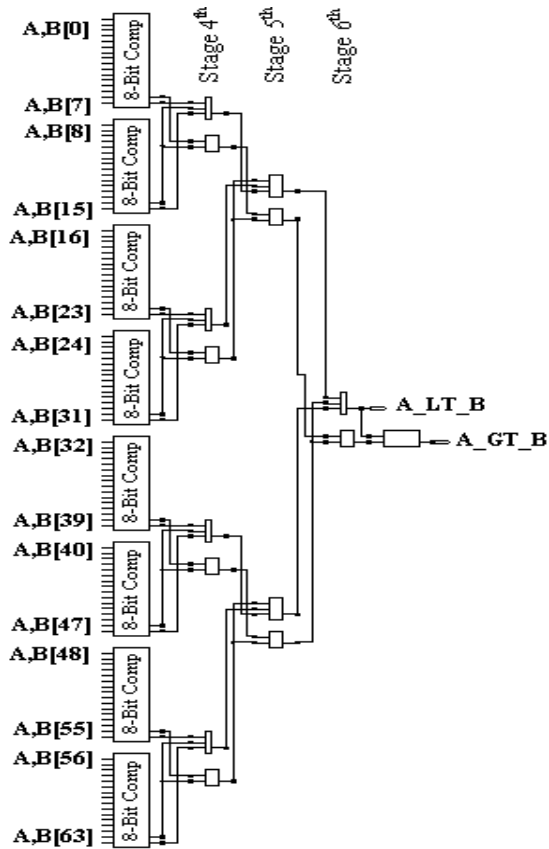


Fig 7: Schematic of Existing 64-Bit Binary Comparator

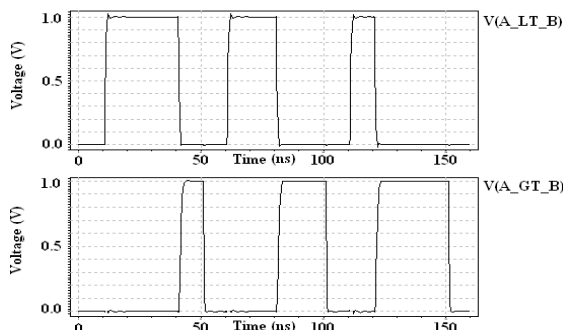


Fig 8: Waveforms of Existing 64-Bit Binary Comparator

According to input bit stream, waveforms of existing 64-bit binary comparator are obtained and shown in Fig. 8. Waveforms show that only one output is high (“1”) at a time. When both the outputs “less than” & “greater than” (A_LT_B & A_GT_B) are low (“0”), then waveforms represent that “equal to” output is high (A_EQU_B is “1”) at that time. Simulation results for this design are given in Table I4– Table 6 for conclusion.

4. MODIFIED 64-BIT BINARY COMPARATOR DESIGN

Some modifications have been done in existing 64-bit binary comparator design [8] to improve the speed of the circuit. Existing 64-bit binary comparator design [8] follows tree-based structure from 2-bit to 64-bit circuitry. But modified design follows tree-based structure from 2-bit to 8-bit circuitry only. After 8-bit to 64-bit circuitry, modified design follow simple logic structure having two stages (Stage A and Stage B) in place of tree-based structure. In modified design, both the outputs of eight (from 0th to 7th) 8-bit comparators of stage A are given to 8th 8-bit comparator of stage B to produce final outputs (“less than” and “greater than”). A less than B outputs of 0th to 7th 8-bit comparators are given to A_{0:7} inputs of 8th 8-bit comparator. A equal to B outputs of 0th to 7th 8-bit comparators are given to B_{0:7} inputs of 8th 8-bit comparator that produces final outputs.

For this design, In stage A, all three basic stages (0th, 1st, 2nd) have been implemented using CMOS logic style. Means stage 0th of modified 64-bit comparator design have been implemented using CMOS logic style (as in Fig. 9) that was implemented using modified PTL style in existing design. Remaining two stages (1st & 2nd) are exactly same as existing 64-bit comparator design Fig. 4 and Fig. 5. Description of this design is given in tabular form in Table 2.

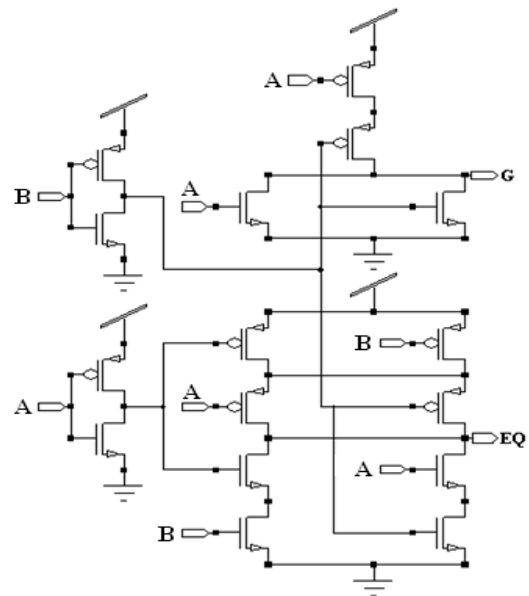


Fig 9: Schematic of Stage 0th of Stage A of Modified 64-Bit Binary Comparator

In stage B, basic stage 0th is same as existing 64-bit comparator design & implemented using modified pass transistor logic style (Fig. 3) giving output in actual manner. Stage 1st is also implemented using modified pass transistor logic style (MPTL) giving output in actual manner as in Fig. 10. Stage 2nd is same as stage 1st of existing 64-bit comparator design & implemented using CMOS logic style but giving output in inverse manner as in Fig. 11. Description of this design is given in tabular form in Table 3.

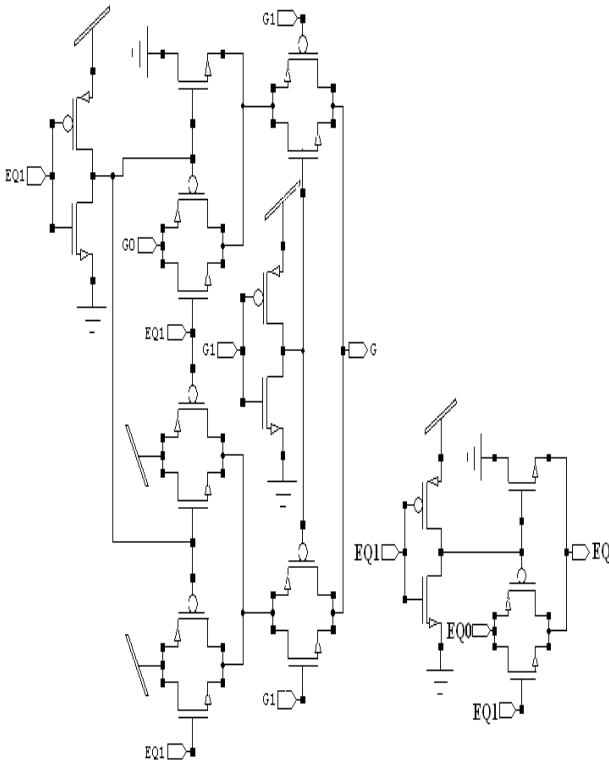


Fig 10: Schematic of Stage 1st of Stage B of Modified 64-Bit Binary Comparator

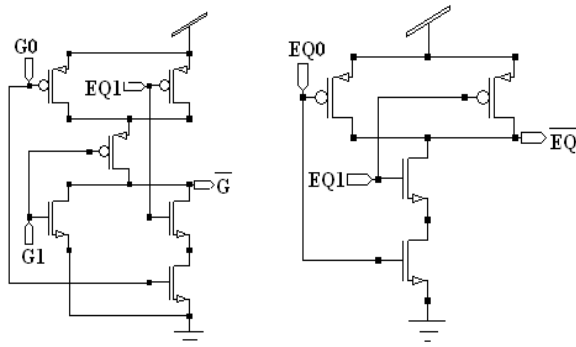


Fig 11: Schematic of Stage 2nd of Stage B of Modified 64-Bit Binary Comparator

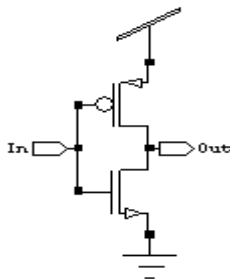


Fig 12: Schematic of Inverter of Modified 64-Bit Binary Comparator

Since output of 8-bit comparators are obtained in inverse form. So, at the end of schematic design of modified 64-bit comparator two inverters (Fig. 12) are required to produce actual form of output waveform. This design requires 1780 transistor count for 64-bit comparator. Schematic (using instances of each section) of modified 64-bit binary comparator design is drawn and shown in Fig. 13.

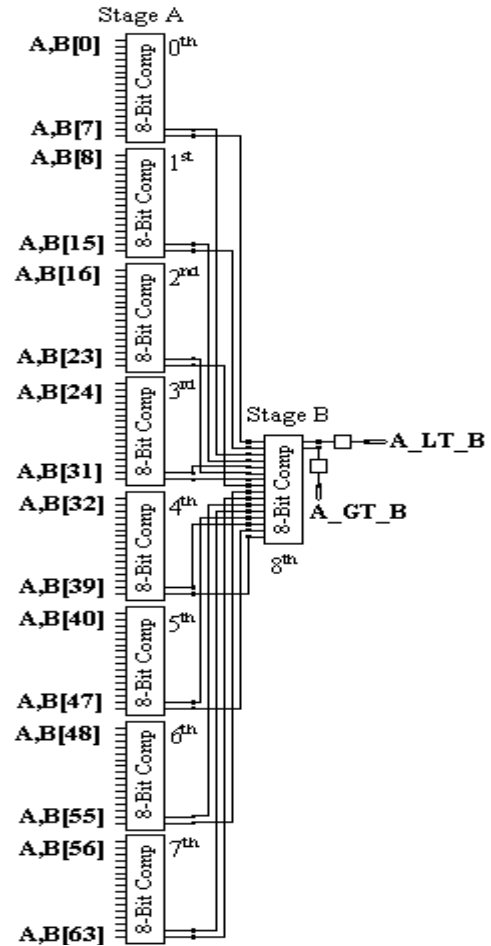


Fig 13: Schematic of Modified 64-Bit Binary Comparator

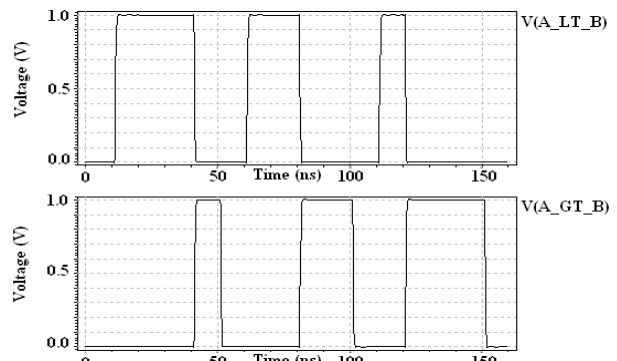


Fig 14: Waveforms of Modified 64-Bit Binary Comparator

According to input bit stream, waveforms of modified 64-bit binary comparator are obtained and shown in Fig. 14. Input bit stream for modified design is same as in existing design of 64-bit comparator. Output waveforms of modified design produce same position of 1,s and 0,s as in waveforms of existing design for each input bits. Waveforms show that only one output is high ("1") at a time. When both the outputs "less than" & "greater than" (A_LT_B & A_GT_B) are low ("0"), then waveforms represent that "equal to" output is high (A_EQU_B is "1") at that time. Simulation results for modified 64-bit binary comparator design are given in tabular form in Table 4 –Table 6.

5. SIMULATION AND COMPARISON

After simulation of both the designs final results are obtained for delay and power consumption and are shown in Table 4 – Table 6. Simulations have been carried out at 90nm technology in Tanner EDA Tool.

Table 1. Description of Existing 64-Bit Binary Comparator design

| Detail | Stage 0 th | Stage 1 st | Stage 2 nd | Transistor Count |
|------------------|-----------------------|-----------------------|-----------------------|------------------|
| Design | Using MPTL Style | Using CMOS Style | Using CMOS Style | 1210 |
| Nature of output | Actual | Inverse | Actual | |

Table 2. Description of Stage A of Modified 64-Bit Binary Comparator Design

| Detail | Stage 0 th | Stage 1 st | Stage 2 nd | Transistor Count |
|------------------|-----------------------|-----------------------|-----------------------|------------------|
| Design | Using CMOS Style | Same as Existing | Same as Existing | 1584 |
| Nature of output | Actual | Inverse | Actual | |

Table 3. Description of Stage B of Modified 64-Bit Binary Comparator Design

| Detail | Stage 0 th | Stage 1 st | Stage 2 nd | Transistor Count |
|------------------|-----------------------|-----------------------|---|------------------|
| Design | Same as Existing | Using MPTL Style | Same as Stage 1 st of Existing | 196 |
| Nature of output | Actual | Actual | Inverse | |

Table 4. Simulation Data with 1volt Input Voltage

| Design | Power Consumption (watt) | Delay Time (second) | |
|----------|--------------------------|---------------------|----------------|
| | | $t_{A_LT_B}$ | $t_{A_GT_B}$ |
| Existing | 9.0675e-6 | 4.4240e-9 | 1.6028e-8 |
| Modified | 2.1636e-5 | 4.2439e-9 | 1.5763e-8 |

Table 5. Simulation Data with 30°C Temperature

| Design | Power Consumption (watt) | Delay Time (second) | |
|----------|--------------------------|---------------------|----------------|
| | | $t_{A_LT_B}$ | $t_{A_GT_B}$ |
| Existing | 9.2485e-6 | 4.4187e-9 | 1.6033e-8 |
| Modified | 2.1875e-5 | 4.2410e-9 | 1.5769e-8 |

Table 6. Simulation Data with 50MHz Frequency

| Design | Power Consumption (watt) | Delay Time (second) | |
|----------|--------------------------|---------------------|----------------|
| | | $t_{A_LT_B}$ | $t_{A_GT_B}$ |
| Existing | 9.2765e-6 | 4.4240e-9 | 1.6020e-8 |
| Modified | 2.1484e-5 | 4.2439e-9 | 1.5763e-8 |

After simulation of both the designs final results are obtained for delay and power consumption with 1 volt input voltage. Delay comparison of modified and existing 64-bit comparator designs is shown in Fig. 15 & Fig. 16. Simulated data for these graphs is given in Table 4.

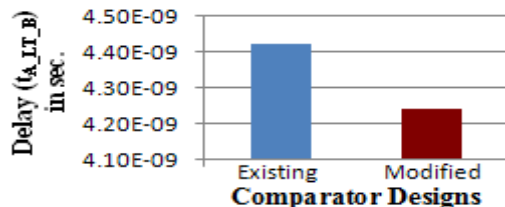


Fig 15: Delay ($t_{A_LT_B}$) vs Comparator Designs

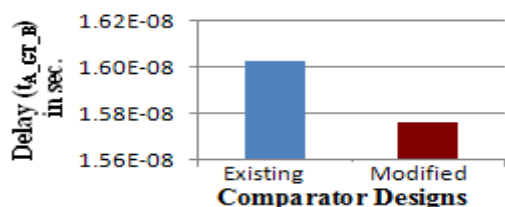


Fig 16: Delay ($t_{A_GT_B}$) vs Comparator Designs

The graphs shown in Fig. 15 & Fig. 16 reveal that delay of modified 64-bit comparator design at 1 volt input voltage is remarkably reduced than existing 64-bit comparator design. In Fig. 15, delay is reduced 4.1%. In Fig. 16, delay is reduced 1.7%.

After simulation of both the designs final results are obtained for delay and power consumption with 30°C temperature. Simulation with temperature has been done at 1 volt input voltage. Delay comparison of modified and existing 64-bit comparator designs is shown in Fig. 17 & Fig. 18. Simulated data for these graphs is given in Table 5.

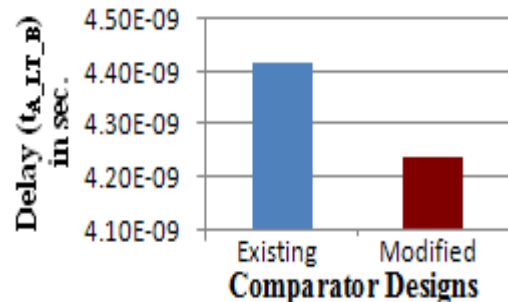


Fig 17: Delay ($t_{A_LT_B}$) vs Comparator Designs

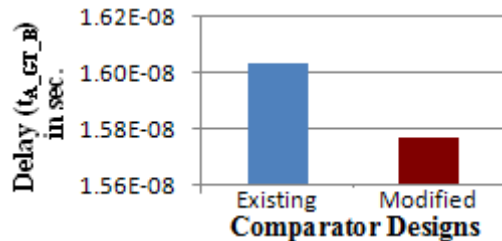


Fig 18: Delay ($t_{A_GT_B}$) vs Comparator Designs

The graphs shown in Fig. 17 & Fig. 18 reveal that delay of modified 64-bit comparator design at 30°C temperature is remarkably reduced than existing 64-bit comparator design. In Fig. 17, delay is reduced 4.0%. In Fig.18, delay is reduced 1.6%.

After simulation of both the designs final results are obtained for delay and power consumption with 50MHz frequency. Simulation with frequency has been done at 1 volt input voltage. Delay comparison of modified and existing 64-bit comparator designs is shown in Fig. 19 & Fig. 20. Simulated data for these graphs is given in Table 6.

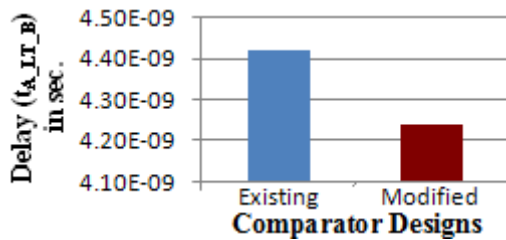


Fig 19: Delay ($t_{A_LT_B}$) vs Comparator Designs

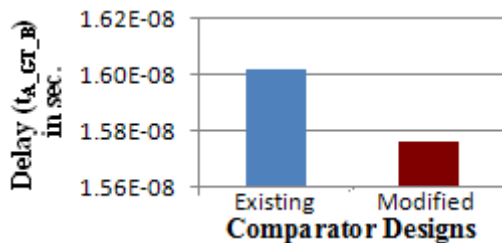


Fig 20: Delay ($t_{A_GT_B}$) vs Comparator Designs

The graphs shown in Fig. 19 & Fig. 20 reveal that delay of modified 64-bit comparator design at 50MHz frequency is remarkably reduced than existing 64-bit comparator design. In Fig. 19, delay is reduced 4.1%. In Fig.20, delay is reduced 1.6%.

6. CONCLUSION

In modified design, at 1 volt input voltage delay for output “A less than B” ($t_{A_LT_B}$) is reduced 4.1 % and delay for output “A greater than B” ($t_{A_GT_B}$) is reduced 1.7 % in comparison to existing design. Similarly, at 30°C temperature delay for output “A less than B” ($t_{A_LT_B}$) is reduced 4.0 % and delay for output “A greater than B” ($t_{A_GT_B}$) is reduced 1.6 %. And also at

50MHz frequency delay for output “A less than B” ($t_{A_LT_B}$) is reduced 4.1 % and delay for output “A greater than B” ($t_{A_GT_B}$) is reduced 1.6 % in comparison to existing design. Hence, superiority of modified design is maintained for temperature and frequency also. All of the reduction in delay is obtained after sacrificing power consumption and transistor count. But still modified design gives better result (for delay) than existing design. Therefore, modified 64-bit binary comparator design can be better option for high-speed applications.

7. REFERENCES

- [1] M. Morris Mano “Digital Design” (Pearson Education Asia, 3rd Ed, 2002).
- [2] R. Zimmermann and W. Fichtner, “Low Power Logic Styles: CMOS Versus Pass Transistor Logic” IEEE Journal of Solid State Circuits, Vol.32, No.7,pp1079-1090,July 1997.
- [3] S. Kang and Y. Leblebici “CMOS Digital Integrated Circuit, Analysis and Design” (Tata McGraw-Hill, 3rd Ed, 2003).
- [4] A. Bellaouar and Mohamed I. Elmasry, “Low Power Digital VLSI Design: Circuits and Systems” (Kluwer Academic Publishers, 2nd Ed, 1995).
- [5] C.-H. Huang and J.-S. Wang, “High-performance and power-efficient CMOS comparators,” IEEE J. Solid-State Circuits, vol. 38, no.2, pp. 254–262, Feb. 2003.
- [6] H.-M. Lam and C.-Y. Tsui, “High-performance single clock cycle CMOS comparator,” Electron. Lett., vol. 42, no. 2, pp. 75–77, Jan. 2006.
- [7] H.-M. Lam and C.-Y. Tsui, “A MUX-based high-performance single cycle CMOS comparator,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 7, pp.591-595 July 2007.
- [8] Pierce Chuang, David Li, and Manoj Sachdev, Fellow, IEEE “A Low-Power High-Performance Single-Cycle Tree-Based 64-Bit Binary Comparator” IEEE Transactions on Circuits And Systems—II: Express Briefs, Vol. 59, No. 2, February 2012.
- [9] F. Frustaci, S. Perri, M. Lanuzza, and P. Corsonello, “A new low-power high - speed single – clock -cycle binary comparator,” in Proc. IEEE Int. Symp. Circuits Syst., pp. 317–320, 2010.
- [10] S. Perri and P. Corsonello, “Fast low-cost implementation of single-clock-cycle binary comparator,”IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 12, pp. 1239–1243, Dec. 2008.