Wide Tuning Range CMOS VCO for Radio Frequency Application

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ABSTRACT

This paper presents a three-stage 1.8V ring VCO in a 0.18 μm CMOS technology with wide tuning range and a good phase noise differential ring oscillator . The oscillator architecture is a three stage differential ring with Multi pass path using push-pull inverters. The circuit was implemented and the measured tuning range of the from 3.8741 GHz to 5.913 GHz, phase noise is -106dBc/Hz from center frequency 5.9GHz and Power Dissipation 28.392dBm at Control Voltage 1Volt.

Keywords

CMOS, low power, phase noise, tail current, voltage controlled oscillator (VCO)

1. INTRODUCTION

Voltage controlled oscillators (VCOs) are essential components of RF circuit used in transmitters and receivers as sources of carrier waves with variable frequencies. As wireless communication systems move towards high data-rate applications high frequency and low-phase-noise oscillators become important building blocks in the frequency synthesizer design. The most important parameters of the oscillator are the phase noise, the voltage supply, the power consumption and the tuning range. Unlike an LC-VCO, this type of VCO requires no on chip inductors, which contributes to its relatively small chip area.The ring oscillator frequency is controlled by the cascade differential inverter time delay, which in turn is governed by the charge / discharge rate of the capacitors loading each differential inverter. Voltage-controlled oscillators (VCOs) are critical building blocks in phase-locked loops (PLLs) and they are widely used in communications systems. We have developed a ring VCO with improved supply noise and common-mode noise rejection, and its phase noise is comparable to that of LC oscillators with on-chip spiral inductors. A CMOS voltage-controlled-oscillator (VCO) is conventionally built using the ring. Architectures or an LC resonant circuit, Among these, the LC design has better phase-noise and frequency performance owing to the large quality factor Q achievable with resonant networks. However, adding high quality integrated inductors to a CMOS process flow increase the cost and complexity of the chip, and also introduces problems such as the control of eddy currents in the substrate [1]. Ring oscillators can be built in any standard CMOS process and may require less die area than LC designs. The design is straightforward, and ring architectures can be used to provide multiple output phases and wide tuning rang [2]. And on-chip spiral inductors occupy a lot of chip area. The on-chip spiral inductor usually occupies a large chip area, which is undesirable for cost and yield considerations [4]. The phase noise performance of ring oscillator is the worst, comparing to LC-oscillators. The Basic differential CMOS three stage Multi pass ring oscillator.

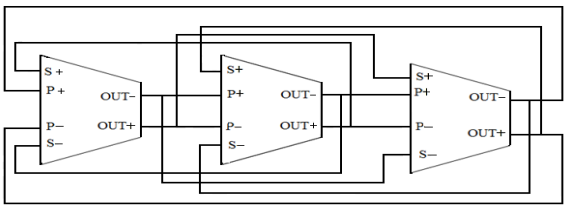

Figure 1: Basic differential CMOS three stage Multi pass ring oscillator.

The delay cell circuits are differential in nature because of the improvements in noise and common mode suppression.The differential multi pass ring oscillator can be created by cascading *N* differential inverters with the outputs tied to input complements and the feedback connection going to the corresponding input as shown in Figure 1. The tail current is used control fine tuning in figure 2. The voltage-controlled oscillator (VCO) used in delay stages with symmetric loads and These stages have supply noise rejection operating over a

broad delay range with low supply voltage requirements that scale with the operating delay[5].

2. PROPOSED DIFFERENTIAL DELAY CELL

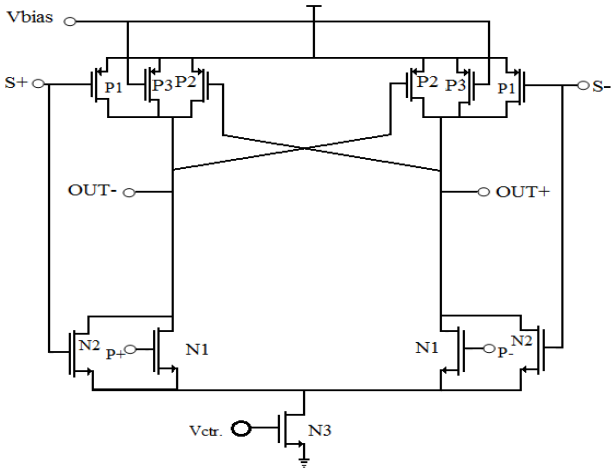

Figure 2 : Differential CMOS delay cell.

The Delay cell consists of cross coupled PMOS. The cross-couple PMOS provide Positive feed- back and coupling so frequency is decrease but it good for Phase noise. The cross coupled NMOS is not use because of NMOS higher noise than the PMOS [6] and PMOS have better in static power dissipation. Without use of Cross–coupled PMOS latch differential delay cell of output nodes forms converging at same voltage so differential oscillation may be end up becoming single–ended ring oscillators. The cross coupled PMOS latch provide a negative resistance [7] which cancellation resistance due to channel-length modulation which are provide an equivalent negative resistance to cancel out the resitive load due to G_{ds} [8]. G_{ds} is the resistive load due to channel-length modulation and it is equal to $G_{P1}+G_{P2}+G_{N2}+g_{N1}+g_{N2}$ where

$G_{P1},G_{P2},G_{N2},g_{N1},g_{N2}$ are resistive load due to P1,P2.N1,N2. Science P3 are work in deep triode region so we are not considering secondry effect.the tail current controle transitor N3 is not consider for aproximation.

2.1 SMALL-SIGNAL MODEL OF MULTI PASS RING OSCILLATOR

The small signal model we assume that oscillation is sinusoidal and amplitude is small. G_n ,G_p and g_n represent the transconduction secondary input to output and primary input to output of transisterN2, P1 and N1 . g_{pc} is transconduction of cross-coupled pair P2. R is the equivalent resistance of load and C is the output capacitance at the output node of differential delay. We assume that θ is phase difference between output node and primary input and ϕ is the phase difference between output node and secondry input node.

$$V_{out-} = V_{p+}e^{-j\theta} \quad (1)$$

$$V_{out-} = V_{s+}e^{-j\phi} \quad (2)$$

$$V_{out-} = V_{out+}e^{-j\pi} \quad (3)$$

Use KCL at the output node, OUT-

$$V_{out-} = \frac{R}{1+j\omega RC}\left[-g_n V_{p+} - \left(G_n + G_p\right)V_{s+} - g_{pc} V_{out+}\right] \quad (4)$$

Substituting equations (2) and (3) into equation (4) and rearranging V_{out-} and V_{P+}

$$V_{out-} = \frac{R}{1+j\omega RC}\left[-g_n V_{p+} - \left(G_n + G_p\right)V_{out-}e^{j\phi} - g_{pc} V_{out-}e^{j\pi}\right]$$

Therefore the transfer function $H(j\omega)$ can be written as

$$H(j\omega) = \frac{V_{out-}}{V_{p+}}$$

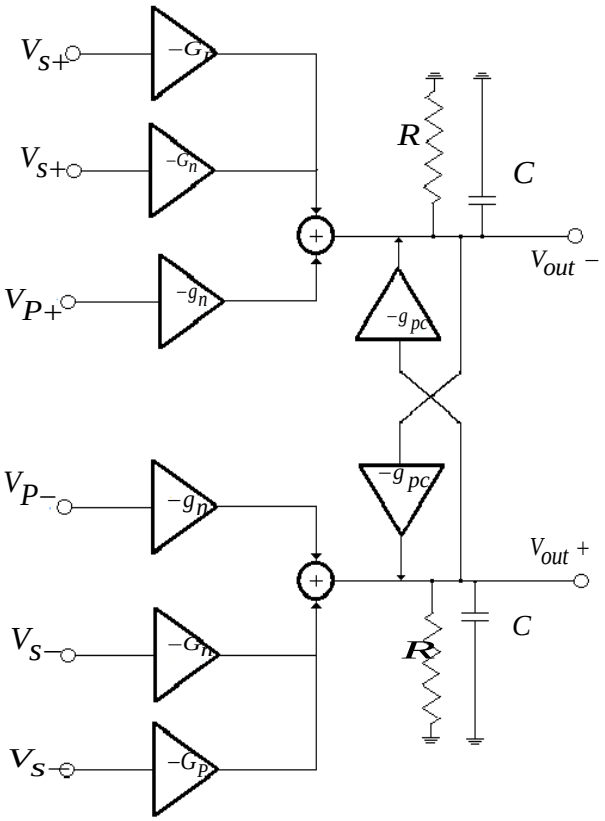

Figure 3: Small signal model of Differential CMOS delay cell.

$$H(j\omega) = \frac{\left[-g_n R\right]}{\left[\begin{array}{l} 1 + R\left(G_n + G_p\right)\cos\phi - g_{pc} R + \\ j\left\{\omega RC + R\left(G_n + G_p\right)\sin\phi\right\} \end{array}\right]} \quad (5)$$

From transfer function $H(j\omega)$ the following a relationship can be obtained from equation (5).

$$-\tan^{-1}\frac{\omega RC + R\left(G_n + G_p\right)\sin\phi}{1 + R\left(G_n + G_p\right)\cos\phi - g_{pc} R} = -\theta \pm \pi \quad (6)$$

Taking tangent both side and rearranging equation (6), the frequency factor can be written as:

$$\tan\theta = \frac{\omega RC + R\left(G_n + G_p\right)\sin\phi}{1 + R\left(G_n + G_p\right)\cos\phi - g_{pc} R}$$

$$\omega = \left[\frac{\tan\theta}{RC} + \frac{\left(G_n + G_p\right)\left(\tan\theta\cos\phi - \sin\phi\right)}{C} - \frac{g_{pc}\tan\theta}{C}\right] \quad (7)$$

From equation (7), it is seen that R, ϕ and G_n, G_p will affect the tuning range of the oscillator. Since θ is defined by the number of delay cells in the ring oscillator and C is equivalent parasitic capacitance of the circuit, both of these cannot be changed by tuning the control signals. The second term in the equation presents the effect of the oscillation frequency that is due to the secondary loop. In order to improve the oscillation frequency the term, $\tan\theta\cos\phi - \sin\phi$, has to be positive. $\tan\theta$ is always a positive value because $\pi < \theta \le \frac{3\pi}{2}$. Thus, the secondary loop has to be properly connected to ensure that above term is positive. On the other hand greater value of G_n, G_p will results greater frequency improvement but it cannot improve moor because this improvement is nonlinear since the larger secondary input transistor leads to extra capacitance at the output node. The third term in equation due to cross- coupled PMOS pair. We can see that it decreases the frequency which is proportional to the transistor transconductance. Hence decrease the transistor size will reduce the frequency decreasing.

From equation (5) and (7) and according to the Barkhausen criterion of oscillation, the minimum DC gain required of each gain stage can be written as

$$\left|-g_n R\right| \ge \sqrt{\left\{1 + R\left(G_n + G_p\right)\cos\phi - g_{pc} R\right\}^2 + \left\{\omega RC + R\left(G_n + G_p\right)\sin\phi\right\}^2}$$

$$\left| -g_n R \right| \geq \left| \frac{1 + R\left(G_n + G_p\right)\cos\phi - g_{pc} R}{cas\theta} \right| \quad (8)$$

The equation (8) is conceder for the minimum requirement in design process for meet oscillation. The size of the cross-coupled PMOS is design to be sufficiently small as compare to the other transistors in the delay cell, so as to ensure minimum influence on the loop frequency as well as noise contribution that is low enough to be ignored. The transconductance g_m [7] is defined by

$$g_m = \mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_{TH}\right)$$

Hence transconductance g_m is directly proportional to width (W) by very the width (W) getting good result of frequency and phase noise.

2.2 WIDE TUNING

From equation (7)

$$\omega = \left[\frac{\tan\theta}{RC} + \frac{\left(G_n + G_p\right)K_0}{C} - \frac{g_{pc}\tan\theta}{C} \right] \quad (9)$$

where

$$K_0 = \left(\tan\theta\cos\phi - \sin\phi\right)$$

we are more interested in comparing the relative frequency improvement between different topologies rather than be used to qualitatively estimate the relative frequency increase/decrease $\Delta\omega$ compared to the conventionalring topology. We have

$$\frac{\Delta\omega}{\omega_C} = \left(\frac{C_c}{C} - 1\right) + \frac{\left(G_n + G_p\right) R C_c K_0}{C \tan\theta} - \frac{g_{pc} C_c}{C} \quad (10)$$

Where C_C is output load capacitance for conventional ring oscillator.We have assumed that R remains the same.

To increase the frequency of voltage controle oscillator we observe from equation (9) that frequency is very according to three parameters loading registance, loading capacitance and transconduction strength.Capacitive tuning have draback it decreases the speed of operation because it still load the circuit even its minimum value.The resistive tuning can provide a large variation and it cause voltage gain and voltage swing variation[9] when transistors operating in the triode region .it work as load registor . From equation (7) osillation frequency of subfeedback path ring oscillator depend on lenear G_n, G_p . When G_n, G_p are controlled by an external voltage, the tuning range is $\Delta\omega \approx \frac{\left(\Delta G_n + \Delta G_p\right)K_0}{C}$ So G_n, G_p are increase tuning range is increase[10].

3. SIMULATION RESULT

The schematic of basic 3 stage differential ring oscillator using Multi Pass path shown in Figure 4. Output oscillation frequency waveforms are shown in Figure5 and Figure 6 for Vctrl = 1 V and Vctrl = 1.8 V respectively. In Figure 4 all the 3stages are shown. All the outputs are plotted using Cadence Spectre tool. Control voltage is applied to the gate of tail transistor while other inputs are acting as feedback. The oscillation frequency (f_{osc}) at V_{ctrl} = 1 V is 4.3354 GHz shown in figure 5 and the oscillation frequency (f_{osc}) at V_{ctrl} = 1.8V is 5.913 GHz as shown in figure 6. Figure 7 gives a graph between oscillation frequency and control voltage.Figure8 gives a graph between control voltage and phase noise(dBc/Hz) at offset frequency 1MHz. Figure 9 is PowerDissipation (dBm) at Control Voltage 1Volt

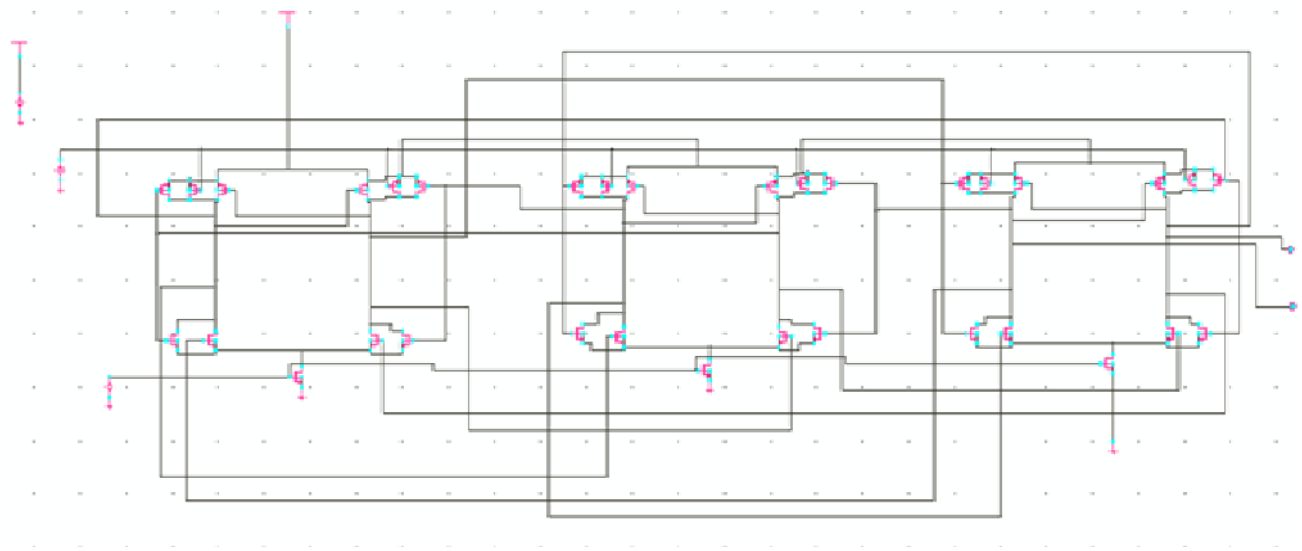

Figure 4 Ring Oscillator schematic designed using cadence tool.

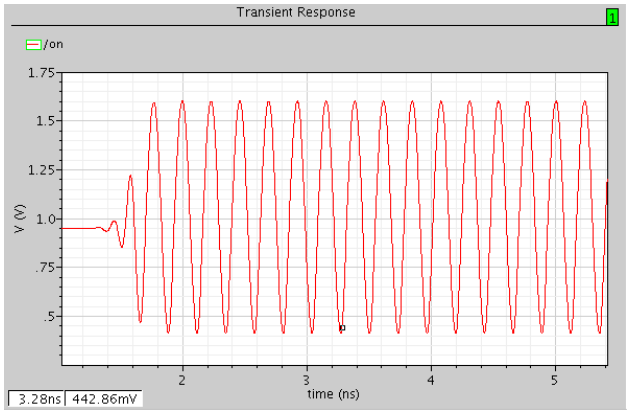

Figure 5 Transient response of 3 stage Ring Oscillator for V_{ctrl} = 1 V, f_{osc}=4.3354 GHz

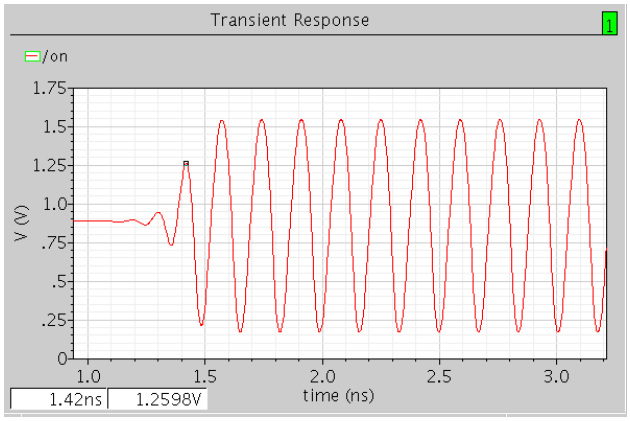

Figure 6 Transient response of 3 stage Ring oscillator for V_{ctrl} = 1.8 V, f_{osc}=5.913 GHz

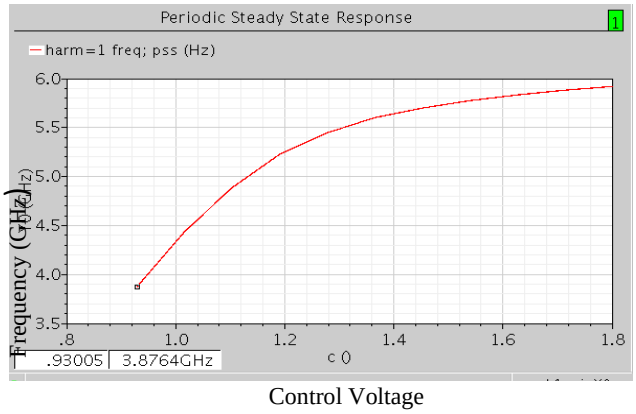

Figure 7 Oscillation frequency variation with control voltage

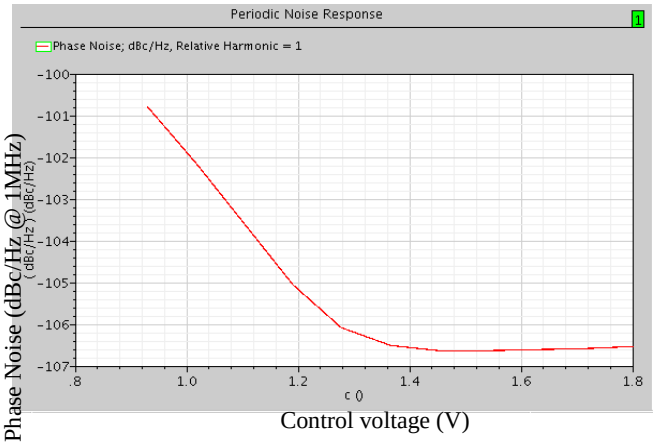

Figure 8 Phase Noise (dBc/Hz @ 1MHz) versus Control Voltage

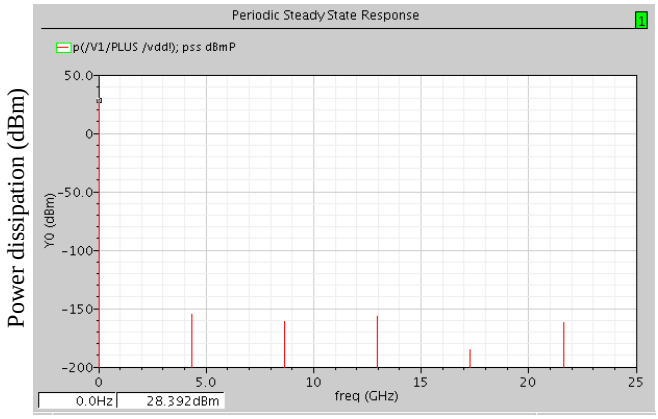

Figure 9 Power Dissipation (dBm) at Control Voltage 1Volt

Table 1 Performance Comparison (0.18 µm CMOS Process Technology)

Reference	Type	Tuning Range (GHz)	Phase Noise dBc/Hz @ 1 MHz	Supply Voltage (Volts)
[11]	Ring	5.16-5.93	-99.5	1.8
[2]	Ring	8.5-14	-95.35	1.8
[12]	Ring	8.4-10.1	-99.9	1.8
[13]	Ring	1.01-1.055	-103	1.8
[14]	Colpitts	4.61-5	-120.99	1.8
[15]	Hartley VCO	4.02-4.5	-122.5	1.8
This work	Ring	3.8741 - 5.913	-106	1.8

4. CONCLUSIONS

A 3 stage CMOS differential ring oscillator is designed successfully. It is designed using 1P6M 0.18µm CMOS process provided by TSMC. This differential ring oscillator is design without the use of any passive elements such as inductor or capacitor. It operates at wide band RF frequency. The control voltage is applied to tail transistor of differential delay cell. Phase noise and dissipation power analysis also done successfully.

5. REFERENCES

[1] S.-M. Yim, T. Chen, and K.K. O, "The effects of a ground shield on the characteristics and performance of spiral inductors," *IEEE J. Solid-State Circuits*, vol. 37, pp. 237–244, Feb. 2002.

[2] Yalcin A. Eken and John P. Uyemura , "The Design of a 14GHZ I/Q ring oscillator in 0.18 µmCMOS," IEEE, ISCAS,Page(s): IV - 133-136, Vol.4,2004

[3] Graninckx and Steyaert, M. "A 1.8-GHz Low-phasmnoise CMOS VCO using optimized hollow spiral inductors", *IEEE J. Solid-State Circuits*, Volume : 32 ,pp 736-744, May 1997.

[4] Timár, Á. Vámos, G. Bognár, "Comprehensive design of a high frequency PLL sythesizer for ZigBee application", *IEEE DDECS*,Prague, April 2006

[5] J. Mancatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," in ISSCC 1996 Dig. Tech. Papers, Feb.1996 pp.130-131.

[6] Sung Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata McGraw Hill, Edition 2003, Sixteenth reprint 2007.

[7] Razavi B., "Design of Analog CMOS Integrated Circuits", McGraw Hill Companies, inc., 2001.

[8] Changzhi Li and Jenshan Lin, "A 1–9 GHz Linear-Wide-Tuning-Range Quadrature Ring Oscillator in 130 nm CMOS for Non-Contact Vital Sign Radar Application" IEEE ,2009.

[9] B. Razavi, "Design of monolithic phase-locked loops and clock recovery circuits—A tutorial," in Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design.Piscataway, NJ: IEEE Press, 1996.

[10] L. Sun and T. A. Kwasniewski, "A 1.25-GHz 0.35- µm monolithic CMOS PLL based on a multiphase ring oscillator," IEEE J. Solid-State Circuits, vol. 36, no. 6, pp. 910–916, Jun. 2001

[11] Y. A. Eken and J. P. Uyemura, "A 5.9-GHz voltage-controlled ring oscillator in 0.18-µm CMOS," IEEE J. Solid-State Circuits, vol.39, No. 1, pp. 230-233, January 2004.

[12] Hai Qi Liu, Wang Ling Goh and Liter Siek, "A 0.18-µm 10-GHz CMOS Ring Oscillator for Optical Transceivers"pp1525-1527 IEEE2005.

[13] Zuow-Zun Chen and Tai-Cheng Lee, "The Design and Analysis of Dual-Delay-Path Ring Oscillators", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 58, NO. 3, MARCH 2011,pp 470-478.

[14] Ming-Da Tsai,Yi-Hsien Cho, and Huei Wang, "A 5-GHz Low Phase Noise Differential Colpitts CMOS VCO" IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 15, NO. 5, MAY 2005,pp327-329

[15] S.-H. Lee, Y.-H. Chuang, S.-L. Jang, and C.-C. Chen, "Low phase noise IEEE Microwave and Wireless Components Letters Vol. 17, No. 2, PP. 145–147, February 2007.