Survey on Various Types of Power in DLL

Ranjana Kumari Mishra
M.Tech Scholar

Rajesh Nema
Associate Professor

Teena Raikwar
Assistant Professor

NRI Institute of Information Science & Technology
Bhopal (M.P)-462021, India

ABSTRACT

A low power analysis of the jitter bounded is presented in this paper. Digital Delay Locked Loop (DLL) are commonly used for clock synchronization in modern ICs because of their superior stability and process portability. The DLL has a graduated course delay line and a phase interpolating fine delay line.

Keywords- All digital delay locked loop (ADDLL), clock generator, Jitter, agilent E4422B, Oscilloscope 54833D.

1. Introduction

There are two components that establish the amount of power dissipated in a CMOS circuit. These are:

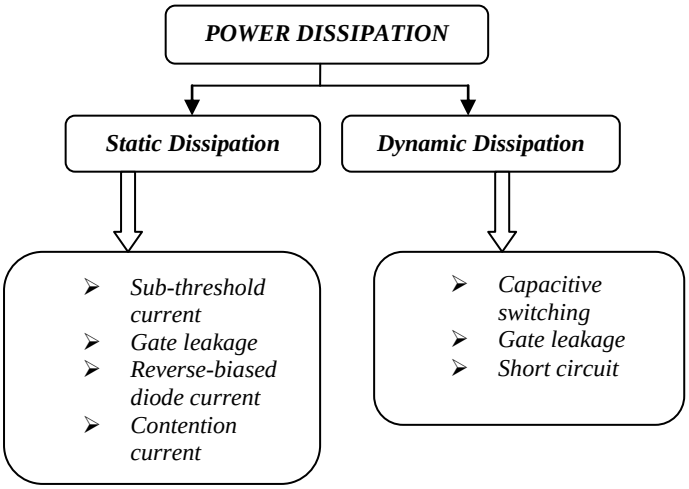


Figure 1.Block Diagram of power dissipation

Power dissipation has skyrocketed due to transistor scaling, chip transistor counts and clock frequencies.

- Static dissipation due to leakage current or other current drawn continuously from the power supply.
- Dynamic dissipation due to

➢ Switching transient current.

➢ Charging and discharging of load capacitances.

A. Static Dissipation

Static dissipation due to –

- Sub threshold conduction through OFF transistors
- Tunneling current through gate oxide
- Leakage through reverse-biased diodes
- Contention current in ratioed circuits

B. Dynamic Dissipation

- Charging and discharging of load capacitances
- Short circuit current while both PMOS and NMOS networks are partially ON

$$P_{total} = P_{static} + P_{dynamic}$$

2. Delay Locked Loop:

In electronics, a **delay-locked loop** (DLL) is a digital circuit similar to a phase locked loop (PLL), with the main difference being the absence of an internal voltage controlled oscillator, replaced by a delay line.

As the clock frequency of synchronous VLSI circuits increases, there arises a greater need to correctly align system clocks. Emphasis must be placed on suppressing clock skew and jitter. As the clock period is reduced, if jitter and skew remain the same, the total clock phase error is increased. This can affect many aspects of a synchronous system, including setup and hold times, data access times, and accuracy of internal control signals.

To eliminate clock skew, a simple, fixed-delay circuit might be used, but with variations in process, voltage, and temperature (PVT), the delay time would vary. Also, if the clock period were to change, the delay time would need to be modified. Therefore, a dynamic, variable delay circuit is needed to eliminate system clock skew across PVT and varying clock frequencies.

A Delay-Locked Loop (DLL) is such a circuit. Fig. 1 shows a DLL being used to ensure proper synchronization between a synchronous memory device and a memory controller. In this simple example, the DLL within the memory device is used to ensure that there is no skew between the control clock generated by the controller and the data coming out of the memory. This is especially important when a fast control clock is used; if skew remains in the output data while using a fast clock rate, the memory controller might have a difficult time distinguishing from one bit to the next being clocked from the memory.

As synchronous memory moves to other standards, such as double-data rate (DDR) devices, where data is clocked out on both the rising and falling edges of the control clock, the problem of internal clock skew is compounded. A DLL can solve this problem by ensuring proper synchronization across PVT as well as variations in the control clock frequency [1], [2].

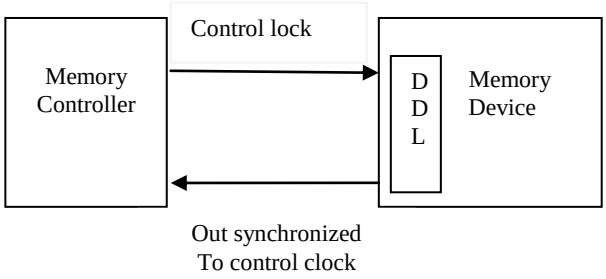


Figure2. DDL Usages Example

3. Literature Review

Descriptions Of Papers

(1) In 2011, *Chien-Hung Kuo, Hung-jing Lai,* and *Meng-Feng Lin* presented a fast locking delay locked loop (DLL) with jitter bounded features because this paper for locking process of the DLL without increasing the loop bandwidth of the system, a frequency estimator is designed to quickly detect the possible frequency range of the reference input clock. In general, a DLL output clock having narrower jitter can be expected and the amplitude of the ripple on the control voltage of VCDL could be reduced. The ripple might be caused by a dead zone of the phase-frequency detector (PFD), jitter of reference input, loop delay, charge loss of capacitor in LF, etc. In this paper, a clock uncertainty region is assumed to represent these non ideal effects such that the jitter of the output clock could be bounded within two clock edges served by distinct references. The presented delay locked loop (DLL) in this paper is implemented in a 0.18 um 1P6M CMOS technology. The output frequency ranges of the delay locked loop (DLL) and the frequency multiplier from 200 to 400 Mhz and 1 to 2 Ghz. And power dissipation of the delay locked loop (DLL) is 31.5 mw at 1.8V supply voltage.

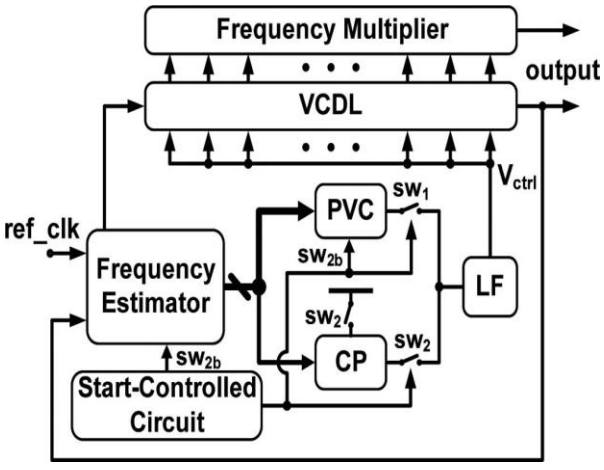


Figure 3. Architecture of the presented delay-locked loop

(2) In 2011, *Doo-Chan Lee, Kyu-Young Kim, Young-Jae Min, Jongsun Park,* and *Soo-Won Kim* presented a jitter and power analysis on a digitally controlled oscillator. This proposed mathematical analysis in this paper can be effectively used for the accurate and faster estimation of the DCO jitter and power consumption; thus, the overall DCO design time can be significantly reduce. There are validate our proposed mathematical modeling, the DCO has been designed and fabricated using a 0.13 um 1.2V CMOS process. A novel jitter analysis for the DCO considering variable delay stages.

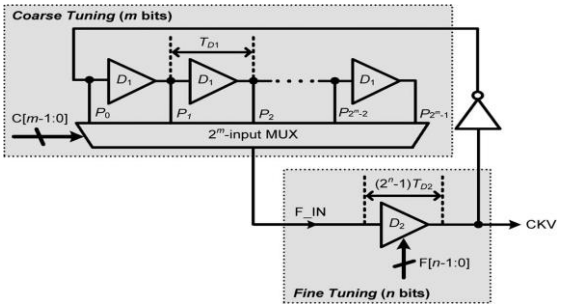


Figure 4. Block diagram of the Conventional DCO

(3) In 2012, *Brandon Rumberg,* and *David W. Graham* are presented a magnitude detection techniques in this paper like envelope detection or RMS estimation, which is needed for many low power signal analysis. This paper Present a low-power audio frequency magnitude detectors that simultaneously achieve both high temporal accuracy and high amplitude accuracy and this can we achieved by signal rectification whit high ripple peak detector and then averaging this rectified signal with an adaptive time.

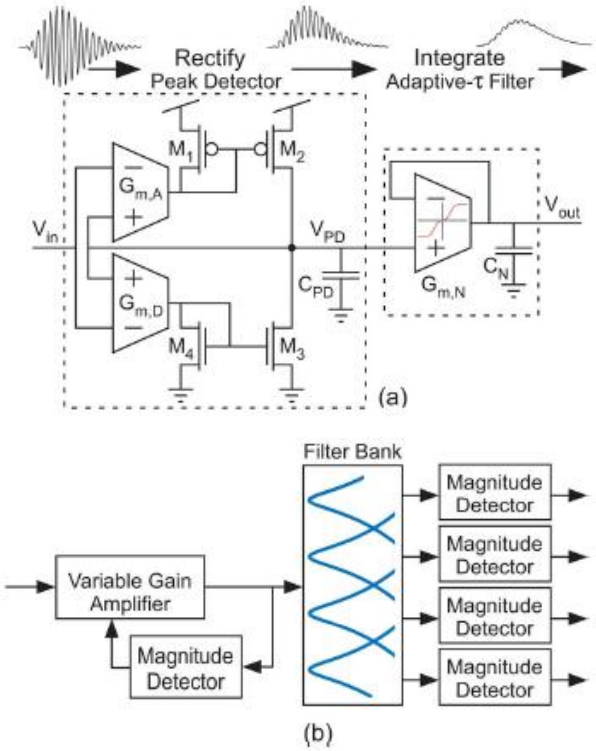


Figure 5. (a) Schematic of our magnitude detector. (b) Block diagram of an analog spectral-analysis system.

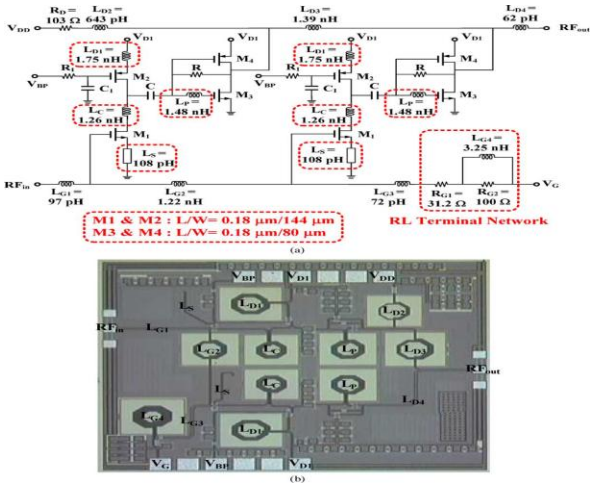
(4) In 2011, *Xiaohong Peng, Willy Sansen, Ligang Hou, Jinhui Wang* and *Wuchen Wu* present a power efficient frequency compensation topology Impedance Adapting Compensation (IAC) for loading serial *RC* impedance to the intermediate stage, performance can be boosted without. An extra power consumption. Remarkable achievements for both small- and large-signal performance have been reached with an optimized low-power low-voltage three-stage amplifier using this Impedance Adapting Compensation. In past research or in paper three stage NMC amplifier two miller capacitor Cm1 and Cm2 are attached from the output to each preceding stage forming two negative feedback loops, this nested miller compensation requires a large value of last stage transconductence gmL given by

$$gmL \geq 4*(2\text{^}GBW)\ C_L$$

Table I Summary Of Different Topologies

Topology	PM	GBW	T_{el}	$T_{el}/T_{el(NMC)}$
Single	$<90^0$	(g_m/C_L)	1.0	4.0
SMC	$<63^0$	$0.5(g_{m2}/C_L)$	0.5	2.0
NMC	$\approx 60^0$	$0.25(g_{m3}/C_L)$	0.25	1.0
NGCC	$\approx 60^0$	$0.25(g_{m3}/C_L)$	0.25	1.0
NMCF	$>60^0$	$<0.5(g_{m3}/C_L)$	<0.5	<2.0
MNMC	$\approx 63^0$	$\approx 0.5(g_{m3}/C_L)$	≈0.5	≈2.0

(5) In 2011, *Jin-Fa Chang* and *Yo-sheng Lin* presents 1.2-8.6 Ghz two stage distributed amplifier (DA) with cascade gain cell, which constitutes two enhanced CMOS inverters. Multiple noise suppression technique including three noise-suppression/gain- peaking inductor and RL terminal network. Because CMOS distributed ampliers have become more and more popular for wideband communication systems so that DA must have achieved excellent flat and high $|S_{12}|$ and an average NF and good linearity and wide bandwidth can be achieved simultaneously for a CMOS DA are design in this paper.



Fig(6) (a) Schematic of our magnitude detector, (b) chip micrograph of the proposed two-stage DA with cascaded inverter gain cell.

4. Problem Formulation

(1) In 2011 , *Chien-Hung kuo, Hung-Jing Lai*, and *Meng-Feng Lin* solved locking process of the DLL by mixed-mode multi-band fast-locking DLL with jitter-bounded feature was presented in this paper. An FE combined with the PVC is developed to accelerate the locking of the DLL' s output clock and using multi band fast locking delay locked loop (DLL) with jitter bounded feature is fabricated in a CMOS 0.18um 1P6M technology. Delay Locked Loop (DLL) is fed by a 250Mhz clock from an agilent E4422B(Agilent technologies, Santa clara, CA), and VCDL-Clk is measured by Agilent mixed signal oscilloscope 54833D.

(2) In 2011, *Doo-Chan Lee, Kyu-Young Kim, Young-Jae Min, Jongsun Park and Soo-Won Kim* solved using a novel jitter. proposed a simple yet accurate analysis of power and jitter on the DCO. Analysis for the DCO considering variable delay stages. DCO has fabricated using 0.13um 1.2V CMOS process.

(3) In 2012, *Brandon Rumberg* and *David W. Graham* solved high power magnitude detector circuit. They are used to low power magnitude detector circuit, which achieves good temporal responsiveness through the use of novel peak detector non linear integrator topology. A low power audio frequency magnitude detector that simultaneously achieves both high temporal accuracy and high amplitude accuracy. The circuit has been fabricated in a 0.18um CMOS process. Author successfully find problem and that solved.

(4) In 2011, *Xiaohong Peng, Willey Sansen, Ligang Hou, Jinhui Wang* and *Wuchen Wu* proposed a power-efficient multistage amplifier frequency compensation method and the problem resolve by using Impedance Adapting Compensation (IAC) topology and it has been suited for low-power low voltage application. A three stage Impedance Adapting Compensation (IAC) amplifier was implemented and fabricated in a 0.35um CMOS technology for improving performance parameters such as stability, gain-bandwidth product and power dissipation which show in the paper.

(5) In 2011, *Jin-Fa Chang and Yo-Sheng Lin* solved by using Multiple Noise Suppression techniques including three noise-suppression/gain peaking inductors and an RL terminal network were used to achieve flat and low noise figure(NF) and flat and high gain power at the same time. That they are successfully solved the problems**.**

5. Conclusion

This paper discussed common topologies for jitter synchronization. Analog and Digital Delay Locked Loop (DLL) implementation paying special attention to the effect of large delay model in the feedback path. The jitter simulation showed that at high frequency there was much less margin to the jitter target than at lower frequency. To improve this, the delay line could be divided into three sections- a shallow section with no graduation for maximum performance at high frequencies, a middle section with moderate graduation for balanced performance versus layout area, and a deep section with a large graduation value to take advantage of the jitter margin at the lower frequencies.

6. References

[1] M. Zanuso, P. Madoglio, S. Levantino, C. Samori, and A. L. Lacaita,"Time-to-digital converter for frequency synthesis based on a digital bang-bang DLL,"*IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 57, no. 3,Mar 2010, pp. 548–555, .

[2] Y . S. Hwang, C. M. Kung, H. C. Lin, and J. J. Chen, "Low-sensitivity, low-bounce, high-linearity current-controlled oscillator suitable for single-supply mixed-mode instrumentation system," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 56, no. 2, Feb 2009, pp. 254–262,.

[3] D.-C. Lee, K.-Y. Kim, Y.-J. Min, K.-M. Kim, A. Abdullah, J. Park, and S.-W. Kim, "A low-power all-digital PLL with power optimized digitally controlled oscillator," in *Proc. IEEE Int. Conf. EDSSC*, 2010, pp. 1–4. [4] K.-H. Choi, J.-B. Shin, J.-Y. Sim, and H.-J. Park, "An interpolating digitally-controlled oscillator for a wide-range all-digital PLL," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9,Sep 2009, pp. 2055–2063,.

[5] J. Alegre, S. Celma, J. G. del Pozo, and N. Medrano, "Fast-response low-ripple envelope follower," *Integration, the VLSI J.*, vol. 42, no. 2, 2009, pp. 169–174,.

[6] E. Rodriguez-Villegas, P. Corbishley, C. Lujan-Martinez, and T. Sanchez-Rodriguez, "An ultra-low-power precision rectifier for biomedical sensors interfacing," *Sensors and Actuators A: Physical*, vol. 153, no. 2, 2009, pp. 222–229,.

[7] F. Yuan, "Design techniques for ASK demodulators of passive wireless microsystems: a state-of-the-art review," *Analog Integr. Circuits Signal Process.*, vol. 63,2010, pp. 33–45,.

[8] S.-C. Liu, A. van Schaik, B. Minch, and T. Delbrück, "Event-based 64-channel binaural silicon cochlea with Q enhancement mechanisms," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2010, pp. 2027–2030.

[9] B. Rumberg, D. Graham, V. Kulathumani, and R. Fernandez, "Hibernets: Energy-efficient sensor networks using analog signal processing," *IEEE J. Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 3, Sep 2011, pp. 321–334,.

[10] J. F. Chang and Y. S. Lin, "A 3–10 GHz low-power, low-noise CMOS Distributed amplifer using splitting-load inductive peaking and noise-suppression techniques", IET Electron, Lett, vol. 45, no. 20, 2009 pp. 1035,.

[11] B. Machiels, P. Reynaert, and M. Steyaert, "Power efficient distributed low-noise amplifier in 90 nm CMOS," in *Proc. IEEE RFIC Symp.*, 2010, pp. 131–134.

[12] R. M. Weng, C. Y. Liu, and P. C. Lin, "A low-power full-band lownoise amplifier for ultra-wideband receivers," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 8,Aug 2010, pp.2077-2083**,.**