Area and Power Efficient CMOS Adder Design by Hybridizing PTL and GDI Technique

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ABSTRACT

In this paper an area and power efficient 9T adder design has been presented by hybridizing PTL and GDI techniques. The proposed adder design consist of 5 NMOS and 4 PMOS. A PTL based 5T XOR-XNOR module has been proposed to improve area at 120 nm and 90nm technology and compared with the previous XOR-XNOR design. The proposed Hybrid full adder design is based on this area efficient 5T XOR-XNOR module design. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the proposed full adder. XOR-XNOR modules outputs act as input to Carry and Sum module which has been implemented by the GDI MUX. The proposed adder has been designed and simulated using DSCH 3.1 and Microwind 3.1 on 120nm and 65nm technology. Also the simulation of layout and parametric analysis has been done for the proposed full adder design. Power and current variation with respect to the supply voltage and temperature has been performed on BSIM-4 and LEVEL-3 on 120nm. Results show that area consumed by the proposed hybrid adder is 98.5μm^2 on 120nm technology. At 1.2V input supply voltage the proposed adder has shown an improvement of 76.9% in power and 74.82% in current on BSIM-4 120nm technology.

Keywords

BSIM, CMOS, Gate Diffusion Input, Pass transistor logic, VLSI.

1. INTRODUCTION

Full adder is a basic building block in the arithmetic unit of digital signal processors and application specific integrated circuits used in various digital electronic devices. In the world of technology the demand of portable devices are increasing day by day. Demand and popularity of these devices depends on the small silicon area, higher speed, longer battery life and reliability. Overall system performance can be affected by enhancing the performance of the full adder circuit used in these systems. Power and area consumption is a key limitation in many electronic devices such as mobile phone and portable computing systems etc. So far several logic styles have been used to design full adder cell to improve area and power consumption [1]-[4]. Design of full adder by using conventional CMOS design style has been presented. To generate the output transistor level design of CMOS full adder contains total of 14 PMOS and 14 NMOS transistors and two CMOS inverter. All NMOS and PMOS transistors used in this circuit have the same W/L ratio. It is required to adjust the transistor dimensions individually to get optimized time domain performance of the circuit. In [5]-[13] the area and power delay performance of full adder designs by different logic styles have been investigate.

2. ADDER DESIGNS

In the recent past various approaches of CMOS full adder design by using various different logic styles has presented and unified into an integrated design methodology. Circuit area, speed and power consumption are the main criteria of concern in CMOS full adder design which often conflict with the design methodology and act as a constrain on the design of full adder circuits. These performance criteria's are individually investigated, analyzed and their interaction to develop both quantitative and qualitative understanding of the various designs have been presented in literature**.**

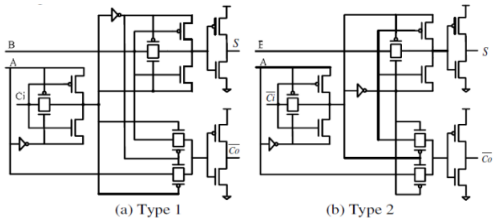

Fig 1: 20T Transmission Gate based Full Adder [14]

Full adder design by using 20 and 16 transistors has been proposed in [14]-[16]. As transmission gate based full adder designs are low power designs and consume fewer transistors. A new transmission gate based full adder has shown in Fig. 1 in which only 20 transistors for achieving high driving ability and low power consumption [14].

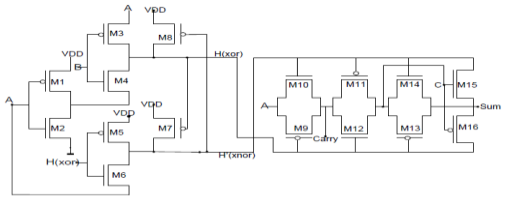

Fig 2: 16T 1 Bit Full Adder [16]

In TG full adder XOR and multiplexing function are implemented by using transmission gates and inverter shown in Fig.2. In the proposed design author used the TG based XOR and MUX because there is no threshold loss problem. If logic style shows good performance in one parameter it can be on the expense of the others. The majority of the power dissipated in CMOS VLSI circuits is by dynamic power dissipation which is the power dissipated during charging or discharging of the load capacitance of a given circuit [15]-[16]. Three different full adder designs are shown in Fig.3, 4, [17], [19].

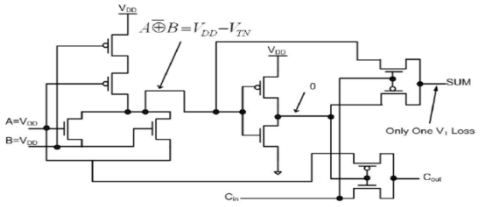

Fig 3: 10T 1 Bit Full Adder [17]

An another approach of full adder design by 10 transistor is proposed by author which provide the features of low complexity, higher speed, low operating voltage and low energy consumption [18].XOR is a basic building block of full adder architecture. So if the transistor count in XOR circuit can be reduced it can further decrease the area consumption of full adder. A new full adder design by using 10 transistors is proposed by the authors in [19] which consists XOR module by only four transistors.

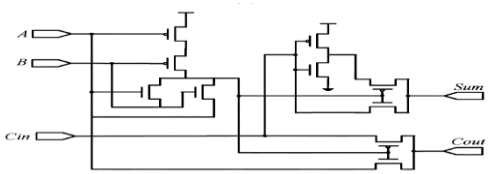

Fig 4: 10T Full Adder design [19]

Design is based on complementary and level restoring carry logic (CLRCL). Design provides features like low operating voltage, high speed and low PD product. Low power consumption is due to the fact that circuit does not contain any direct path to the ground. Inverted buffered XOR/XNOR design is used to overcome the threshold loss problem encountered in pass transistor logic design. Although threshold loss problem is common in 10T full adder, CLRCL design can give higher speed while using much smaller transistor count.

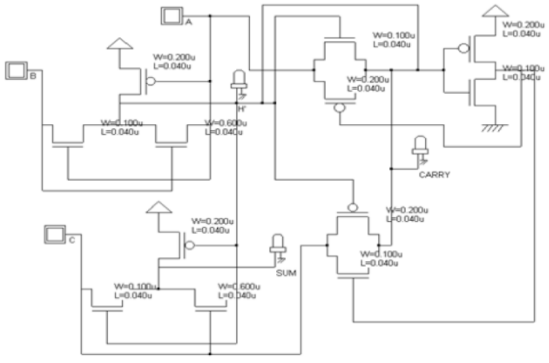

Fig 5: 12T 1 Bit Full Adder [20]

This full adder is simulated using different technologies i.e. 32nm and 120nm. Since the transistor count is less hence the area consumption is very less as compared to the convention CMOS full adder design In paper PTL and inverter based XOR/XNOR circuits and 4 different 2x1 MUX are also shown by the authors. In [20] and [21] full adder circuits has been implemented by 3T XOR/XNOR hybrid CMOS design style and MUX based style using MICROWIND designing tools. Full adder circuit in Fig.5 [20] consist 7 NMOS and 5 PMOS.

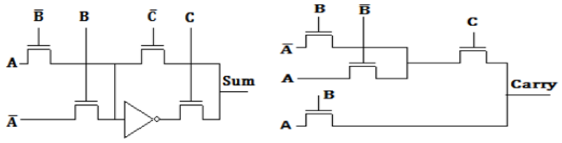

Fig 6: MUX based full adder [21]

In [21] authors have proposed a multiplexer based 10T full adder design by using same designing tool as in [20] shown in Fig.6. The proposed adder cell gives better performance in terms of power, propagation delay and PDP than the other existing six adder circuits. Proposed full adder consist multiplexer based sum and carry circuit.

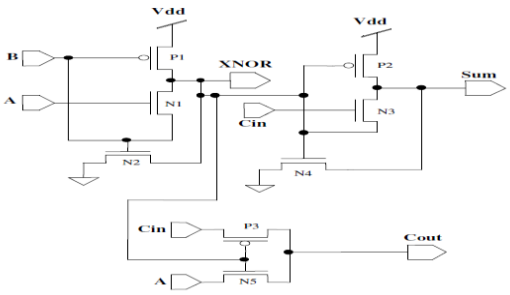

Fig 7: Full adder using two XNOR gate and MUX [22]

In [22] authors present a new XNOR gate using three transistors which shows power less power dissipation in the full adder design as shown in Fig.7. By XNOR cell 8T full adder has been designed. XNOR cell is made by the 2 NMOS and one PMOS.

3. XOR-XNOR MODULES

The simultaneous generation of the two non-skewed XOR and XNOR outputs is highly desirable in full adder designs in which sum and carry outputs are obtained from 2x1 MUX. Some combined XOR-XNOR designs that combine the implementation of both the XOR and XNOR functions in one circuit are discussed below [5], [6], [11], [23]-[26]. The reported XOR-XNOR circuit in [5] shown in Fig. 8 consist two complementary feedback NMOS and PMOS transistors to restore the non full voltage swing.

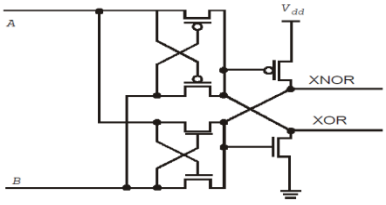

Fig 8: 6T XOR-XNOR Gate [5]

At low-supply voltage above circuit shows an unsatisfactory performance, modified the circuit of above fig has been shown in Fig.9. In this circuit the two series PMOS and NMOS transistors are added to get the full output voltage swing for all possible input combinations.

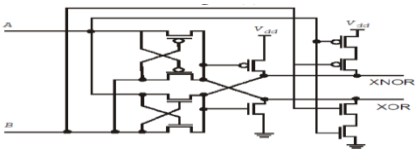

Fig 9: Modified 6T XOR-XNOR Gate [5]

A new 10T XOR-XNOR circuit for full adder has been shown in Fig.10 [11]. The proposed circuit produces both XOR and XNOR signal with full voltage swing. This circuit has been designed by CPL and TG logics. Proposed circuit has advantages of less power consumption, full voltage swing and simple design.

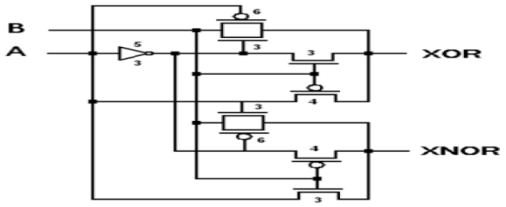

Fig 10: 10T XOR-XNOR Circuit [11]

In [24] XOR –XNOR functions are simultaneously achieved by using GDI technique shown in Fig.11. Circuit by using this technique uses 6 transistors to generate balanced XOR and XNOR output. Same GDI cell is used three times with different Logic functions to get to complementary output.

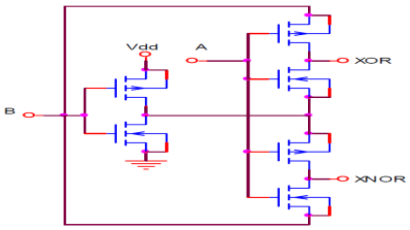

Fig 11: GDI XOR-XNOR cell [24]

The XOR and XNOR circuit shown in Fig.12 [25] is based on non-complementary input signals and has a better power delay product and noise immunity. To remove the threshold voltage loss problem commonly encountered in pass transistor logic Design the NMOS and PMOS transistors are added to the basic circuits.

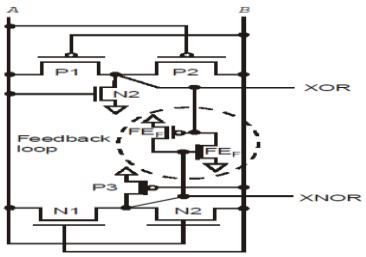

Fig 12: 8T XOR-XNOR Circuit with feedback loop [25]

8T XOR–XNOR module that generates XOR and XNOR outputs simultaneously is reported in [6], [26] has been shown in Fig.13 can provides a full voltage swing at low supply voltage. XOR–XNOR circuit is based on CPL logic. The first half of the module is made by only NMOS pass transistors for the generation of the two complementary outputs. To overcome threshold loss problem the cross-coupled PMOS transistors are connected between XOR and XNOR output.

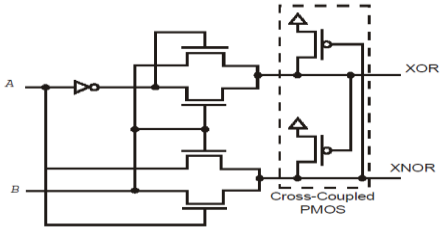

Fig 13: XOR-XNOR circuit [6], [26]

4. GDI TECHNIQUE

GDI method is based on the use of a simple cell as shown in Fig 14. The basic GDI cell looks like the standard CMOS inverter, but there is an important difference that GDI cell contains 3 inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).

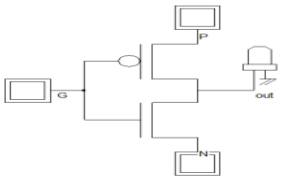

Fig 14: Basic Gate Diffusion Input Cell

No of different logic functions can be implemented by only two transistors by using Gate diffusion input (GDI) approach. GDI approach is suitable for design of high speed, power efficient circuits with improved logic level swing and static power characteristics using a reduced number of transistors as compared to CMOS and PTL techniques [27]-[28].

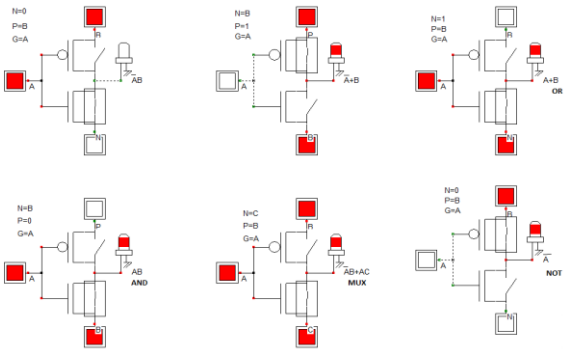

Fig 15: Various Function of Basic GDI Cell

Various logic functions of GDI cell for different input combination is shown in Fig.15. Six different functions can be implemented by GDI cell. Colored box and output LED is showing high output.

5. PROPOSED ADDER SCHEMATIC

The design of propose full adder consists three modules. Module 1 comprises 5T XOR –XNOR module. Module 1 produces two intermediate signals which are passed to the module 2 and module 3 to obtain sum and carry output as shown in Fig.16. Module 2 and 3 are GDI 2x1 MUX with different input and select lines which produce carry and sum output respectively. Module 1 produces two outputs $A \oplus B$ and AΘB. For module 2, $A \oplus B$ act as a select line and A, C as inputs. On the other hand for module 3, C act as a select line and AΘB and $A \oplus B$ as

inputs. Proposed full adder design is hybridized design because two different logic styles have been used to make the full adder. Module 1 has been made by PTL logic and GDI technique has been used for module 2 and 3.

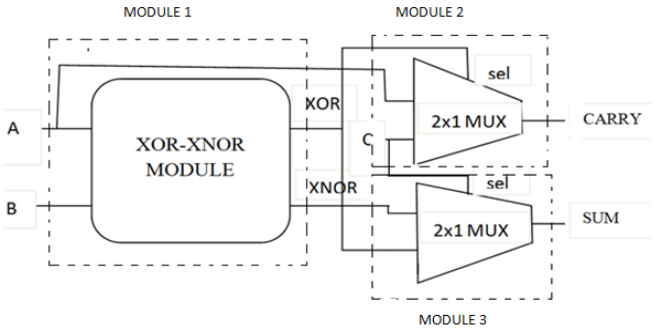

Fig 16: Logic Block Diagram of Proposed Full Adder

Proposed full adder has been implemented by using only 9 transistors i.e. five transistors in module 1and module 2and 3 has been implemented by using 2T GDI cell. Sum is realized by module 1 and module 3 as per equation 1 and carry is realized by module 1 and module 2as per equation 2. Module 1 has been implemented by proposed 5T XOR-XNOR module and GDI technique has been used for module 2 and 3. In module 1 a combined XOR-XNOR cell is used to drive the selection lines and, control signal lines of the multiplexer in module 2 and 3. Proposed XOR-XNOR module in Fig.17 has been designed by the PTL logic and consist only 5 transistors which is least as compared to all previous discussed designs.

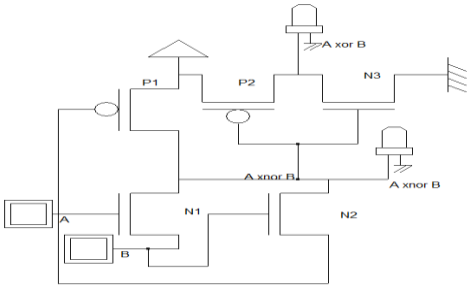

Fig 17: Proposed PTL based XOR-XNOR Module

Proposed design has been made by 3 NMOS and 2 PMOS transistors which provide an area efficient design as compared to previous discussed designs [5],[6],[11],[23]-[26]. MOS logic states on four different input combination has been shown in table 1 for both XOR and XNOR output. Comparative analysis of proposed XOR-XNOR module in terms of area with other existing XOR-XNOR module has been shown in Table-2.

Table 1. Analysis of Proposed XOR-XNOR Module

Inputs		MOS Logic State					Output	
A	**B**	**N1**	**N2**	**N3**	**P1**	**P2**	A⊕B	AΘB
0	0	OFF	OFF	ON	ON	OFF	0	1
0	1	OFF	ON	OFF	ON	ON	1	0
1	0	ON	OFF	OFF	OFF	ON	1	0
1	1	ON	ON	ON	OFF	OFF	0	1

Verification and simulation of the functionality of proposed XOR-XNOR module is first done by using DSCH 3.1 designing tool. Channel width should be accurate for efficient working of the design. Channel width can be changed in DSCH schematic editor [29]. The timing simulated of 5T XOR –XNOR module is shown in Fig. 18 which shows the accurate functioning of the proposed design.

Proposed XOR-XNOR module has been compared with the previous discussed XOR-XNOR design in terms of area in microwind designing tool. Microwind deals with both front end and back end designing. In front end it has DSCH in which both transistor level and gate level designing can be done.

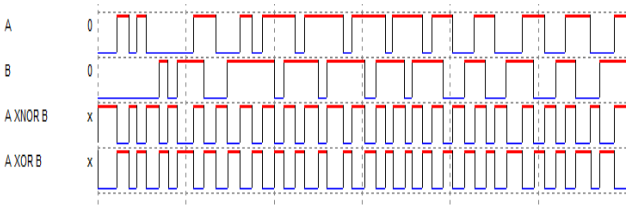

Fig 18: Timing Simulation of Proposed XOR-XNOR module

DSCH generate a verilog file which can be compiled by the microwind back end designing tool to get power and area consumption. Proposed XOR-XNOR module is compared with the discussed XOR-XNOR design in terms of area on 90nm and 120nm technologies.

Table 2. Comparative Analysis of Proposed XOR-XNOR Module in terms of area with other existing XOR-XNOR

XOR-XNOR module		**[5]**	**[11]**	**[24]**	**[25]**	**[26]**	**Proposed**
NMOS		3	5	3	3	4	3
PMOS		3	5	3	3	2	2
Area (μm^2)	**120nm**	58.3	115	67.7	58.3	69.2	49.7
	90nm	40.5	80	47	40.5	48.1	34.5

Outputs of module 1 act as inputs for the module 2 and module 3. The logical Boolean expression for module 2 and 3 can be expressed as:

$$SUM = C(A \Theta B) + \overline{C}(A \oplus B) \quad (1)$$

$$CARRY = C(A \oplus B) + A(A \Theta B) \quad (2)$$

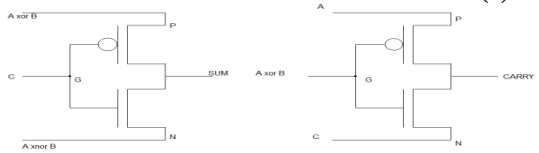

Fig 19: Use of GDI Cell as Module 2 and 3

GDI technique is an efficient technique for designing area and power efficient digital circuits as compared to PTL,TG,CPL and DPL designing approaches [30]-[32].Schematic of proposed full adder has been designed and simulated in DSCH 3.1 logic editor and simulator.

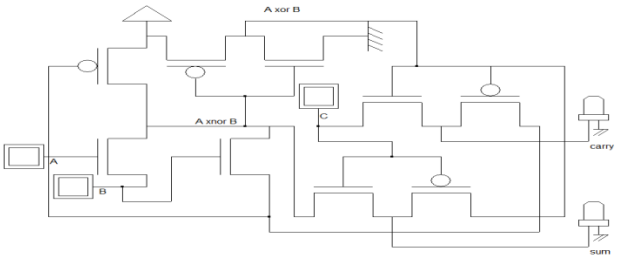

Fig 20: Proposed 9T Hybrid Full Adder Design

Before the actual layout design it necessary to validate the schematic of logic circuit. DSCH and MICROWIND designing tools works parallel. Firstly the design is simulated in DSCH designing tools to know the exact functionality of the circuit. Proposed hybrid full adder and its timing simulation have been shown in Fig.20 and 21

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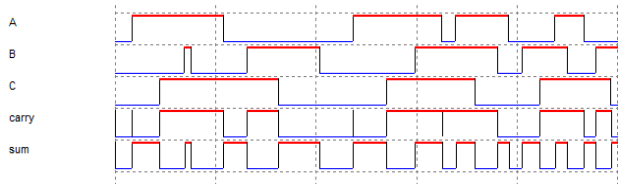

Fig 21: Timing Simulation of Proposed Hybrid Full adder

In order to simulate the full adder at logic level the design has been made in the DSCH tool and after launching the simulation the timing waveform can be obtained by chronogram icon. As seen in the waveform the value of carry and sum output is according to required full adder operation. Timing simulation shows the exact functionality of full adder for both sum and carries output.

6. LAYOUT ANALYSIS

For a very complex circuit it become very difficult to conduct the manual layout so an automatic layout generation approach is proffered. The schematic diagram has been firstly designed and validated using DSCH tool at logic level. Although at logic level DSCH have feature to analyze timing simulation as well as power consumption but accurate layout information is still missing. Verilog file is generated by the DSCH tool which is understandable by the MICROWIND to construct the corresponding layout with exact desired design rules. Another way to create the design is by NMOS and PMOS devices using cell generator provided by the microwind. The advantage of this approach is to avoid any design rule error. W/L can be adjusted by the MOS generator option on microwind tool.

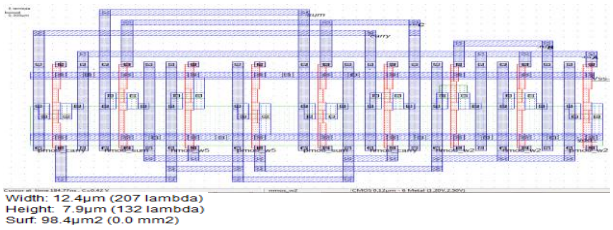

Fig 22: layout of proposed Full Adder on 120nm

By default W=0.6µm (10 Lambda) and L=0.12µm (2 Lambda) in 120nm technology and W=0.3µm and L=0.07µm in 65nm technology. Due to less W/L ratio at 65nm technology area is also less at 65nm as compared to 120nm technology.

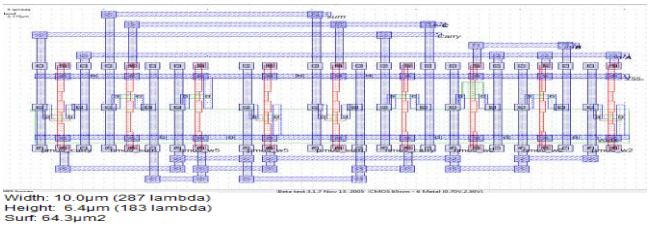

Fig 23: Layout of Proposed Full Adder on 65nm

This means the layout result will change if we use 120nm or 65nm design rules. The supply property and other simulation information have been added in the layout automatically as shown in Fig. 22 and 23.

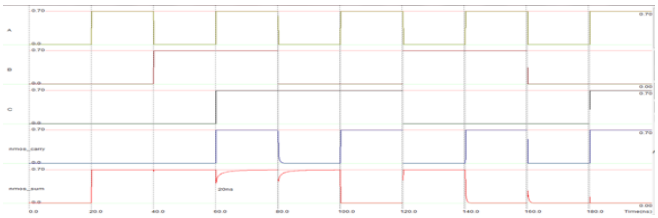

Fig 24: Analog Simulation of proposed full adder on 65nm

Finally the analog simulation has been obtained to know the power consumption at different voltage and temperature. Analog simulation is carried out for proposed full adder at both 120nm and 65nm technology. For 120nm VDD is fixed to 1.2V and VSS to 0V whereas for 65nm VDD is 0.7V.Simulation can be done by four ways in microwind.-Voltage vs. Time, Voltage and current vs. time, Voltage vs. Voltage and Frequency vs. Time. Voltage vs. Time simulation for proposed hybrid full adder on both 65nm and 120 nm has been shown in Fig.24 and 25. From the analog simulation it is clear that the proposed hybrid full adder work efficiently on smaller and higher nm technology.

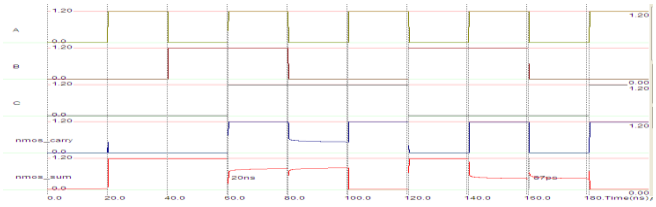

Fig 25: Analog Simulation of Proposed Full Adder on 120nm

7. SIMULATION RESULTS

The performance of proposed hybrid full adder has been evaluated in terms of area and power on 120nm technology. Simulation has been performed using Microwind 3.1. Results are measured in terms of variation in power and current with respect to the variation in voltage and temperature.

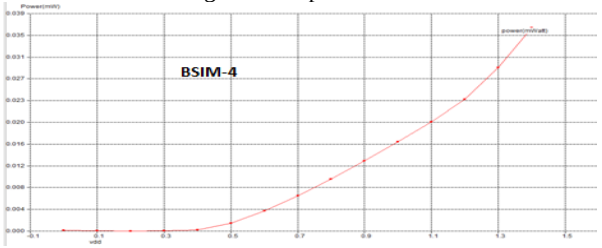

Fig 26: Power Variation of with Supply Voltage on BSIM-4

Simulation results have been measured using the MOS Empherical model Level-3 and BSIM Model-4 at different

power supply voltages and different temperatures. Threshold voltage on both levels is 0.4V and gate oxide thickness is 2nm.

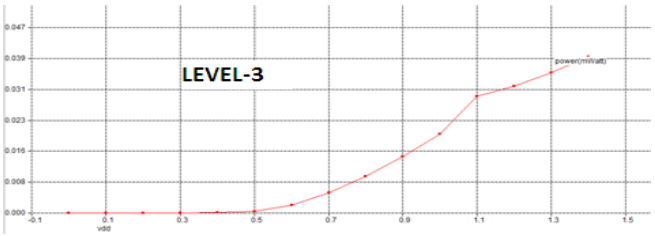

Fig 27: Power Variation with Supply Voltage on LEVEL-3

All the results are measured using MOS Empherical model Level-3 and BSIM Model-4 in terms of power and current on voltage levels 0.6, 0.8, 1, 1.2 and 1.4V on operating temperature 27^0C. MOS Empherical model Level-3 work with 10 different curve fitting parameters whereas BSIM Model-4 work with 19 different parameters.

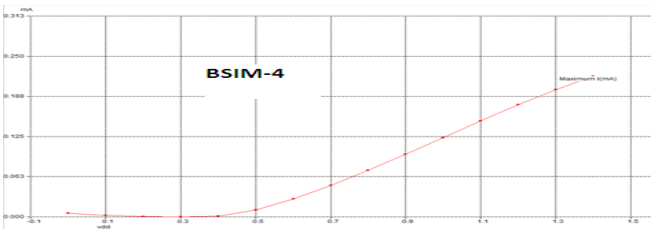

Fig 28: Current Variation with Supply Voltage on BSIM-4

Difference between these two levels is that BSIM-4 work with more curve fitting parameters. As the average power consumption is proportional to square of voltage.

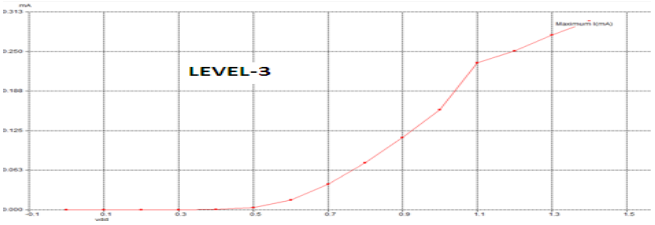

Fig 29: Current Variation with Supply Voltage on LEVEL-3

To know the incremental change in power and current from 0V to 1.5V parametric analysis tool of microwind has been used. Steps of incremental voltage are 0.1V.

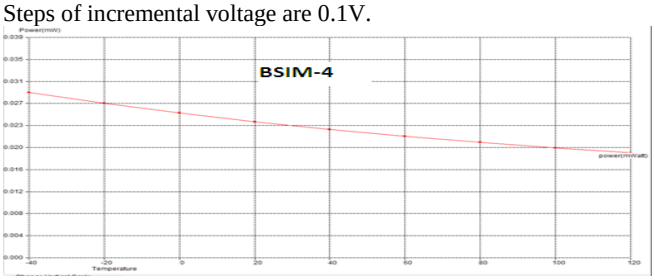

Fig 30: Power Variation with Temperature on BSIM-4

Results plotted for change in power and current have been shown in Fig.26 and 28 for BSIM-4 and in Fig.27 and 29 for LEVEL-3 are showing non linear dependence of the power with VDD. Result of variation of power and current is with respect to temperature has been shown in Fig. 30 and 32 for BSIM-4 and in Fig.31 and 33 for LEVEL-3.

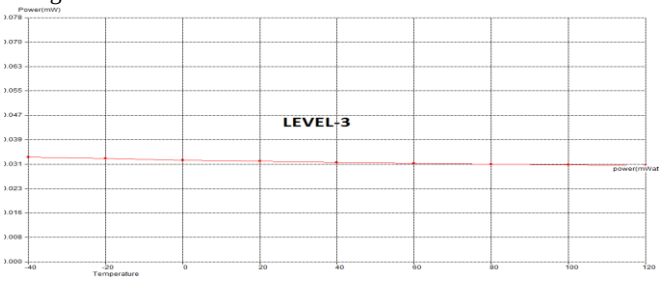

Fig 31: Power Variation with Temperature on LELEL-3

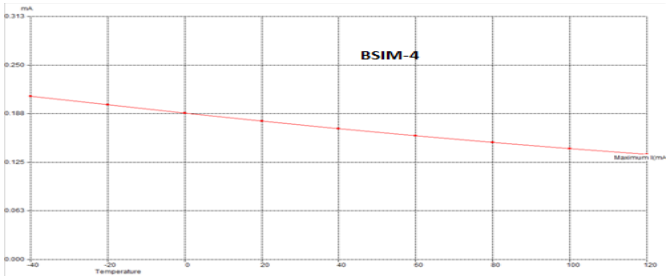

Fig 32: Current Variation with Temperature on BSIM-4

Power is decreasing with the increase in temperature for both level-3 and BSIM-4. Simulation results have been shown in table-3. From table it is clear that power dissipation increases with the power supply. Table also shows that the power and current dissipation is less at BSIM-4 as compared to LEVEL-3.

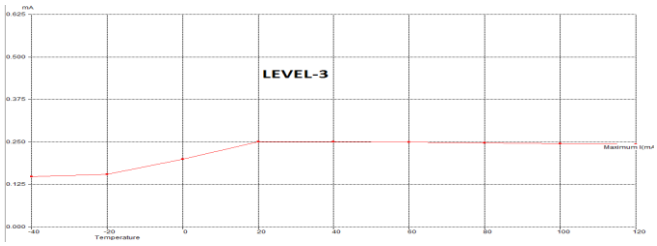

Fig 33: Current Variation with Temperature on LEVEL-3

Table 3. Simulation results of proposed Hybrid Full Adder Design

Design Technology	Area(μm$^{2)}$	Threshold Voltage	Supply Voltage(V)	Power Dissipation(μW)		Maximum Current(μA)	
				LEVEL-3	BSIM-4	LEVEL-3	BSIM-4
5T PTL XOR-XNOR Module and GDI MUX based Hybrid Full Adder On **120nm**	A=98.4(μm^2) W=12.4(μm) L= 7.9(μm)	0.4 V	0.6	2	4	16	28
			0.8	9	9	75	72
			1	20	16	158	123
			1.2	32	24	215	175
			1.4	39	36	298	219
			Temperature (^{0}C)	**Power Dissipation(μW)**		**Maximum Current(μA)**	
				LEVEL-3	**BSIM-4**	**LEVEL-3**	**BSIM-4**
			20	32	24	251	178
			40	32	23	251	168
			60	32	23	250	159
			80	31	20	247	150
			100	31	19	245	142

Proposed full adder has shown improvement in terms of area, power and current as compared to other full adder design. Results show that area consumed by the proposed hybrid adder is 98.5μm^2 on 120nm technology. At 1.2V input supply voltage the proposed adder has shown an improvement of 76.9% in power and 74.82% in current on BSIM-4-120nm technology as compared to full adder design proposed in [20]. Proposed adder also has shown an improvement of 86.3% in power and 80.8% in current at LEVEL-3-120nm technology. Result comparison of proposed full adder with design in [20] has shown in Table-4.

Table 4. Comparison of Proposed Adder at 120nm Technology

Parameters	Proposed Adder Design	Adder design in [20]
Area (μm^2)	98.4 μm^2	103.8 μm^2
NMOS	7	5
PMOS	5	4
Power dissipation (μW) at level-3	32 μw	235 μw
Power dissipation (μW) at BSIM-4	24 μw	156 μw
Maximum Current (μA) at level-3	215 μA	1125 μA
Maximum Current (μA) at BSIM-4	175 μA	870 μA
Threshold Voltage (V)	0.4V	0.4V
Supply Voltage (V)	1.2V	1.2V
Operating Temperature (^{0}C)	27^{0}C	27^{0}C

8. CONCLUSION

An alternative hybrid full adder design by using PTL based XOR-XNOR module and GDI MUX has been introduced which consist only 9 transistors. Proposed full adder has been implemented by using 5 NMOS and 4 PMOS transistors. A new area efficient XOR-XNOR module has been proposed which is designed by only 5 transistors. Proposed XOR-XNOR model consume 49.7μm^2 area at 120nm. Proposed module has been also compared in terms of area from other existing XOR-XNOR modules and proposed XOR-XNOR module has been proven area efficient as compared to other. This XOR-XNOR module has been used as a basic module in proposed hybrid full adder. Area and simulation of proposed full adder has been shown on 120nm and 65nm technology. The simulation results have been shown on LEVEL-3 and BSIM-4 models. Area of proposed design is 98.4μm^2 on 120nm technology and 64.3μm^2 on 65nm technology. At 1.2V input supply voltage the proposed adder has shown an improvement of 76.9% in power and 74.82% in current on BSIM-4-120nm technology. The proposed circuit can work efficiently with minimum voltage supply of 0.4V and can work on wide range of frequency range between 2MHz to 400MHz. simulation results shows that the power consumption and current is less at BSIM-4 as compared to LEVEL-3 model.

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