

# Designing and Simulating a 2.4 GHz Integer-N Frequency Synthesizer with 1 MHz Frequency Step

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## ABSTRACT

This article consists on the design and the simulation of a 2.4 GHz Integer-N Frequency Synthesizer with 1 MHz Frequency Step which can be used for exchanging data over short distances (using short-wavelength radio transmissions in the ISM band from 2400–2480 MHz) from fixed and mobile devices, creating personal area networks (PANs) with high levels of security. The effects of the sideband's spurious noise on the adjacent channels and the phase noise in each component in the circuit on system performances are discussed. An accurate transient analysis of the PLL system is also presented in this work. The obtained output spectrum presents a noise density of -82dBc/Hz at an offset frequency of 1MHz, a switching time for a frequency jump of 80 MHz about 50.83  $\mu$ S. The essential component used to design the PLL frequency synthesizer is ADF4106 from Analog Devices, Inc.

## Keywords

Frequency Synthesizer, Phase Locked Loop (PLL), phase noise, switching time, ADF 4016.

## 1. Introduction

Today's mobile communication systems require a higher quality of communication, higher data rates, more increased frequency operation, and more channels per unit bandwidth.

Frequency synthesizers are critical components in modern mobile communications systems, powering both transmitters and receivers. Typically, they are designed with a phase-locked-loop (PLL) approach [1],[2]. PLL frequency synthesizers are widely used in all forms of radio communications systems [3].

In nearly all the PLL applications, it is required to generate low noise and low spur signals while achieve fast settling time. The phase locked loop (PLL) has been widely used in wireless communication systems due to the high frequency resolution and the short locking time [4].

The main objective of this paper consists on the design and simulation of a 2.4 GHz Integer-N Frequency Synthesizer with 1 MHz Frequency Step. This paper discusses the effects of the phase noise in each component in the circuit on the system performances. The loop filter must be designed for the correct balance between reference spurs and lock time that the system requires. These performances are greatly influenced by many factors including the VCO, loop filter and N divider value.

## 2. PLL Frequency Synthesizer Design

A Phase Locked Loop (PLL) is a feedback control system. It compares the phases of two input signals and produces an error signal that is proportional to the difference between their phases. The error signal is then low pass filtered and used to

drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the phase error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is locked to the frequency at the other input. This other input is called the reference and is usually derived from a crystal oscillator, which is very stable in frequency. Figure 1 shows the basic elements of a PLL-based frequency synthesizer. It consists of a high-stability crystal oscillator, phase detector, charge pump, low pass filter (LPF), voltage-controlled oscillator (VCO), and programmable frequency dividers. Integer-N PLL frequency synthesizers divide the output frequency by an integer value [5],[6].

The PLL is a highly non-linear system [7]. However, it can be described with a linear model if the loop is in lock. The loop is in lock when the phase error signal produced by the phase detector settles on a constant value. This implies that the output signal has the same frequency as the input reference signal. A phase difference between the reference and output signal may exist depending on the type of PLL used. However, this phase difference remains constant while the loop is in lock. If the PLL is used as a frequency synthesizer, the output signal will have a frequency N times the reference frequency.

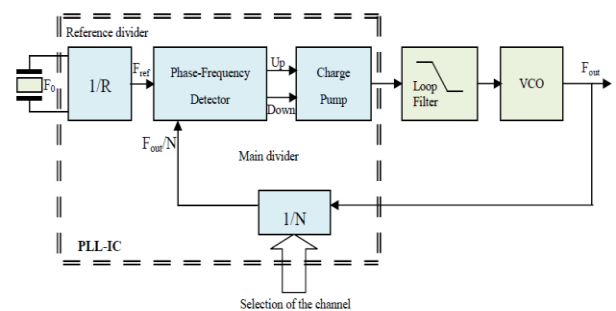


Fig 1: Block diagram of the designed frequency synthesizer

## 3. Loop Filter

The loop filter is a low pass filter that is often implemented with discrete components. Compared to an active filter, a passive filter is desirable for its simplicity, low cost and phase noise performance. The loop filter design is the most critical part of the whole synthesized oscillator development. The outputs of the phase detector are associated in a single signal by the charge pump. This resulting signal is then applied to a low-pass filter in order that the output voltage of the phase detector does not vary too quickly. In the loop, a low-pass filter (LPF) is present so as to suppress spurs produced in the

phase detector so that they do not cause unacceptable frequency modulation in the VCO. The circuit in Figure 2 shows a third order passive loop filter configuration.

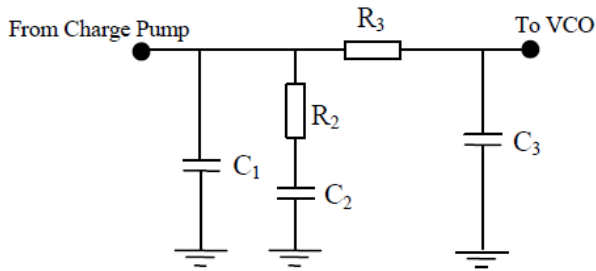


Fig 2: Loop filter circuit

The transfer function of the loop filter in figure 2 is given by

$$Z_{fil3} = \frac{Z(s) \left( \frac{1}{C_3 \cdot s} \right)}{Z(s) + R_3 + \left( \frac{1}{C_3 \cdot s} \right)} \quad (1)$$

Where  $Z(s)$  describes the transfer function of the second order loop filter given by

$$Z(s) = \frac{s \cdot C_2 \cdot R_2 + 1}{s^2 \cdot C_1 \cdot C_2 \cdot R_2 + s \cdot C_1 + s \cdot C_2} \quad (2)$$

The loop bandwidth is the most critical system design parameter for the PLL. The loop bandwidth is determined by many factors, including the loop filter, which is usually

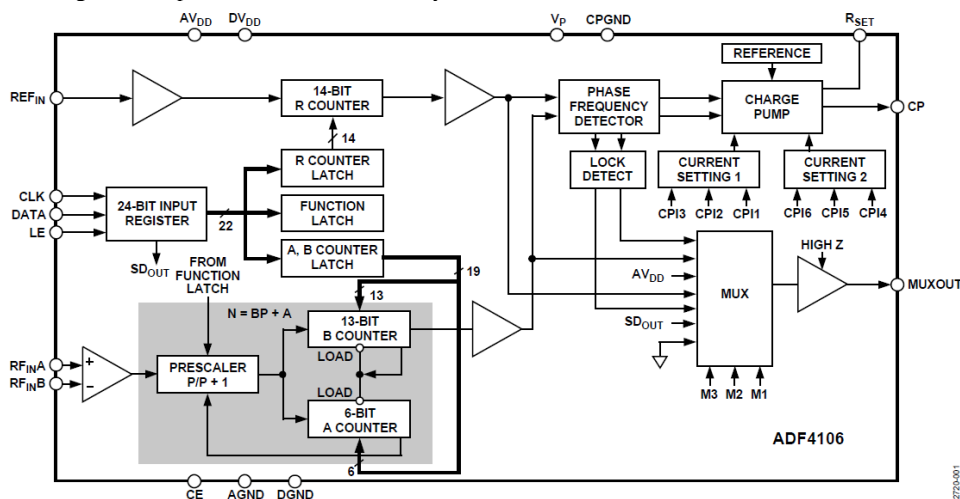


Fig 3: Functional block diagram of the ADF4106

#### 4.1 Frequency Domain Analysis of PLL

For a frequency synthesizer  $F_{out}=2.4$  GHz, the most important parameters to achieve the design are as follows:

- Channel Spacing:  $F_{ref} = 1$  MHz.
- Reference Oscillator Frequency:  $F_o = 10$  MHz.
- The gain of the VCO:  $K_{VCO} = 160$  MHz/V.

external to the PLL chip. The user therefore chooses a loop bandwidth and designs for this parameter. The classical design trade-off in PLLs is lock time vs. spurs. If one designs for a narrow loop bandwidth, the spur levels look much better, but the lock time is degraded. If one increases the loop bandwidth, lock time can be improved at the cost of spur levels. Consequently we note that at the time when a problem is solved, another is created. This is why the choice of the loop filter remains a great interest of the microwave circuits' designers.

#### 4. Results and Discussions

A good example of a PLL Frequency Synthesizer application is a Bluetooth transceiver. Bluetooth is a wireless technology standard for exchanging data over short distances (using short-wavelength radio transmissions in the ISM band from 2400–2480 MHz) from fixed and mobile devices, creating personal area networks (PANs) with high levels of security. The frequency synthesizer used to generate and to control a very stable signal with a low noise in the frequencies range is ADF4106.

The ADF4106 from Analog Devices ([www.analog.com](http://www.analog.com)) frequency synthesizer presented on figure 3 can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters [8]. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A counter and B counter, and a dual-modulus prescaler ( $P/P + 1$ ). The A (6-bit) counter and B (13-bit) counter, in conjunction with the dual-modulus prescaler ( $P/P + 1$ ), implement an N divider ( $N = BP + A$ ). In addition, the 14-bit reference counter (R Counter) allows selectable REF\_IN frequencies at the PFD input [8],[9].

ADIsimPLL enables the rapid and reliable evaluation of new high performance PLL products from Analog Devices, Inc. It is the most comprehensive PLL Synthesizer design and simulation tool available today.

- Gain of the charge pump:  $K_{CP} = 5 \text{ mA} / 2 \cdot \pi \text{ rad}$ .
- Main divider:  $N = \frac{2400 \text{ MHz}}{1 \text{ MHz}} = 2400$ .
- Reference divider:  $R = \frac{10 \text{ MHz}}{1 \text{ MHz}} = 10$ .

- Phase Margin:  $\Phi=55^\circ$ .

In a loop bandwidth of 100 KHz, and a phase margin of  $55^\circ$ , the component values of the third order loop filter are  $C_1=135$  pF,  $C_2=3.05$  nF,  $R_2=2$  K $\Omega$ ,  $R_3=7.76$  K $\Omega$  et  $C_3=33.3$  pF. Figure 4 shows the open-loop gain and phase transfer functions for the PLL design, whereas Figure 5 shows the closed-loop gain transfer functions. It can be seen from Figure 5 that the gain drops to 1 (0 dB) at the specified Loop bandwidth frequency (100 kHz) and the phase is at its peak of about  $-125^\circ$  which corresponds to a phase margin of  $55^\circ$  ( $180^\circ-125^\circ$ ). In the loop bandwidth of the synthesizer, the transfer function of the closed loop is very large in amplitude (Figure 5), thus causing an increased noise level of reference oscillator. This gain is constant until it reaches the loop bandwidth, then it drops rapidly. This function represents also the gain of noise in the bandwidth and the attenuation of this noise above this frequency.

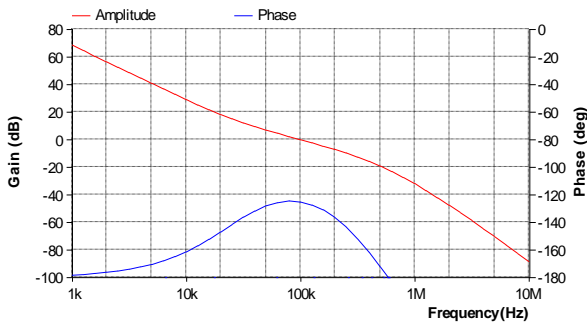


Fig 4: Open-loop gain transfer function

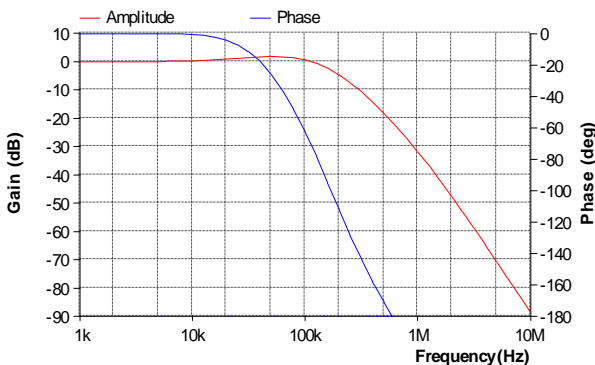


Fig 5: Closed-loop gain transfer function

Figure 6 illustrates the phase noise in each component (reference oscillator, phase detector, loop filter and VCO), the chip and the total phase noise. The results show that inside the loop bandwidth, the noise level of the reference oscillator is more significant owing to the fact that the gain of the closed loop transfer function is high in this band and it falls quickly outside. Figure 7 shows the frequency modulation response that is applied to the VCO whilst locked in the PLL. This is a high-pass response as within the loop bandwidth the PLL will try to remove the modulation. This response demonstrates that the noise of the VCO is high pass filtered by the PLL, providing rejection of the phase noise or phase error within the bandwidth.

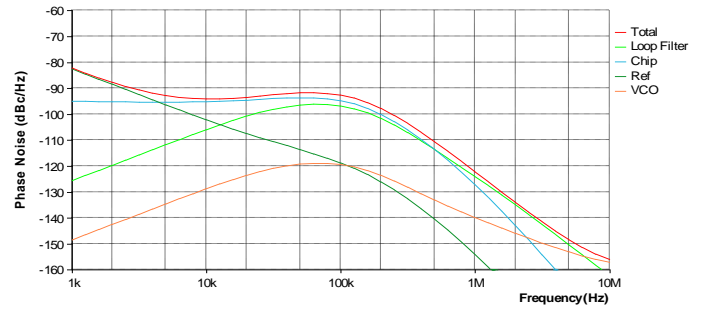


Fig 6: Phase noise for each of the potential noise components in the PLL synthesizer

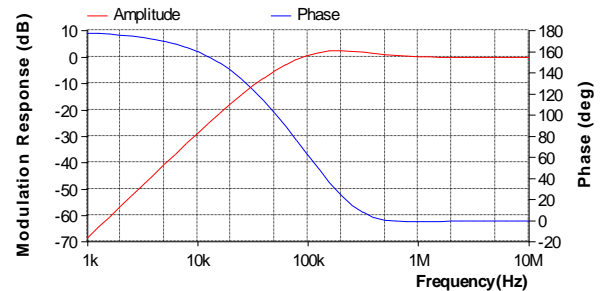


Fig 7: Frequency modulation response

Figure 8 shows the reference spurs generated by leakage at the phase detector. The charge pump leakage current introduced in the simulation is 1nA. The results obtained indicate first three spurs of  $-82$  dBc/Hz,  $-98$  dBc/Hz and  $-108$  dBc/Hz at 1MHz, 2MHz and 3MHz respectively. Concerning Phase jitter from 10 kHz to 100 kHz, the obtained RMS phase Jitter is 0.60 degrees.

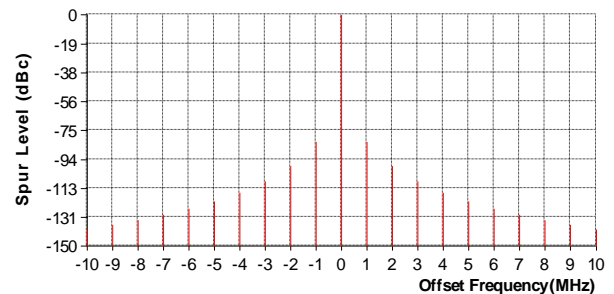


Fig 8: Reference spurs

## 4.2 Transient Analysis of PLL

In modern telecommunications systems, the synthesizer often has strict requirements for settling time, defined as the time that it takes the PLL to switch between two different frequencies. This time is measured from the start of the frequency switching action to the time of the new frequency settles within a specified accuracy. When the PLL switches between two different frequencies, the chip can neither transmit nor receive any data until the frequency offset error is acceptable. In turn, this reduces the effective data rate that the system can achieve. While the PLL lock time is mainly dependent on the loop bandwidth (the lock time is always inversely proportional to the loop bandwidth), it also depends on the size of the frequency jump during the PLL switching [5]. Figure 9 shows the PLL's transient response. This

analysis of the evolution of the instantaneous frequency of the VCO output versus time for a frequency jump of 80 MHz follows an adequate design of the loop filter. As expected, the switching time predicted following a transient simulation is about 50.83  $\mu$ S. This value is adequate for a 2.4 GHz standard in the case where the user equipment (UE) is mobile and changing location.

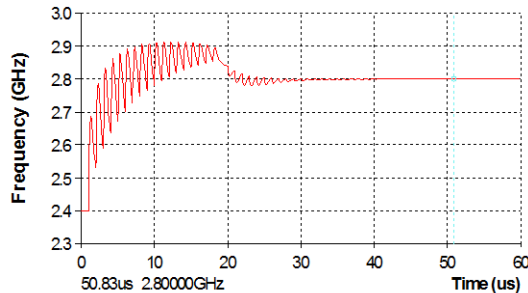


Fig 9: Transient response of the PLL

## 5. Conclusion

The simulation and the design of 2.4 GHz Integer-N Frequency Synthesizer with 1 MHz frequency step operating in the ISM band from [2400–2480] MHz are presented in this paper. The phase noise analysis of each component constituting the frequency synthesizer and their effects on its RF output is presented. Moreover, an accurate transient analysis of the PLL system is presented. The obtained output spectrum presents a noise density of -82 dBc/Hz at 1MHz offset, a switching time for a frequency jump of 80 MHz is about 50.83 $\mu$ S and an RMS phase Jitter of 0.60 degrees. These performances confirm and justify the use of such circuits in wireless ISM band communication system.

## 6. REFERENCES

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