Digitally Programmable Floating Impedance Converter using CMOS-DVCC

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ABSTRACT
A novel digitally programmable floating impedance converter circuit is realized using two CMOS digitally programmable differential voltage current conveyors and three grounded passive elements. The realized impedance converter can provide digitally programmable floating impedances like ideal floating resistor, capacitor, inductor and frequency dependent negative resistor through appropriate selection of three grounded passive elements without any component matching constraint. The realized digitally programmable floating impedance converter is designed and verified using PSPICE and the results thus obtained justify the theory.

Keywords
Current conveyors, DVCC, impedance converter.

1. INTRODUCTION
For over last two decades the current conveyors have been dominating in the area of analog signal processing due to their functional versatility in addition to higher signal bandwidth and greater linearity. As a result vast variety of linear and nonlinear analog signal processing applications are reported in technical literature [1-34]. Recently, the introduction of digital control to the current conveyor (CCII) has eased the on chip control of continuous time systems with high resolution capability and reconfigurability [15-26]. Such reconfigurable modules are suitable for realizing the field programmable analog array [22-24], [35-37].

In analog signal processing applications the component simulators play an important role and several component simulators are reported in technical literature employing current conveyors as well [27-34]. However, many of them use a complex circuitry and component matching constraints. The component matching constraints increase the system parameter sensitivity to the unacceptable level [34].

In this paper a novel digitally programmable floating impedance converter (DPFIC) is presented which uses two digitally programmable differential voltage current conveyors (DPDVCC) and three grounded passive components. The realized DPFIC can provide ideal floating resistor, capacitor, inductor and frequency dependent negative resistor (FDNR) through appropriate selection of three grounded passive elements without any component matching constraint. All the DPFIC based simulated floating components can be digitally controlled and possess low sensitivity. To verify the proposed theory the DPFIC is used to simulate the floating ideal inductor and floating ideal frequency dependent negative resistor (FDNR). The simulated ideal floating inductor and ideal floating FDNR, respectively have been used to realize the prototype second order low pass filter (LPF) and high pass filter (HPF). These the DPFIC based LPF and HPF are designed and verified using PSPICE and the results thus obtained justify the theory.

2. THE CMOS DPDVCC
The digitally programmable differential voltage current conveyor (DPDVCC) symbol is shown in "Figure 1(a)" and its CMOS implementation with 4-bit current summing network (CSN) at port-Z is shown in "Figure 1(b)". The transfer matrix of the DPDVCC can be expressed as

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & N^m & 0 & 0 \\ 0 & 0 & -N^m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

Thus the port voltages and currents for the DPDVCC can be expressed as

$$\begin{aligned} I_{Y1} &= I_{Y2} = 0 \\ V_X &= V_{Y1} - V_{Y2} \\ I_{Z+} &= +N^m I_X \\ I_{Z-} &= -N^m I_X \end{aligned} \quad (2)$$

where, N is an n-bit digital control word. The power integer 'm = 1' for current summing network (CSN) at port-Z and m = -1 for the CSN at port-X of the DPDVCC [20-26].

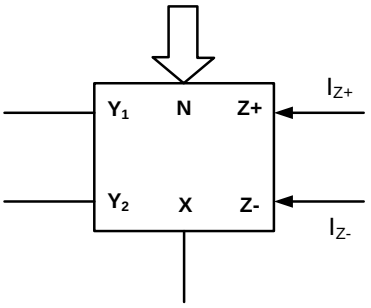

Fig 1(a): Symbol for DPDVCC

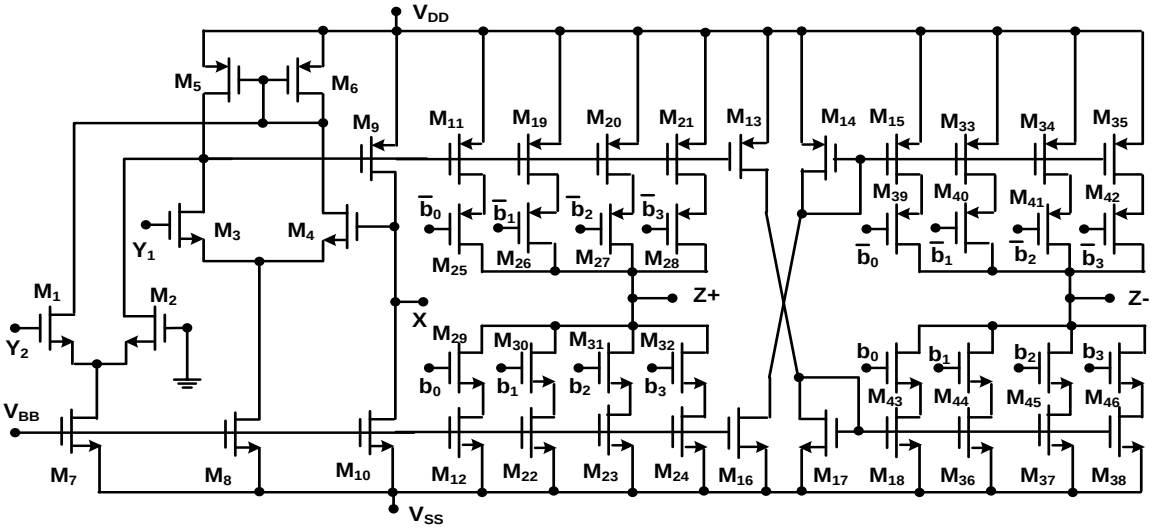

Fig 1(b): The CMOS implementation of a DPDVCC with 4-bit CSN at Z+ and Z- terminals

3. THE DPFIC CIRCUIT

The realized digitally programmable floating impedance converter (DPFIC) using DPDVCC of "Figure 1" with 'm=1', is given in "Figure 2".

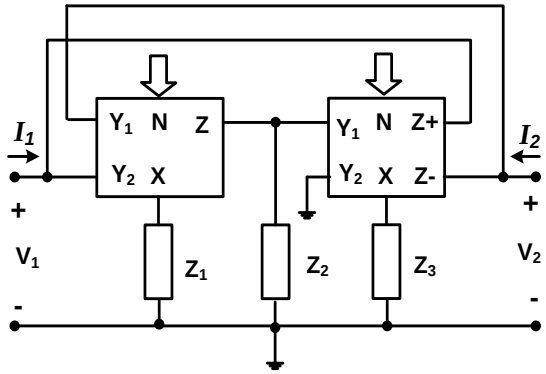

Fig 2: The DPFIC circuit

The routine analysis yields its admittance matrix as follows.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{N^2 Z_2}{Z_1 Z_3} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (3)$$

Thus the equivalent floating impedance Z_f can be expressed as

$$Z_f = \frac{Z_1 Z_3}{N^2 Z_2} \qquad (4)$$

The realized floating impedance given in equation (4) can result the following digitally programmable floating ideal element simulators through appropriate selection of three grounded impedances Z_1, Z_2 and Z_3.

(i) Digitally programmable ideal floating resistor (R):
If $Z_1=R_1$, $Z_2=R_2$ and $Z_3=R_3$, then $Z_f=(R_1R_3/R_2)N^2$, with $R = (R_1R_3/R_2)N^2$.

(ii) Digitally programmable ideal floating capacitor (C):
If $Z_1=1/sC_1$, $Z_2=R_2$ and $Z_3=R_3$, then $Z_f=1/s(C_1R_2/R_3)N^2$, with $C = (C_1R_2/R_3)N^2$.

(iii) Digitally programmable ideal floating inductor (L):
If $Z_1=R_1$, $Z_2=1/sC_2$ and $Z_3=R_3$, then $Z_f = s(R_1R_3C_2)/N^2$, with $L = (R_1R_3C_2)/N^2$.

(iv) Digitally programmable ideal floating FDNR (D):
If $Z_1=1/sC_1$, $Z_2=R_2$ and $Z_3=1/sC_3$, then $Z_f = 1/s^2(C_1C_3R_2)N^2$, with $D = (C_1C_3R_2)N^2$.

Thus, the realized DPFIC simulates the digitally programmable ideal floating resistor, capacitor, inductor and FDNR without any matching constraint. The incremental sensitivity measures of the above realized floating impedances with respect to various passive elements and the control word N, are analyzed and expressed as follows.

$$S^{Z_f}_{Z_1,Z_2,Z_3,N} = |1| \qquad (5)$$

From equation (5), it is evident that the incremental sensitivity measures of the realized floating impedance with respect to various passive elements are unity in magnitude [34].

Taking the tracking errors of the DPDVCC into account, the relationship of the terminal voltages and currents of the DPDVCC can be rewritten as

$$\begin{aligned} I_{Y1} &= I_{Y2} = 0 \\ V_X &= \beta(V_{Y1} - V_{Y2}) \\ I_{Z+} &= +\alpha N I_X \\ I_{Z-} &= -\alpha N I_X \end{aligned} \qquad (6)$$

where, β is the voltage transfer gain from Y to X terminal and α is the current transfer gain of the DVCC from X to Z terminal. The above transfer gains slightly deviate from unity and the deviations are quite small and technology dependent [13]. By including these non-ideal effects the DPDVCC the floating impedance given in equation (4) is modified as follows.

$$Z_f = \alpha\beta \frac{Z_1 Z_3}{N^2 Z_2} \qquad (7)$$

Thus, from equation (7) it is observed that the magnitude of the floating impedance Z_f may get slightly affected due to non idealities of the DPDVCC.

4. DESIGN AND VERIFICATION

The realized DPFIC of "Figure 2" was designed and verified by performing PSPICE simulation with supply voltage ± 2.5 V, using CMOS TSMC 0.25 µm technology parameters. The aspect ratios used are given in the Table 1. The DPFIC was used to design a digitally programmable ideal floating inductor (L) and FDNR (D), which were used in second order

Table 1: The aspect ratios of the MOSFETs of the DPCCII

MOSFETs	W µm	L µm
M_1, M_2, M_3, M_4	0.8	0.25
M_5, M_6	4	0.25
M_7, M_8,	14	0.25
M_9, M_{13}, M_{14}, M_{11}, M_{25}, M_{17}, M_{39}	25	0.25
M_{19}, M_{26}, M_{33}, M_{40}	50	0.25
M_{20}, M_{27}, M_{34}, M_{41}	100	0.25
M_{21}, M_{28}, M_{35}, M_{42}	200	0.25
M_{10}, M_{15}, M_{16}, M_{12}, M_{29}, M_{18}, M_{43}	10	0.25
M_{22}, M_{30}, M_{36}, M_{44}	20	0.25
M_{23}, M_{31}, M_{37}, M_{45}	40	0.25
M_{24}, M_{32}, M_{38}, M_{46}	80	0.25

low pass filter (LPF) and high pass filter (HPF), respectively as shown in "Figure 3(a)" and "Figure 4(a)". Thus the resulting DPFIC based LPF and HPF, are respectively shown in "Figure 3(b)" and "Figure 4(b)". The cutoff frequency (f_0) and pole-Q of the LPF with R_1=R_3=R and C_2=C_0=C, can be expressed as follows.

$$f_o = \frac{N}{2\pi RC} \qquad 8(a)$$

$$Q = \frac{R_0}{R} N \qquad 8(b)$$

Similarly, the cutoff frequency (f_0) and pole-Q of the HPF with C_1=C_3=C and R_2=R_0=R, can be expressed as follows.

$$f_o = \frac{1}{2\pi RCN} \qquad 9(a)$$

$$Q = \frac{C}{C_0} N \qquad 9(b)$$

Thus from equation (8) and (9) it is evident that the cutoff frequency f_0 of the LPF is directly proportional to the digital control word N while for HPF it is inversely proportional to N. It is to be noted that with N the pole-Q also increases in both the cases which can be readjusted with resistor R_0 for LPF and with C_0 for HPF. Initially the LPF was designed for a cutoff frequency f_0 = 100KHz and Q = 0.707 at N=1. Using equation (8) the designed values were found as R_1=R_3=R= 37 KΩ, R_0=26.16KΩ, C_2=C_0=C= 0.043 nF. Then to control the cutoff frequency f_0, the digital control word N was changed to 2, 4, 8 and 15, and the pole-Q was readjusted to 0.707 through R_0. Thus the results observed are shown in "Figure 3(c).

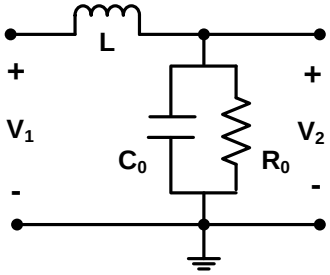

Fig 3(a): The prototype second order LPF

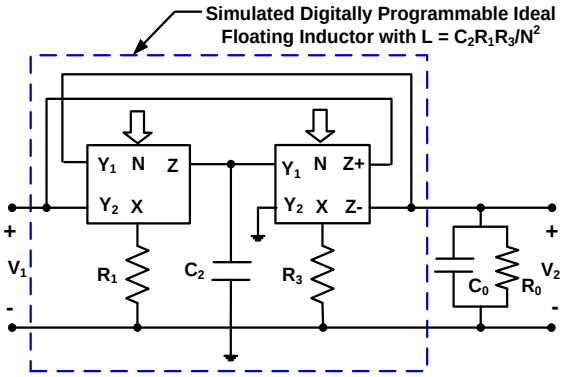

Fig 3(b): The DPFIC based second order LPF

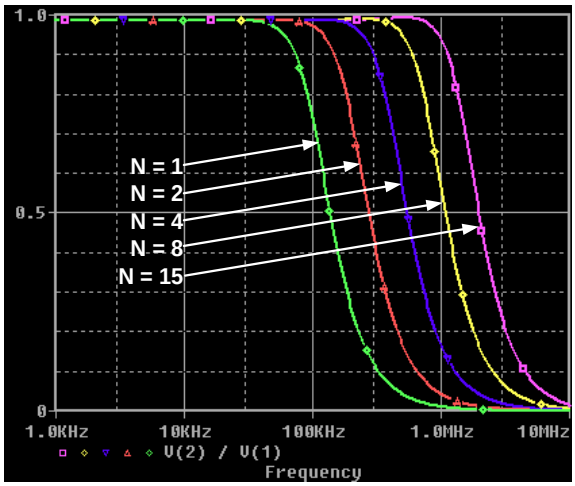

Fig 3(c): The frequency response of the LPF using Digitally controlled ideal floating inductor realized from DPFIC, at different control word N

Similarly, the DPFIC based HPF of "Figure 4(b) was also designed for a cutoff frequency f_0 = 100 KHz and Q = 0.707 at N=1. Using equation (9) the designed values were found as C_1=C_3=C= 0.043 nF, R_2=R_0=R= 37 KΩ, C_0= 0.0608 nF. Then to control the cutoff frequency f_0, the digital control word N was changed to 2, 4, 8 and 15, and the pole-Q was readjusted to 0.707 through C_0. The results observed for HPF are shown

in "Figure 4(c). Thus the observed results of "Figure 3(c) and "Figure 4(c)", show the close conformity with the theory.

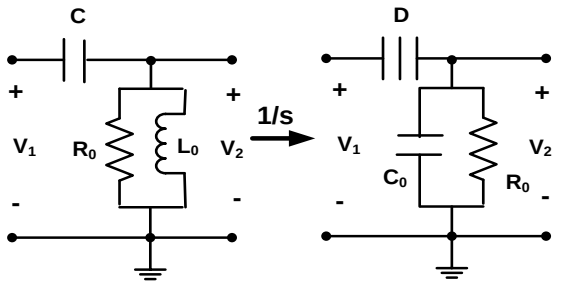

Fig 4(a): The prototype second order HPF and its 1/s transformed version

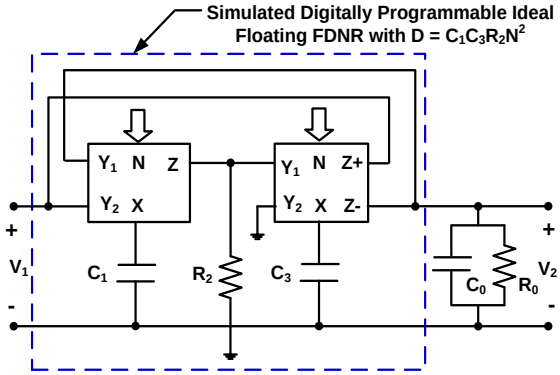

Fig 4(b): The DPFIC based second order HPF

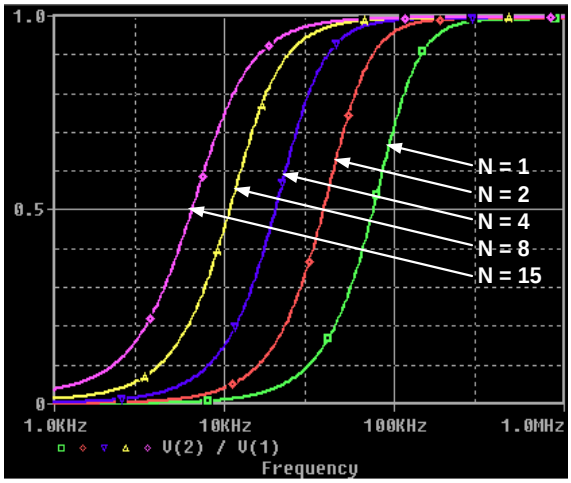

Fig 4(c): The frequency response of the HPF using Digitally controlled ideal floating FDNR realized from DPFIC, at different control word N

5. COMPARATIVE STUDY

The digitally programmable floating impedance converter presented in this paper, is compared with some other floating impedance converters available in recent technical literature and the comparative results are given in Table 2. It is observed from the Table 2 that DPFIC presented here, enjoys the additional feature of digital programmability and reconfigurability along with the low sensitivity, over the other floating impedance converters.

Table 2: The comparative results

Ref. No.	No. of Active Devices	No. of Passive Elements	Passive Elements Matching	Digital Control
[30] Fig 3(a)	3 CCII	3	No	No
[30] Fig 3(b-d)	2 CCII	5	No	No
[33] Fig 4	2 DDCC	3	Yes	No
[34] Fig 1	2 CFOA	5	Yes	No
Proposed DPFIC Fig 2	2 DPDVCC	3	No	Yes

6. CONCLUSION

A novel digitally programmable floating impedance converter is presented which uses two digitally programmable differential voltage current conveyors and three grounded passive components. The realized digitally programmable floating impedance converter provides ideal floating resistor, capacitor, inductor and frequency dependent negative resistor through appropriate selection of three grounded passive elements without any component matching constraint. All the digitally programmable floating impedance converter based simulated ideal floating components are digitally programmable and possess low sensitivity figures. These reconfigurable modules are suitable for realizing the field programmable analog array. To verify the proposed theory the digitally programmable floating impedance converter is used to simulate the floating ideal inductor and floating ideal frequency dependent negative resistor. The simulated ideal floating inductor and ideal floating frequency dependent negative resistor, respectively have been used to realize the prototype second order low pass filter and high pass filter. The digitally programmable floating impedance converter based low pass and high pass filters were designed and verified using PSPICE and the results thus obtained justify the theory.

7. REFERENCES

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