Self-Buffer Management for Effective Utilization of Memory Power Consumption for Wireless Sensor Networks

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ABSTRACT
Self-Configuration is the core capability that supports Self management in Autonomic computing. An Autonomic computing promises to solve hardware and software evolution problems in wireless sensor networks (WSNs). In case of WSNs the consumption of memory is limited and hence the research focus is to maximize the performance, to improve the Quality of Service (QoS).The basic sensor node architecture in a wireless sensor network consists of sensing unit, transceiver unit, processing unit and memory unit along with the power supply module. Due to the basic nature of the sensor network applications being surveillance, there is a possibility that these networks will be deployed in a remote environment without human intervention. Also the sensor nodes are battery powered tiny devices with limited memory capacity. Because of these limitations of the sensor nodes, in order to self configure the memory for efficient utilization of energy during memory accesses, the architecture can be modified by dividing the memory into multiple banks and including a self-Configurable memory switching controller unit along with a power switching module. This modification will result in energy conservation so that power can be supplied only to the bank or part of the memory being accessed instead of powering the entire memory module thus leading to efficient energy consumption. This leads to increase in node and network life time.

General Terms
System Architecture –Algorithm, Quality of service (QoS)

Keywords
Self-Configure, memory-switch, energy consumption and Queue Model

1. INTRODUCTION
Currently, many WSNs have self-configuration features at protocol and hardware level [8][12] which are used to detect anomalies in network and adjust performance for certain tasks. Wireless sensor networks (WSN's) are becoming popular in military and civilian applications such as surveillance, monitoring, disaster recovery, home automation and many others. Almost any sensor network application requires some form of self-configuration and autonomic functionality. These networks are comprised of sensor nodes where each sensor node consists of sensing unit, transceiver unit, processing unit and memory unit as shown in figure 1. The limited memory capability and energy utilization nature of the sensor nodes has compelled many researchers to dig deep into this area. Usually, the memory architecture of a sensor node is made up of RAM with less memory capacity, which is used to store programs for processing (32 KB – 128 KB). Modern flash-based micro-controllers contain between 1KB and 512 KB of memory for program storage. This can be used as both program memory and for temporary data storage.

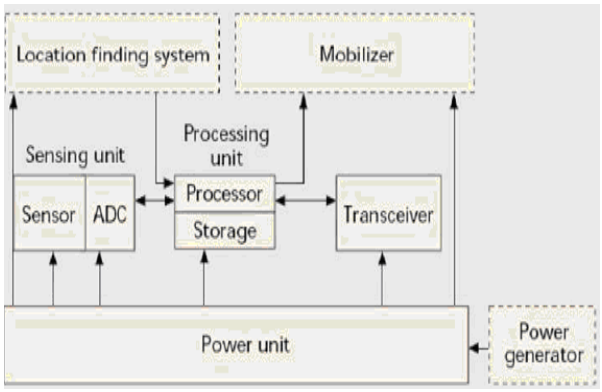

Figure 1. A typical Wireless Sensor Node (Ref [11])

Design of flash memory influences the life span of the sensor node. Recently, flash memory has become a popular alternative storage for many portable devices. Construction of memory architecture in a wireless sensor network depends on the application type. In addition, the size of traffic data also varies from small to large based on the application. For instance, transmitting scalar data, such as temperature, humidity or pressure resort to smaller traffic size over the WSN; while transmitting captured images, videos, audio [9] [13] etc. require sending more amount of information over the WSN. When the sensor nodes are deployed for a specific application within the network and are switched on, power is also supplied to the memory unit attached to the nodes even if the sensors are idle. The energy consumed in this state is known as idle energy since the sensor is not performing any useful operation. Hence, there is a need for modifying the architecture at the sensor nodes by incorporating efficient memory or buffer management schemes.

2. RELATED WORK

One of the components of wireless sensor node is the power source which can be battery. The wireless sensor node is a microelectronic device which can only be equipped with a limited power source [6] [9]. Over the remote inaccessible place with less human control and existence, power source play critical role in the survival of sensor nodes. Power source should be intelligently divided over sensing, computation and communication stages as per requirement. Sensors can hibernate when inactive. Lot of current researchers are focusing on power-aware protocols and algorithms for wireless sensor networks. Following section gives an insight into the work carried out in this direction.

The paper titled "Reducing Power Consumption for Mobile Multimedia Handsets" by authors Rong-Jaye Chen, Ting-Yu Lin, and Yi-Bing Lin [1] proposes 3 techniques called as wake up techniques which reduce the battery power consumption in a mobile multimedia handset. Using these approaches the system is switched into the sleep mode when the memory queue for the packet arrivals is empty. Various wake-up mechanisms are considered based on these concepts. First one among the 3 approaches is the threshold approach mechanism. Here, depending on the number of packets which have arrived in the memory queue, if it is above a threshold, the system is switched on else it remains in the sleep mode. The second approach known as vacation approach switches on the system, on completion of the vacation time. The third approach called the hybrid approach combines the above two approaches. In this approach the system is turned on when either the length of the memory queue goes above the threshold level or at the end of vacation time. A comparative study of these approaches sheds light on some of the important system performance parameters. For eg., it is seen that the threshold approach comes with reduction in the switch-on rate of the system whereas the vacation approach has the lowest mean packet waiting time. In order to maintain lower value for both the system switch-on rate and the mean packet waiting time, the hybrid approach needs to be selected. It is indicated that there is a possibility to obtain a set of threshold values in order to determine a small switch-on rate and the probability for packet dropping in case of threshold approach while such a possibility does not exists for vacation approach to obtain the range of vacation time.

The authors Tie Qiu, Lin Feng, Feng Xia, Guowei Wu, and Yu Zhou have [2] published a paper titled "A Packet Buffer Evaluation Method Exploiting Queuing Theory for Wireless Sensor Networks". They have focused on optimizing the performance of a large-scale wireless sensor networks for improved transmission QoS when the hardware consumption is limited. This paper proposes a novel evaluation scheme based on packet buffer capacity of nodes using queuing network model. Here the packet buffer capacity parameter of the queue is analyzed for each node type when it is in the best working condition. This method expands the queuing network model into the equivalent queuing network model by adding holding nodes to the existing network for evaluating the congestion condition within the queuing network, and to obtain effective arrival and transmission rates. This work establishes an M/M/1/N type open queuing network model with holding nodes for WSNs and includes designing of approximate iterative algorithms to calculate arrival rates when the system reaches a steady state. Experimental results indicate that the model is consistent with the real world data. This paper discusses modeling for only a single-server model in WSN and proposes a method for calculating the packet buffer capacity size of nodes. Recent research focus is on the convergence of multiple processor nodes that can be used for M/M/m/N queues, which are also multi-server queues. In addition, for large-scale WSNs, if the clusters are prioritized then it will effectively improve the performance of WSNs which will be the follow-up research.

In the paper with title, "Fundamental Lower Bound for Node Buffer Size in Intermittently connected Wireless Networks", the authors have [3] carried out an analysis on the fundamental lower bound for node buffer size in intermittently connected wireless networks. Due to some external constraints there is a possibility of occurrence of node inactivity which is the main cause for intermittent connectivity of the network. It is found that in a static random network, each node keeps a constant message generation rate. In such networks, the buffer occupation in each node does not approach zero in spite of having infinite network capacity and node processing speed. An in detail analysis has been done on buffer occupation when the channel capacity is infinite, and the results can be viewed as a lower bound for networks with finite channel capacity. The analysis show that when the probability of node inactivity is below the critical value, the state of the network is supercritical and the fundamental achievable lower bound of node buffer size is $\Theta(1)$, i.e. the minimum node buffer size requirements are asymptotically independent of the size of the network and when the probability of node inactivity is greater than the critical value, the network state is subcritical, and the achievable lower bound on node buffer size shoots up as the network expands, with the order of $\Theta(\sqrt{n})$.

The paper, "Limiting the Power Consumption of Main Memory" focuses[4] on the aspect of peak power consumption by the hardware components. This affects the power supply, packaging and the cooling requirements of the systems hardware equipments. Higher peak power consumption by the hardware leads to bulky and expensive systems. If ever the components and systems actually require peak power, then it becomes necessary to put a limit on power consumption to a less-than-peak power budget. This in turn will lead to intelligent provisioning of the power supplies, packaging and cooling infrastructures of the hardware components. This paper deals with the study of dynamic approaches to limit the power consumption by the main memories. It proposes 4 techniques namely Knapsack, LRU-Greedy, LRU-Smooth, and LRU-Ordered in which the power states of the memory devices are adjusted as a function of load on the memory subsystem. The simulations carried out from 3 benchmark applications prove that these techniques are

consistent in limiting the power to a pre-established budget accompanied by very low performance degradation. The simulation results indicate that the performance of limiting power using these techniques is same as that of the energy conservation approach used in state-of-the-art techniques exclusively designed for performance-aware energy management. Limitations of this work include addressing the issues related to selection of ideal power budget in case of different scenarios and studying the effect of greater concurrency in memory accesses in the context of chip multiprocessors in future.

Han-Lin Li, Chia-Lin Yang, and Hung-Wei Tseng [5] have presented a paper titled "Energy-Aware Flash Memory Management in Virtual Memory System", which revisits the design of virtual memory system using flash memory for many portable devices due to its improvements in storage capacity, reliability and lower power consumption [10] along with its limitations. This paper in particular, concentrates on the energy efficient aspect as power is the first-order design consideration for embedded systems. Frequent writes into the flash memory lead to frequent garbage collection thus incurring significant energy overhead. This is due to the write-once feature of the flash memory. In order to address this issue of increased energy consumption and to prevent excess energy lost, the authors have proposed 3 methods to reduce the number of writes occurring to the flash memory. They are Hot Cache scheme, Sub paging technique and Duplication-aware garbage collection method. In the Hot Cache scheme, an SRAM cache is introduced in order to buffer frequent writes. In the sub paging technique, the pages are partitioned into subunits and only dirty pages are written into the flash memory when page fault occurs. The duplication-aware garbage collection method makes use of data redundancy that exists between the flash memory and the main memory to bring reduction in the writes which occur due to garbage collection. Intrapage locality, a type of data locality, is an inherent feature of the flash memory and is responsible for data allocation. This property of the flash memory should be carefully preserved while data is written from the storage buffer to flash memory. Destruction of this property leads to increase in the energy consumption by the flash memory. Experiments have been carried out using the 3 techniques and the results show an average energy reduction of 42.2% using the combination of the 3 techniques.

3. PROPOSED WORK

3.1 Memory Bank Architecture for WSN

In the heterogeneous class of networks, wireless sensor networks form the lower level of the Internet networking hierarchy where energy utilization due to various factors is the main issue which affects the life span of the wireless sensor network and hence needs to be considered during the design of the network architecture. One such energy consuming factor is the memory access operations. Figure 2 shows the block diagram shows the modified sensor node along with Figure 3 modified memory architecture with switching power controller unit. Consider 128 KB flash memory which is equally divided into 4 blocks of 32 KB each and are known as memory banks. Hence the architecture also consist of a memory switching controller unit which will select the memory block and amount of memory needed by the sensor node based on the traffic flow. This leads to conservation of energy by the memory unit in the sensor node where only that part of memory which is currently in use is powered.

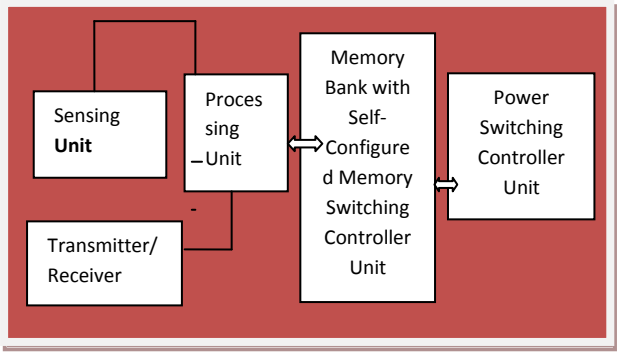

Figure 2. A typical modified Wireless Sensor node

Amount of traffic flow is application specific [8]. For example, let us consider the following cases:

Case I: Within the WSN, there are sensors which will sense data such as temperature, humidity, pressure, etc.. Such data require less storage.

Case II: WSN may also comprise of multimedia sensors, which capture multimedia information such as images, video or audio and process them. Processing of such data may include decision making which is done by the intelligent systems in the network. In such cases the multimedia information requires large amount of storage.

Hence, it is up to the sensor node to activate the number of memory banks required in the system based on the application for optimized energy utilization.

In most of the wireless sensor network applications, we will find variations in the traffic flow i.e. for some duration of the network operation the traffic flow is more while at some time the traffic flow is less. Thus an optimized way to achieve energy consumption is to divide the memory into a number of blocks and then use (power) only the part of the memory required for data storage.

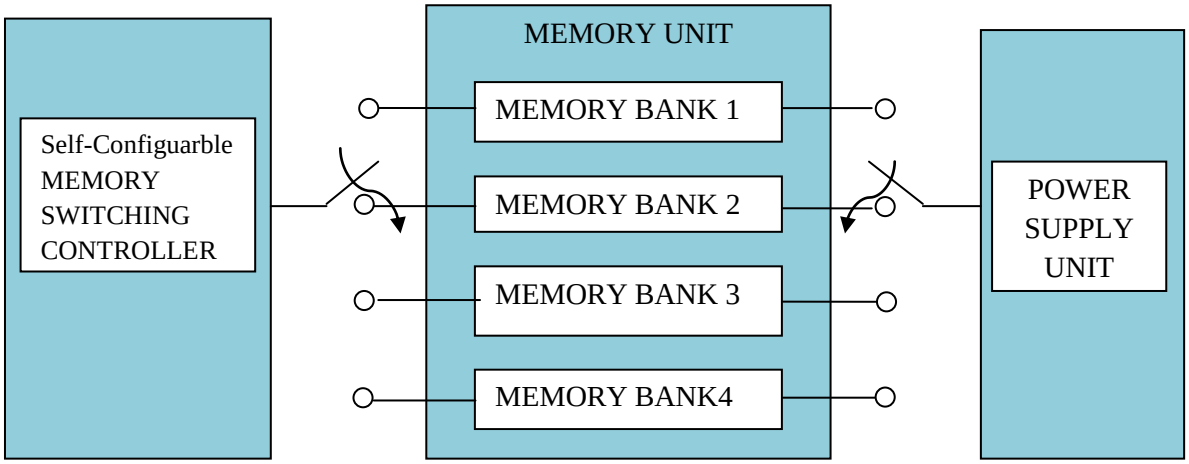

Figure 3. Block Diagram of Memory Bank Architecture of a Sensor Node

For example, let us say that amount of storage required for storing the data sensed by the node is only 20KB out of total flash memory size of 256KB. One approach is to consider the whole memory of 256KB as one block and use only 20KB. Though only 20KB of space is being utilized but the power is supplied to the entire 256KB memory. There is unnecessary wastage of excessive power in such a scenario which can be avoided. Another alternative is to consider the memory unit consisting of a switching controller unit and divide the 256KB memory into 8 banks each of 32KB and use only 1 memory bank to store 20KB of data i.e. power is supplied to only 1 memory bank by the switching controller unit and remaining 7 banks are switched off. Since less memory is being utilized, power required will also be less thus leading to the conservation in energy utilization by the memory unit in the sensor node. Power consumption in different scenarios is given as follows:

Normal Scenario 1: Power consumption in normal memory (P_{normal}) architecture is shown in Figure. 4 and is calculated with the formula as mentioned below.

$$\mathbf{P_{normal} = Energy\ Dissipation\ for\ usage\ space + Idle\ Energy}$$

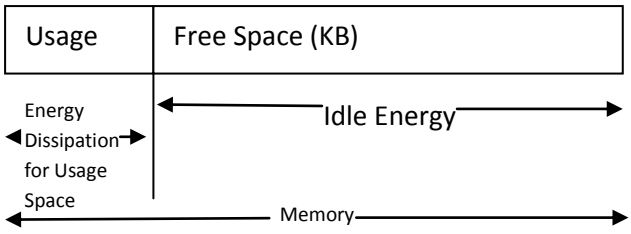

Figure 4. Energy Dissipation in normal memory architecture

Modified Scenario 2: Power consumption in modified memory ($P_{modified}$) architecture is shown in figure 5 and is calculated with the formula as mentioned below.

$$\mathbf{P_{modified} = \{Number\ of\ memory\ banks\} \times Energy\ dissipation}$$

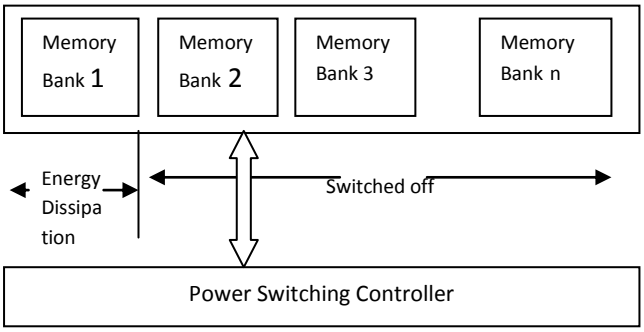

Figure 5. Energy dissipation in modified memory architecture

So, Figure 5, shows that the ideal energy dissipation can be minimized and lead to increase in the life time of the node.

3.2 System Model for Memory Architecture

The concept is simulated by considering simple queue system model, where packets arrive according to Poisson's model at rate λ, hence the interarrival times are independent of exponential random variable with mean 1/ λ. When a node is selected for data processing, a packet from the queue in that node is serviced. In an M/M/1 model, the packet distribution is Poisson with rate λ, or the interarrival time distribution is exponential with mean time 1/λ, similarly, the service rate distribution is also based on Poisson model with rate μ, or the service time distribution is exponential with mean time 1/μ. Interarrival and service time are independent variables. For example consider four packets, P1 through P4 arrive at random and require service time S1 through S4. Ea is the energy dissipation for receiving packet, Es is energy

dissipated during servicing the packet and Eq is energy dissipation when the packet is in queue as shown in figure 6

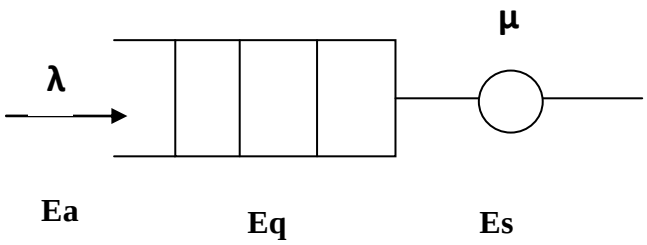

Figure 6. Queuing Model

Algorithm for modified memory architecture:

Input data:

P1, P2, P3….Pn : Arriving Packets

S1, S2, S3 ….Sn : Service Time for every Packet

Ea : Energy Dissipation for packet arrival

Es : Energy Dissipation for servicing the Packet

Eq : Energy dissipation for queuing or Storing in buffer

n : Number of memory banks in use

Step 1: Traffic is generated i.e. Inter arrival time and Service time is generated using random processes for all the incoming packets.

Step 2: if server is idle then

Packet is serviced

Else

Activate the Self-configured memory control unit to allocate the required memory bank for arriving packets and power switching controller unit to supply the power only to the allocated memory banks.

$$Total\ Energy\ Consuption = \mathbf{Ea} + \mathbf{n} * \mathbf{Eq} + \mathbf{Es}$$

Step 3: END

3.3. Simulation Environment

The M/M/1 queuing model is considered for generating the traffic flow at the sensor node. In this process the Inter arrival times and service times are generated randomly using Poisson distribution and the total energy consumption is calculated for every event occurring in the sensor node. The analysis has been carried out for varying interarrival time and service time.

3.4. Result Analysis

This section summarizes the results obtained from simulations. Table -I. lists the parameters and their corresponding values considered in the simulations.

Table I. Simulation Parameters:

Parameters	Value
Energy Threshold	200 Joules
Energy for receiving	0.057 Joules
Energy for Transmitting	0.033 Joules
Idle Queue Energy	0.00012 Joules
Interarrival time	1-7 secs
Service Time	1-7 secs
No of Packets	1000 Packets
QueueLength	100 packets

The graphs in Figures 7 to 9 are the plots of Service time (secs) on X-axis vs Energy Consumption (Joules) on Y-axis.

Case I: Interarrival time : 1 sec

Service time : 1-7 sec

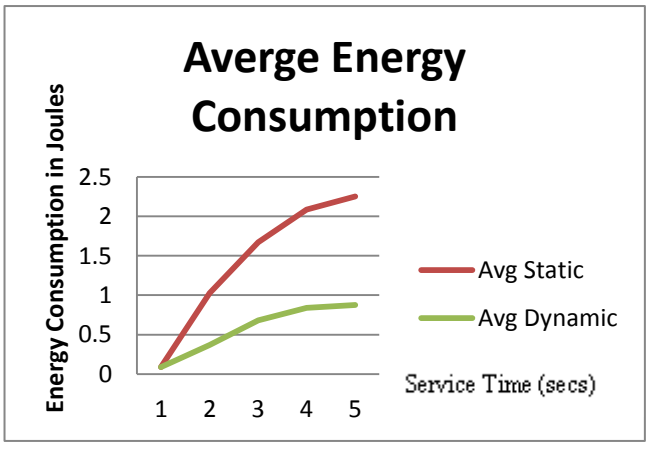

Figure 7. Comparison of average energy consumption by normal memory(static) with modified memory architecture (Dynamic)

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In figure 7, it is observed that at service time 1 sec, there is a deviation in the energy utilization curve in case of modified memory architecture (green curve) from the energy utilization curve obtained for the normal memory architecture (red curve) without the memory banks. The energy utilization by the modified architecture is significantly less as compared with the normal memory architecture.

Case II: Interarrival time : 1-2 sec

Service Time : 1-7 sec

In Figure 8, till service time 2 secs the energy utilization curve for both the architectures is almost the same. At 2 secs of the service time the deviation occurs i.e. the energy consumed during the memory operations in the normal memory architecture is much more than the modified memory architecture at the node.

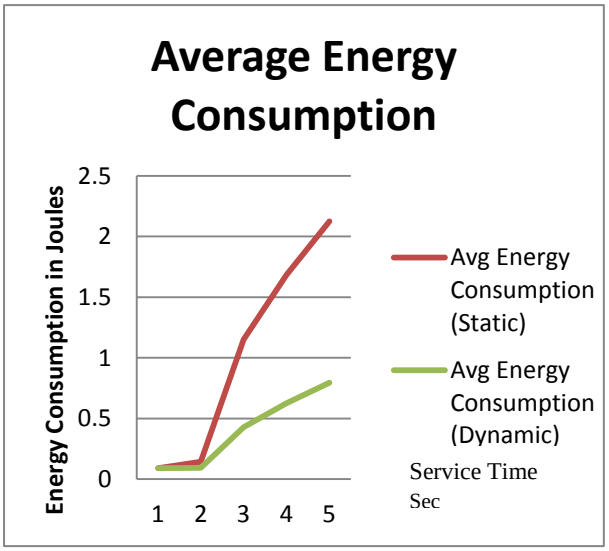

Figure 8. Comparison of average energy consumption by normal memory (static) with modified memory architecture Dynamic)

Case III: Interarrival time : 1-3 sec

Service time : 1-7 sec

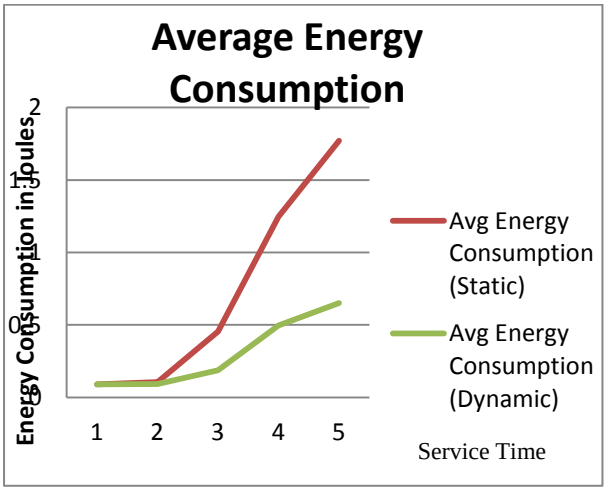

Figure 9. Comparison of average energy consumption by normal memory (static) with modified memory architecture Dynamic)

From Case-I to Case-III, it is seen that there is a deviation in the energy utilization curve for the modified memory architecture from the normal curve i.e. the energy consumed in the dynamic method is very less as compared to the original node memory architecture. During the simulations it is observed that this deviation occurs due to the reason that as more number of packets get queued up to be serviced, the modified memory architecture shows increase in performance as against the normal architecture of the sensor node by consuming less energy during memory operations, which leads to energy saving and thus increases the network lifetime.

4. Conclusion

The proposed work modifies the memory architecture at the sensor node. In this architecture the memory module is divided into a number of blocks known as memory banks which are activated by the memory controller unit and power switching module. Depending on the amount of traffic flow the memory banks are activated. Simulations have been carried out for varying interarrival and service times using M/M/1 queuing model. As observed from the graphs and during simulations, there is a small difference in the energy utilization at the initial stages when the number of packets in the queue is less and the service time is low. But as the number of packets getting queued up increases and even as the service time increases the modified memory energy architecture performs significantly better than the normal memory architecture. This results in the increase in node life time and in turn increases network lifetime

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