Adiabatic Split Level Charge Recovery Logic Circuit

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ABSTRACT
This paper describes the design and circuit simulation of split level charge recovery logic (SCRL). In conventional circuits the bits are thrown away for every transformation in the output level, And their associated energy becomes heat, which directly affects the cost of computation by increasing the system overhead required to get rid of the heat causing inconvenience of weight, short battery life etc. SCRL adiabatic logic promises to be an efficient technique to design low power digital VLSI circuit. The power efficiency of SCRL circuit is observed by comparing its performance with static CMOS inverter. A power efficient SCRL CLA is also designed and verified in this paper. Computer simulation using LTSPICE4 is carried out on SCRL circuit's implemented using CMOS technology.

General Terms
Performance, Design, Verify.

Keywords
Low power, adiabatic Logic.

1. INTRODUCTION
The vital trend of scaling in CMOS technology is the prime reason enabling today's design capable of performing very high speed computations. As MOSFET inherently supports scaling, the complexity and number of devices on a given IC is no longer an issue [12]. With the growing use of portable devices proficient of performing computations comparable to desktop computers, it has become necessary to explore new design methodologies that would consume less power and provide high throughput. The concern of low power is becoming imperative even in non-portable applications where power is available. Interest in low energy computing is growing as the cost of power dissipation become preposterous [8,9].

Adiabatic computing is exact approach in this view point. Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging [1]. The term adiabatic is derived from thermodynamics that describes a process in which there is no exchange of heat with the environment. Today's novel adiabatic logic approach also offers a means to recycle the energy from output nodes instead of wasting this energy by discharging it to ground [4,5,6]. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. As such every time a charge-discharge cycle occurs, an amount of energy equal to CV^2dd is dissipated. Unlike the conventional CMOS circuits, in adiabatic circuits energy is recycled [8]. Instead of discharging the capacitor to ground, the charge is discharged to the power supply. SCRL is a fully adiabatic technique, which does not have non adiabatic loss. This paper focuses on the concept and operation of SCRL. Also practical design considerations of implementing few basic gates are described. Some simulation results are also shown. Power comparison between CMOS logic circuit and SCRL circuit are performed.

2. BASIC SCRL OPERATIONS
The schematic of the SCRL inverter is illustrated in Fig 1. The SCRL inverter consists of a static CMOS inverter circuit with time varying supply followed by an additional transmission gate at the output [3].

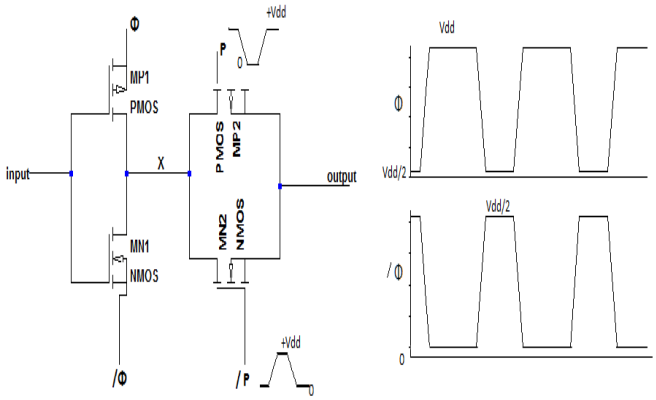

Fig 1. SCRL Inverter and Power clocks Input

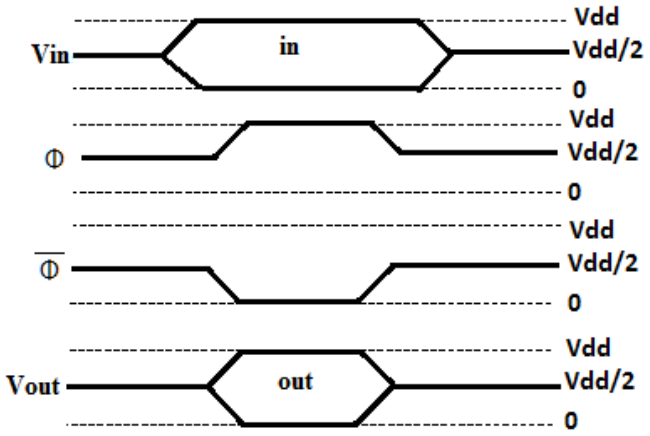

Fig 2. SCRL inverter output

The inverter is driven by two complementary power clocks Φ and / Φ rather than Vdd and ground terminals. Fig 1.clearly explains that the power clock input Φ varies between Vdd and Vdd/2 whereas /Φ varies between Vdd/2 and 0. Initially all the nodes (Φ and / Φ) are at Vdd/2, at that time the transmission gate is turned OFF by the clocks P and /P and the output is also at Vdd/2. After a valid input is applied the

transmission gate at the output is gradually turned ON by swinging P and /P to Vdd and ground respectively. Then clock Φ and / Φ swing to Vdd to ground respectively. If the input to the gate is Vdd then the node marked x and the output will follow / Φ and ground and if the input was at ground the node x and output follow Φ and Vdd [3].

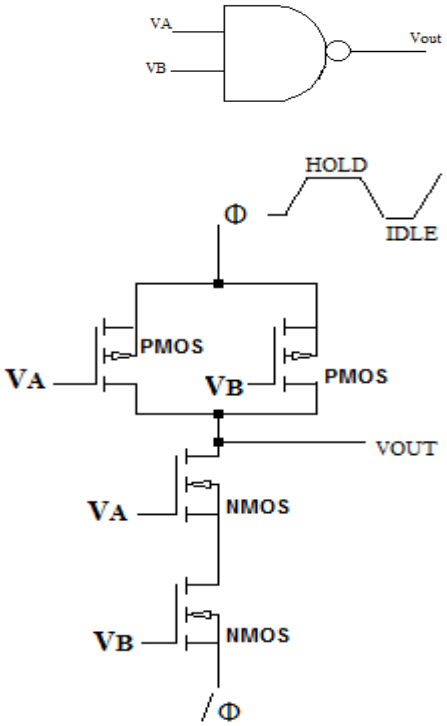

Fig 3 SCRL NAND gate

Fig 3 shows the symbol and schematic of a SCRL NAND gate. Although a static CMOS logic can be used for the same purpose, here power clocks is applied instead of Vdd and ground since the loading capacitance seen by clocks remain constant regardless of their input combinations, which is important for clock circuits.

3. CARRY LOOK-AHEAD ADDER

In a digital system an adder is a fundamental component, so the design of the adder is selected to show the effectiveness of the adiabatic logic family. Adiabatic logic computes only one logic level per phase, so it's difficult to put into operation a complex logic with a long chain of stages. Since a Ripple Carry Adder needs many phases to obtain a result, it's not practical with the adiabatic method [2]. A 32-bit ripple carry adder would need at least 32- phases to carry out one addition. To overcome the drawback of an adiabatic circuit, CLA structure is adopted in the design of SCRL adder.CLA not only reduces logic depth, but also offers a pipelined structure if buffers are added in the circuit.

Carry Look Ahead Adders is used to avoid linear growth of the carry delay. In CLA the carries can be generated in parallel. The Carry of each bit is generated from propagate and generate signals (Pi, Gi) as well as the input carry (Co).

$$G_i = A_i.B_i \quad (1)$$

$$P_i = A_i \oplus B_i \quad (2)$$

The carries from the four carry generator blocks are given by

$$C_1 = G_0 + P_0 C_0 \quad (3)$$

$$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0 \quad (4)$$

$$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \quad (5)$$

$$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0 \quad (6)$$

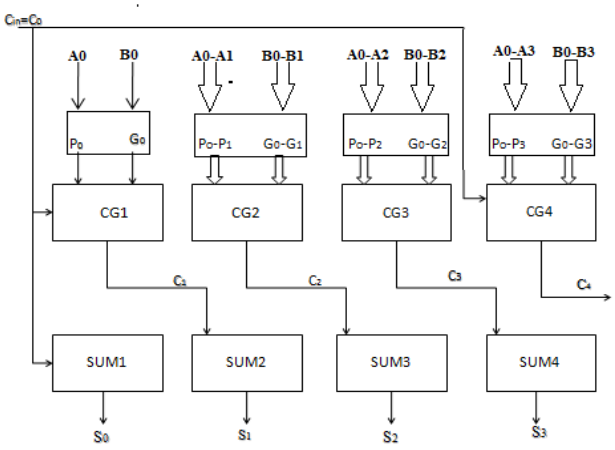

Fig 4 Block diagram of 4-bit Carry Look ahead Adder(CLA)

Fig 4 shows the block diagram of a 4 bit CLA adder. The carries C1 to C4 are generated in parallel from the four carry generator blocks (CG1-CG4) with the carry in signal C0 and propagate and generate signals serving as the inputs for the carry generator blocks[13]. The generate and propagate circuit is shown in Fig 5.

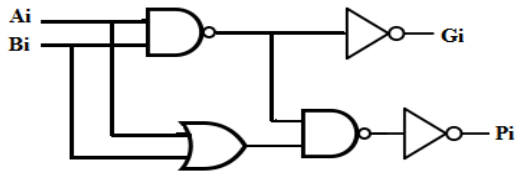

Fig 5 Generate and Propagate circuit

The Schematic 6 and 7 shows the static mirror circuit for four carry signals (C1 TO C4).

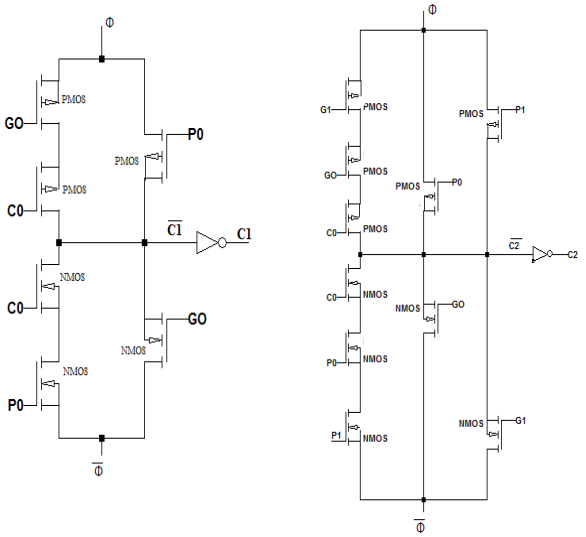

Fig 6 SCRL C1 and C2 carry generator circuit

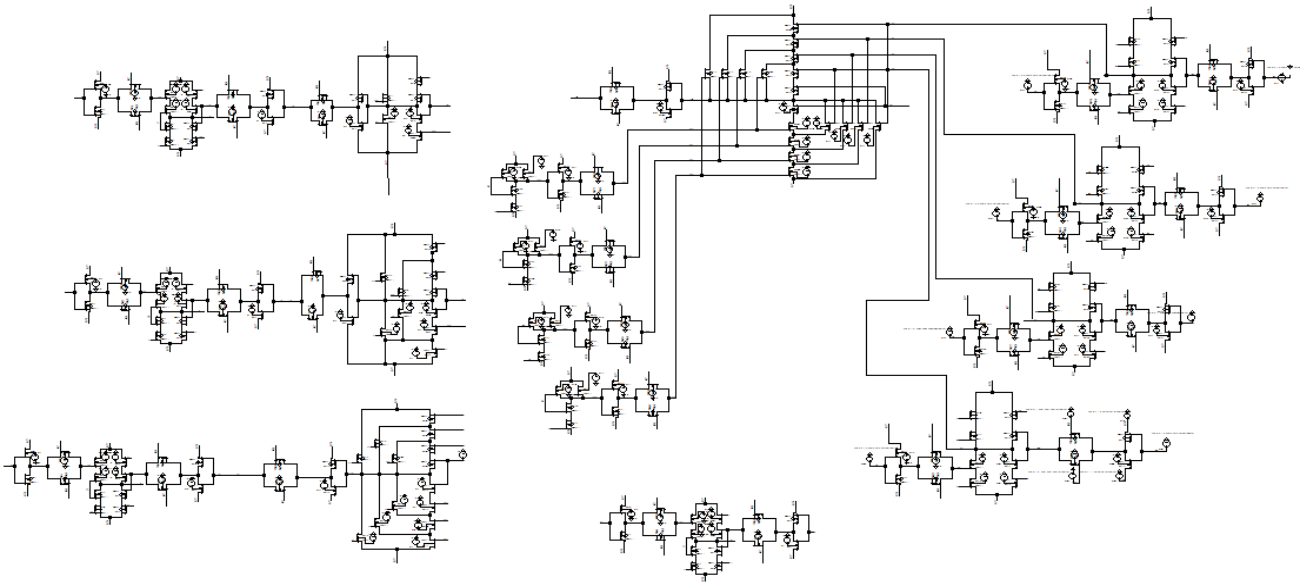

Fig 7 Four bit CLA simulation in LTSPICE

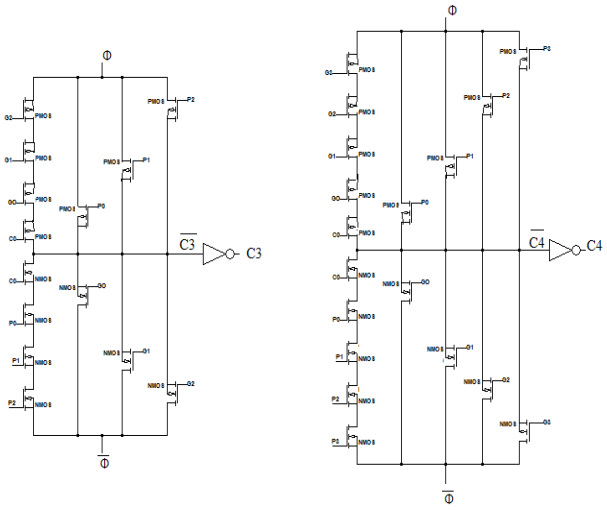

Fig 8 SCRL C3 and C4 carry generator circuit

Fig. 7 is the complete schematic of a 4- bit carry look ahead adder circuit. The generate and propagate signals are generated in parallel and are fed to all carry generators with the input carry signals C0. The carry signals are generated simultaneously [11].

4. ENERGY COMPARISION AND RESULTS

Energy comparison is an interesting concern in adiabatic logic design. The energy loss of a conventional fully static CMOS including the discharge power-dissipation term is

$$E_{CONV} = CV_{dd}^2$$

and the above equation is the basis of the analysis of simulation results. Operating frequency term is excluded in this expression, so the energy loss equation represents energy loss per cycle. When the pull-up network is turned on, capacitor C charges up to V_{DD} through the ON resistance of the switch. The current through the resistance decreases exponentially over time [12]. The energy dissipation is equal to $(1/2)CV_{DD}^2$.Where, $V_{DD}$is the voltage change at the node out. Similarly $(1/2)CV_{DD}^2$ amount of energy is dissipated when pull-down network is ON. Thus overall energy dissipated by static CMOS circuit is CV_{DD}^2. The transition at the output can be slowed down by using a time-varying voltage source instead of a static voltage supply. By spreading the transfer of charge to the capacitor over time, the current is greatly reduced [10]. If the current flow is maintained constant where T is total switching time, the total energy dissipation is reduced to $(RC/T)CV_{DD}^2$ .SCRL saves the energy by returning delivered energy back to the supply. The AC-power supply is needed to efficiently restore the charge, and thus it is required to design an efficient clock circuit which converts DC power to AC [7]. The SCRL inverter is already shown in Fig 1.and Fig 4.shows the basic static CMOS circuit. The energy CV_{DD}^2, which is consumed in the conventional CMOS circuits, is unavoidable since the charge is transferred from the supply and returned to the ground [10,12].

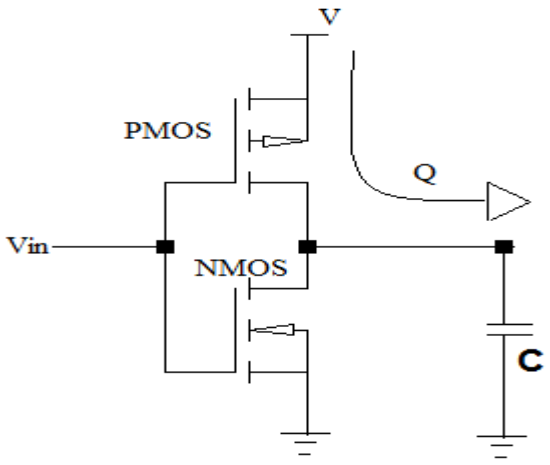

Fig.9 Static CMOS Inverter

The current drawn from the supply during a 0 → 1 transition is relatively large because of the large drain-source voltage. If,

however, the supply voltage can be varied in a manner that would reduce the drain current, the energy will be significantly reduced. This can be achieved by using adiabatic circuits. Comparison of power dissipation between SCRL inverter and CMOS inverter is shown in the Table 1.

Table 1. Summary of Power dissipation of SCRL inverter Operating at 100MHZ

Technology	Power Dissipation (watts)
conventional CMOS inverter	1252uW
SCRL Inverter	290uW
power gain of SCRL over conventional inverter	43%
conventional NAND gate	210uv
SCRL NAND gate	75uv
power gain of SCRL over conventional NAND gate	28%

4.1 Simulations

The CMOS inverter is tested by LTSPICE simulation using a standard CMOS technology.

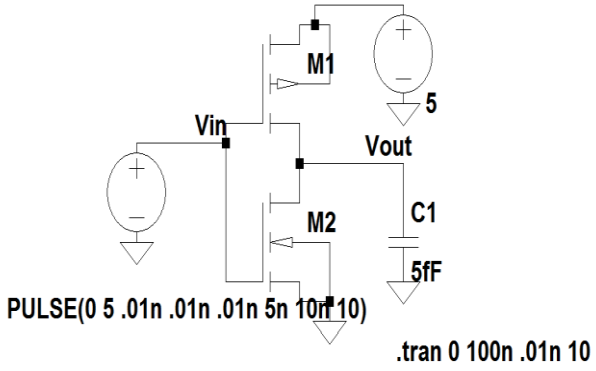

Fig 10 CMOS inverter simulation in LTSPICE

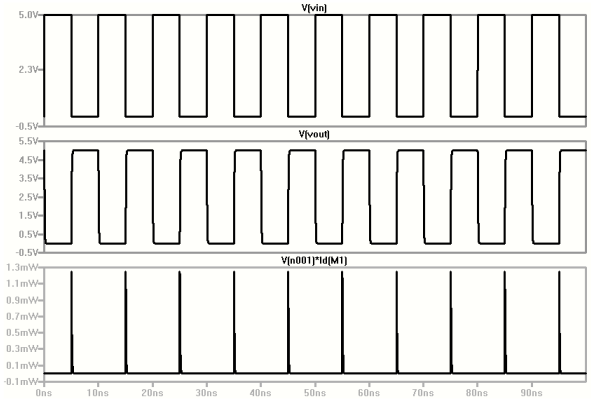

Fig 11 CMOS inverter Simulation power, input and Output waveform in LTSPICE

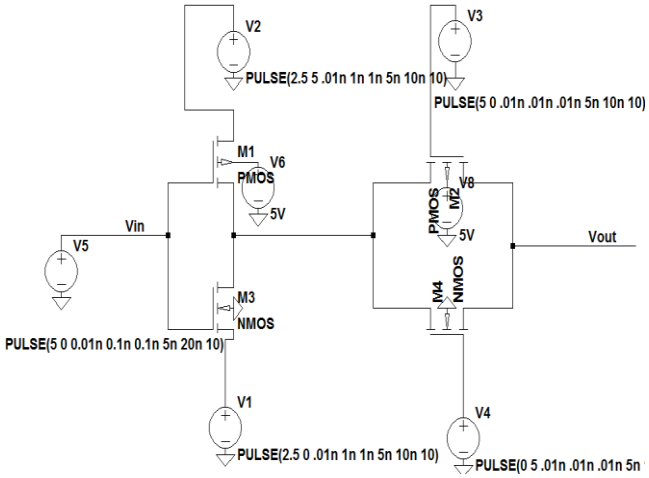

Fig 12 SCRL inverter Simulation in LTSPICE

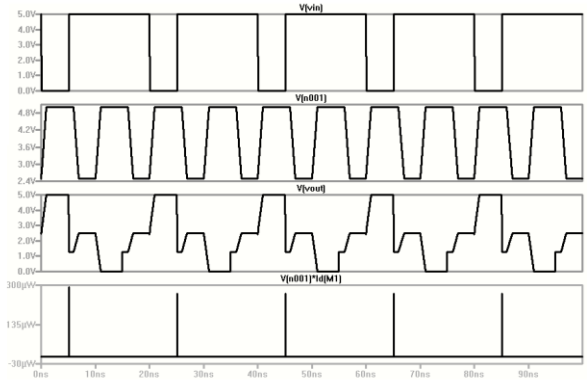

Fig 13 SCRL inverter Simulation output in LTSPICE

A SCRL NAND gate comprising of two NMOS transistors in pull down network connected in series and two PMOS transistors in pull network connected in parallel is simulated using a time varying supply and its power result is shown in the waveform.

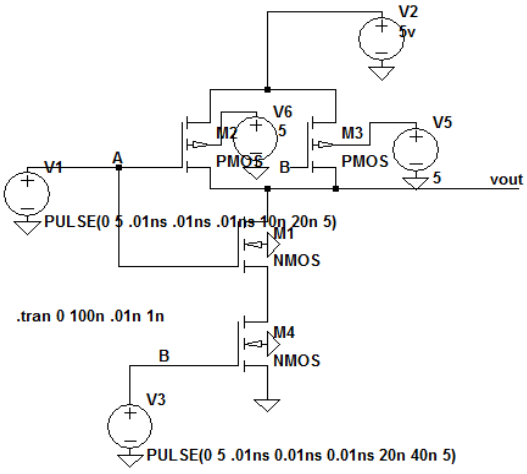

Fig 14 conventional NAND gate simulation in LTspice

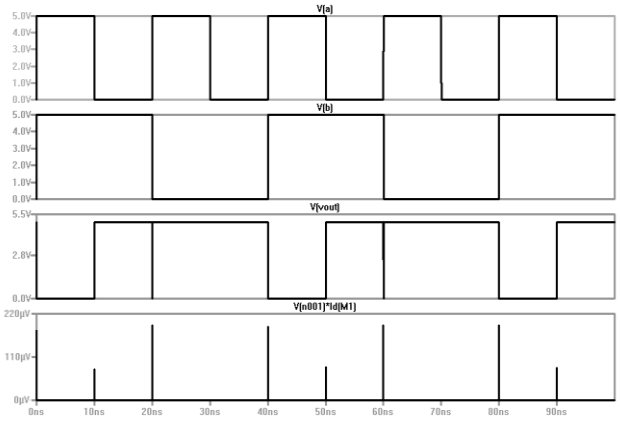

Fig 15conventional NAND gate simulation output

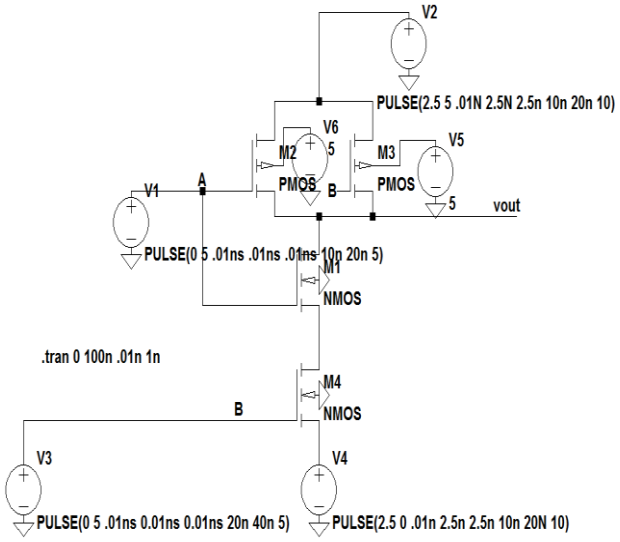

Fig 16 SCRL NAND gate Simulation

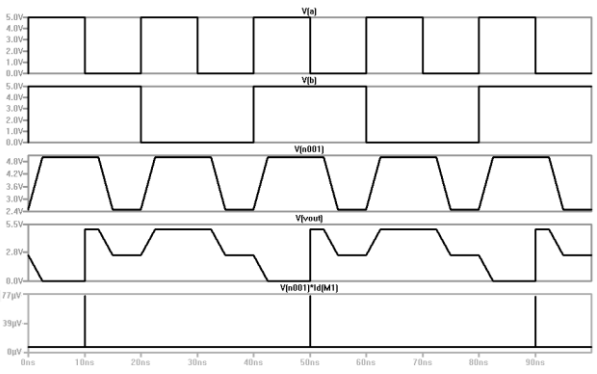

Fig 17 SCRL NAND gate Simulation output

This result shows that the SCRL reduces the energy consumption by about two (or four) times as compared to static CMOS logic in the 10MHz to 100 MHz range.

5. CONCLUSION

This paper presents the Adiabatic SCRL logic. The performance of SCRL has less power dissipation as compared with that of static CMOS logic circuit. SCRL is a low energy adiabatic logic. Simulation indicates power saving over static CMOS circuits. Simulation of an inverter circuit, a two input NAND gate and 4 bit CLA circuit is studied. SCRL proves to be a large power saving technique and shows the promising usage of SCRL in a low power system.

6. REFERENCES

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