A New Method for Balancing Capacitors Voltages in NPC Inverter without DC-link Voltages Sensors

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ABSTRACT
This paper presents a simple SVM technique of capacitors voltages balance for three-level NPC inverters. In the proposed SVM algorithm the voltages sensors are not required. An adaptative observer to estimate capacitors voltages was used. The presented SVM technique slightly modifies space vector modulation technique by adding a control parameter which is used to adjust the distribution of vector times of middle voltage vector according to the capacitors voltages. Simulation results are given to show the validity of the proposed balance algorithm.

Keywords
SVM, three-level NPC inverters, capacitor voltage balance, adaptative observer.

1. INTRODUCTION
The neutral-point-clamped (NPC) converter [1] is the multilevel topology most extensively used nowadays (Figure 1). One of the most important requirements in the operation of multilevel NPC converters is balancing capacitors voltages. They define all levels of the converter output voltage. However, the voltage across the capacitor may grow or decay so that the NP voltage fails to keep the half of the DC link voltage. They have a direct impact on the operation of the converters, as their variations are found on the voltages applied to the switching cells. This imbalanced condition needing higher rated capacitors and also can causes failure of the power semiconductors.

The capacitors voltages must be equitably distributed to ensure a balanced distribution of the constraints in power switches voltage. Many voltage balancing techniques have been proposed to solve this dc-link capacitor imbalance problem: hardware and software techniques. In [2], the author suggested the use of the intermediate circuits of voltages balancing. These circuits transfer energy from the higher capacitor voltage to an adjacent lower capacitor voltage. A variety of different auxiliary circuits has been introduced to solve this problem by [3,4]. This solution increases the complexity in multilevel NPC topologies. Moreover, the cost and the size of the systems become burden for conceptor.

So, several modified space vector modulators have been proposed in literature [5,6,7] to overcome the inconvenient of the hardware solution. These methods focus on using redundant state switching to achieve neutral point regulation. They seek to find the optimal switching sequence allows balancing voltages. Differences between these methods can be summarized:

- How to locate the reference voltage;
- find the optimal switching sequence,
- Calculating the optimal switching sequence duration.

In [8], the problem of balancing capacitors voltages is discussed. The authors demonstrated that multilevel inverters could not balance the capacitors voltages without sacrificing performance output voltage.

This paper presents a new SVM method to balance NPC capacitors voltages. The neutral-point voltage control by changing the dwelling-time of the medium vectors is easy to implement. The proposed scheme is able to deal with the voltage unbalancing problem effectively. Furthermore, the proposed algorithm uses the estimation observers of capacitors voltages developed in [9].This paper is organized as follows. In Section 2, the conventional SVM control Strategies is presented with the modified algorithm. Observer design for capacitors voltages NPC inverter is given in Section 3. Finally, simulation results are given in order to validate the proposed algorithm.

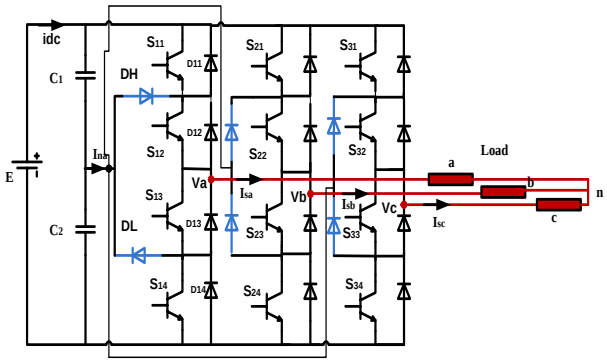

Figure 1: Three-levels NPC converter topologies

2. PWM CONTROL STRATEGIES OF MULTILEVEL INVERTERS

2.1 Open Loop PWM control Strategies

SVM is a highly efficient method of generating the six-pulsed signals for the inverter stage of the motor drive. Conventional switching techniques treat each phase as a separately generated sinusoid that is displaced by 120 degrees. However, a change in the voltage of one half-bridge due to switching invariably influences the other two-phase voltages [10]. SVPWM evaluates the switching schema as a whole, which results in better use of the DC bus and generates significantly less harmonic distortion than the sine triangle method [10].

The SVM control of the 3 levels NPC inverter consists to control it in the (α, β) coordinates which can generate 27 possible voltages vectors (Figure 2). They are divided in: 6 Big vectors (PNN, PPN, NPN, NPP, NNP,PNP), 6 medium vectors (PON,OPN,NPO,NOP,ONP,PNO), 12 small vectors (with redundancy: (PPO,OON), (OPO,NON), (OPP,NOO), (OOP,NNO), (ONO,POP), (POO,ONN)) and 3 zero vectors (OOO,NNN,PPP). When the power devices, S_{k1} and S_{k2}, are connected to the positive DC-link rail the state is noted by "P". In contrast, when the output is connected to the negative DC-rail by turning both S_{k3} and S_{k4} on, the state is called "N". Moreover, the switching state is defined as "O" when S_{k2} and S_{k3} both power devices, are on.

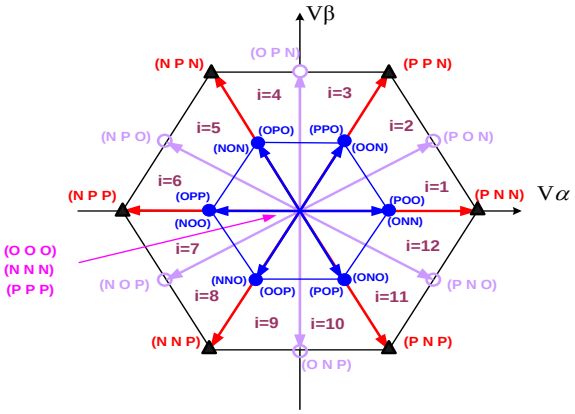

Figure 2: Space vectors Voltage for NPC inverter.

The objective of SVPWM technique is to approximate a reference space vector V_s somewhere within the hexagon of Figure 2**: Space vectors Voltage for NPC inverter**. using a combination of the 27 switching vectors. Indeed, when the reference voltage is in a sector, several couples of vector are possible.

For example in the sector 1 (Figure 3), the V_s vector can be divided on V_{1a}, V_{12} or V_{1b}, V_{12}. We choose the second solution, since V_{1b} is greater in amplitude than V_{1a}. We used only the big and the medium vector to ensure the calculation of the dwelling time of the vector V_s. The table 1 gives examples of switching states sequence in sector 1, 2, 3 and 4.

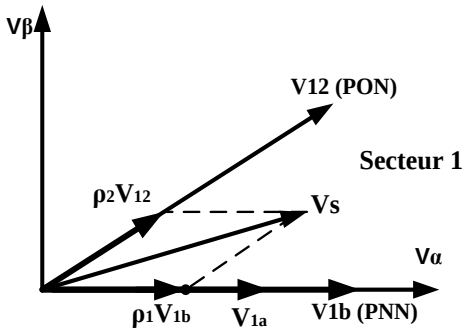

Figure 3. Sector 1

Let T_{mod} be a modulation period , T_{1b} dwelling time of the first vector V_{1b}, T_{12} dwelling time of the second vector V_{12} and $T_{nul} = T_{mod} - T_{1b} - T_{12}$: dwelling time of zero vectors. We define the duty cycle ρ_1 and ρ_2 related to times T_{1b} and T_{12} respectively of the vector V_{1b} and V_{1a} by:

$$\rho_1 = \frac{T_1}{T_{\text{mod}}} \quad , \quad \rho_2 = \frac{T_{12}}{T_{\text{mod}}} \tag{1}$$

For one modulation period T_{mod}, the output voltage of the inverter is given by:

$$T_{\text{mod}} V_S = (T_{1b} V_{1b} + T_{12} V_{12} + T_3 V_{Null}) \tag{2}$$

And the dwelling time of each vector is given by:

$$\begin{cases} T_{1b} = \dfrac{2\sqrt{3} T_{\text{mod}}}{E} \left(\dfrac{1}{2\sqrt{2}} V_{s\alpha} - \dfrac{\sqrt{3}}{2\sqrt{2}} V_{s\beta} \right) \\ T_{12} = \dfrac{2\sqrt{2} T_{\text{mod}}}{E} V_{s\beta} \\ T_{null} = T_{\text{mod}} - T_{12} - T_{1b} \end{cases} \tag{3}$$

For more details see [11].

Table 1. Sequence of switching states

Sector	Sector 1	Sector 2	Sector 3	Sector 4
Sequence	PNN	PON	PPN	OPN
	PON	PPN	OPN	NPO
	OOO	NNN	NNN	NNN
	OOO	NNN	NNN	NNN
	PON	PPN	OPN	NPO
	PNN	PON	PPN	OPN

The Figure **4** shows illustration an example of switching states sequence in sector 1.

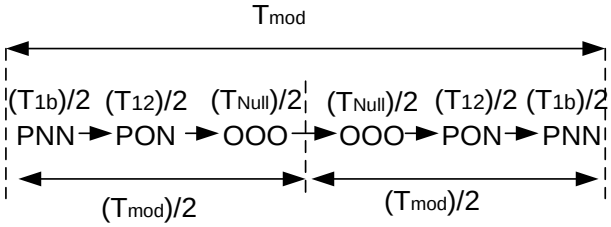

Figure 4: Illustration of switching states sequence in sector 1

The Figure 8 shows the classical algorithm to determine the sector number corresponding to the reference vector.

The weak point of this open loop PWM control is that does not guarantee the balance of capacitors voltages when a perturbation occurs. In order to demonstrate the effect of perturbation in capacitors voltages, we made small asymmetry in static characteristics and dynamic of four power components of three levels NPC inverter in Figure 1. In second step we made second system perturbation corresponding to the introduced asymmetry in the deriving signals duration (15 μs) of transistors (S11 and S12 in sector 1, S12 and S13 in sector 4, S13 and S14 in sector 5).

The Figure 6 and

Figure **5** highlights the necessity to balance the voltages across the capacitors. We note that the capacitors voltages continue to diverge. For this case the power devices cannot guarantee safe operation. The imbalance can destroy the capacitors and causes big damages in all system. For these reasons, we need closed loop algorithm to balance the voltages across the capacitors.

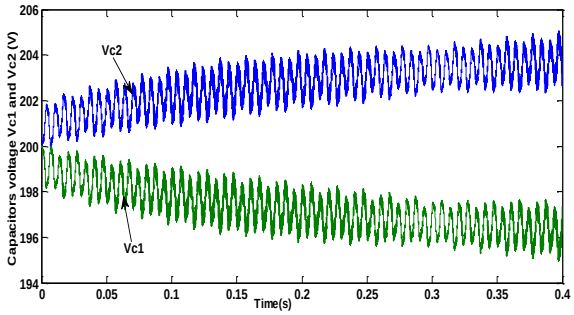

Figure 5 Capacitors voltages Vc1 and Vc2 (V) under the second perturbation (asymmetry in devices parameters)

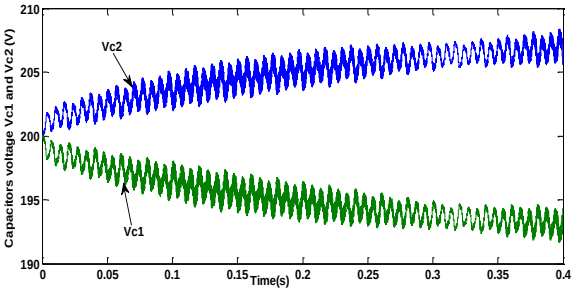

Figure 6 Capacitors voltages Vc1 and Vc2 (V) under perturbation (asymmetry in driving control signals)

2.2 Closed Loop PWM control Strategies

In order to explain the proposed closed loop algorithm, we give the effect of the four groups of vectors (large vectors, medium vectors, small vectors and zero vectors) in voltage balance of DC-link capacitors. The Table 2 shows the effect of switching states.

The effect of medium vector depends in the sign of current. Indeed, if the current is negative it discharges the upper capacitor and charge the lower capacitor and if the current is positive it has the inverse effect as shown in Figure 7.

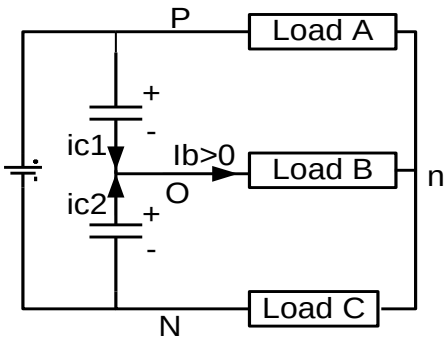

Figure 7: Effect of the medium vector PON

The equivalent circuit of Figure 7 corresponds to PON vector. In fact, in this state only the load B is connected to the middle point between two capacitors and affects voltages balancing.

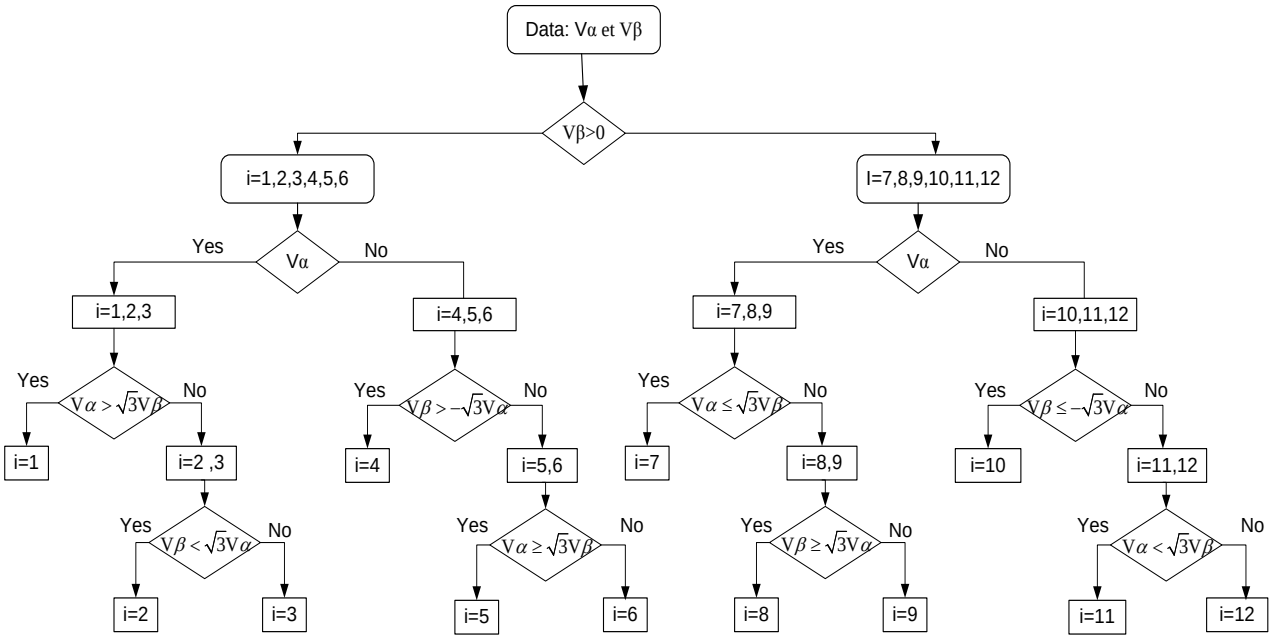

Figure 8: Flow chart of the reference vector location

Table 2. Effect of switching states on capacitors voltages

Voltage vector	Current path	Switching states	Effect on Neutral voltage
Zero voltage vector	No current	PPP, OOO, NNN	No effect
Small voltage vector	Upper capacitor only	POO, PPO, OPO, OPP, OOP, POP	Increase
	Lower capacitor only	ONN, ONN, NON, NOO, NNO, ONO,	Decrease
Medium voltage vector	----------	PON, OPN, NPO, NOP, ONP, PNO	Depend upon load current
Big voltage vector	both	PNN, PPN, NPN, NPP, NNP, PNP	No effect

In order to balance capacitors voltages, we propose a new method based on the change of the applied vector times. The new PWM technique modifies slightly the distribution of the middle vector duration according to the voltages across each capacitor by adding a control factor.

The reference voltage vector corresponding to the equivalent circuit of Figure 7 is located in sector 1. The switching states corresponding to this sector is shown in Figure 4. The switching times for T_{12} and T_{Null} are slightly adjusted according to the capacitor voltages as shown in following equation (4), (5) and (6):

$$\Delta t = f * \mathrm{sgn}(Vc1 - Vc2) * \mathrm{sgn}(In) * |Vc1 - Vc2| * T_{12} \quad (4)$$

$$(T_{12})_{new} = (T_{12})_{old} - \Delta t \quad (5)$$

$$(T_{null})_{new} = (T_{null})_{old} + \Delta t \quad (6)$$

Where:

$$\mathrm{sgn}(G)=\begin{cases}1 & if\ G\geq 0\\ -1 & else\end{cases}$$

f is a real positive parameter. In our case we have chosen $f\leq 0.2$ in order to limit the capacitors voltage variation (ΔVc) less than 1% of the applied voltage E.
In is the current middle point when a medium vector is applied.

In general cases the proposed algorithm can be given by the following expressions available for all sectors:

$$\Delta t = f*\mathrm{sgn}(Vc1-Vc2)*\mathrm{sgn}(In)*|Vc1-Vc2|*T_{medium} \quad (7)$$

$$(T_{medium})_{new}=(T_{medium})_{old}-\Delta t \quad (8)$$

$$(T_{null})_{new}=(T_{null})_{old}+\Delta t \quad (9)$$

3. OBSERVER DESIGN OF CAPACITORS VOLTAGES

The DC side of the three levels NPC inverter (Figure 1) has a DC source *E* and two connections capacitors C_1 and C_2. The switching variable γ_k represents the state of the multilevel inverter active switches, S_{kj}, $k\in\{1,2,3\}$, $j\in\{1,2,3,4\}$.

The three states of the binary switching γ_k can be defined as:

$$\gamma_k=\begin{cases}1 & (S_{k1}=1\wedge S_{k2}=1)\wedge(S_{k3}=0\wedge S_{k4}=0)\\ 0 & (S_{k1}=0\wedge S_{k2}=1)\wedge(S_{k3}=1\wedge S_{k4}=0)\\ -1 & (S_{k1}=0\wedge S_{k2}=0)\wedge(S_{k3}=1\wedge S_{k4}=1)\end{cases}$$

Applying the Kirchhoff laws to the three level inverter circuit (Figure 1) and doing some mathematical manipulations, the dynamic equations of the AC currents, I_{sa}, I_{sb} and I_{sc}, and the capacitor voltages, V_{C1} and V_{C2}, are defined as functions of the circuit parameters and switching variables γ_k:

$$\begin{bmatrix}\frac{dI_{sa}}{dt}\\ \frac{dI_{sb}}{dt}\\ \frac{dI_{sc}}{dt}\\ \frac{dV_{c1}}{dt}\\ \frac{dV_{c2}}{dt}\end{bmatrix}=\begin{bmatrix}-\frac{R}{L} & 0 & 0 & \frac{\psi_{11}}{L} & \frac{\psi_{12}}{L}\\ 0 & -\frac{R}{L} & 0 & \frac{\psi_{21}}{L} & \frac{\psi_{22}}{L}\\ 0 & 0 & -\frac{R}{L} & \frac{\psi_{31}}{L} & \frac{\psi_{31}}{L}\\ -\frac{\Gamma_{11}}{C_1} & -\frac{\Gamma_{12}}{C_1} & -\frac{\Gamma_{13}}{C_1} & 0 & 0\\ -\frac{\Gamma_{21}}{C_2} & -\frac{\Gamma_{22}}{C_2} & -\frac{\Gamma_{23}}{C_2} & 0 & 0\end{bmatrix}\begin{bmatrix}I_{sa}\\ I_{sb}\\ I_{sc}\\ V_{c1}\\ V_{c2}\end{bmatrix}+\begin{bmatrix}0\\ 0\\ 0\\ \frac{1}{C_1}\\ \frac{1}{C2}\end{bmatrix}\times idc \quad (10)$$

And

$$\Gamma_{1k}=\frac{\gamma_k(\gamma_k+1)}{2},\Gamma_{2k}=\frac{\gamma_k(-\gamma_k+1)}{2},\psi_{ki}=\frac{1}{3}(2\Gamma_{ik}-\sum_{j=1,j\neq k}^{3}\Gamma_{ik}) \quad (11)$$

In order to obtain a simplified model which contains less equation, we changes the switching sequences in the (α, β) coordinates:

$$X_{123}=[T]X_{\alpha\beta} \quad (12)$$

Where *T* is the Concordia transformation:

$$T=\frac{\sqrt{2}}{\sqrt{3}}\begin{pmatrix}1 & 0\\ -\frac{1}{2} & \frac{\sqrt{3}}{2}\\ -\frac{1}{2} & -\frac{\sqrt{3}}{2}\end{pmatrix} \quad (7) \quad (13)$$

Applying (12) and (13) to the equation (10), the new model is represented in (α, β) coordinates by:

$$\begin{bmatrix}\frac{dI_\alpha}{dt}\\ \frac{dI_\beta}{dt}\\ \frac{dV_{c1}}{dt}\\ \frac{dV_{c2}}{dt}\end{bmatrix}=\begin{bmatrix}-\frac{R}{L} & 0 & \frac{\Gamma_{1\alpha}}{L} & \frac{\Gamma_{2\alpha}}{L}\\ 0 & -\frac{R}{L} & \frac{\Gamma_{1\beta}}{L} & \frac{\Gamma_{2\beta}}{L}\\ -\frac{\Gamma_{1\alpha}}{C_1} & -\frac{\Gamma_{1\beta}}{C_1} & 0 & 0\\ -\frac{\Gamma_{2\alpha}}{C_2} & -\frac{\Gamma_{2\beta}}{C_2} & 0 & 0\end{bmatrix}\begin{bmatrix}I_\alpha\\ I_\beta\\ V_{c1}\\ V_{c2}\end{bmatrix}+\begin{bmatrix}0\\ 0\\ \frac{1}{C_1}\\ \frac{1}{C_2}\end{bmatrix}\times idc \quad (14)$$

Where

$$\Gamma_{i\alpha}=\frac{\sqrt{2}}{\sqrt{3}}(\Gamma_{i1}-\frac{\Gamma_{i2}}{2}-\frac{\Gamma_{i3}}{2}),\Gamma_{i\beta}=\frac{1}{\sqrt{2}}(\Gamma_{i2}-\Gamma_{i3}). \quad (15)$$

According in our works described in [9], an observer of (14) is the following system φ:

$$\varphi\begin{cases}\dot{\chi}_1=A_1(S_k)\chi_1+\Gamma_1(S_k,\chi_j)+P_1^{-1}C_1^T(\hat{y}-y)\\ \dot{\chi}_2=A_2(S_k)\chi_2+\Gamma_2(S_k,\chi_j)+P_2^{-1}C_2^T(\hat{y}-y)\\ P_1=-\theta_1P_1-A_1^T(S_k)P_1-P_1A_1(S_k)+C_1C_1^T\\ P_2=-\theta_2P_2-A_2^T(S_k)P_2-P_2A_2(S_k)+C_2C_2^T\end{cases} \quad (16)$$

Where: $\chi_j=(I_\alpha \quad I_\beta \quad V_{Cj})^T$ represents the state of the j^{th} subsystem, S_k are the instantaneous inputs applied to the system and *y* is the measurable output and:

$$A_j(S_k)=\begin{bmatrix} -\frac{R}{L} & 0 & \frac{\Gamma_{j\alpha}}{L} \\ 0 & -\frac{R}{L} & \frac{\Gamma_{j\beta}}{L} \\ -\frac{\Gamma_{j\alpha}}{C_j} & -\frac{\Gamma_{j\beta}}{C_j} & 0 \end{bmatrix}, \Gamma_i(S_k,\chi_j)=\begin{bmatrix} \frac{\Gamma_{i\alpha}}{L} \\ \frac{\Gamma_{i\beta}}{L} \\ 0 \end{bmatrix} V_{Ci}+\begin{bmatrix} 0 \\ 0 \\ \frac{1}{C_j} \end{bmatrix} \times idc,$$

$$j=1,2, \quad k=1,2,3 \quad i=1,2\neq j$$

And $C=\begin{pmatrix}1 & 1 & 0\end{pmatrix}$.

A detailed simulation was carried out in [9] to validate the proposed interconnected observer using average model of three levels NPC inverter developed in [12].

4. SIMULATION RESULTS

In this section, a detailed simulation was carried out to validate the proposed algorithm for balancing capacitors voltages. The general block diagram is shown in Figure 9. The observer block corresponds to equation systems given by (16). The capacitors values are C_1=C_2=1000 μF . The NPC Inverter is connected at three equilibrium phases where each phase composed by an inductor L=10mH and a resistor R=20 Ω . To estimate the NPC capacitor voltages according to (16) the observer parameter gain θ_j =15000 for j=1, 2, are used. The switching frequency was fixed at 10kHz. The value of DC-link voltage E is 400V. Simulations were carried out using MATLAB/SIMULINK. Matlab simulator is an important tool where different system models (electrical, mechanical, thermal...) can be developed.

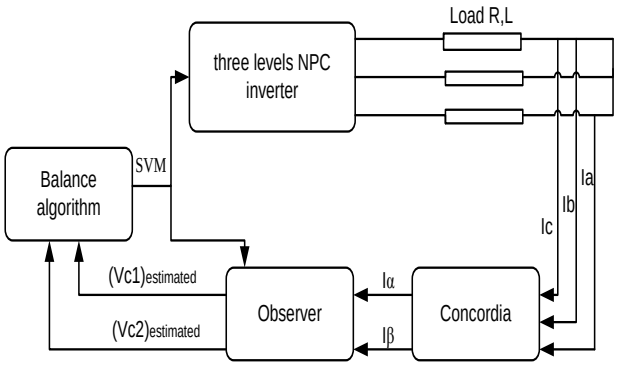

Figure 9 Block diagram of balance capacitors voltages system

In the case of the first system perturbation corresponding to the nonlinearities of static and dynamic characteristics of the first leg uppers devices (S_{11}, S_{12}, D_{11}, D_{12}), Figure 1010Figure 12, 12 shows the new electrical waveforms obtained by the new algorithm.

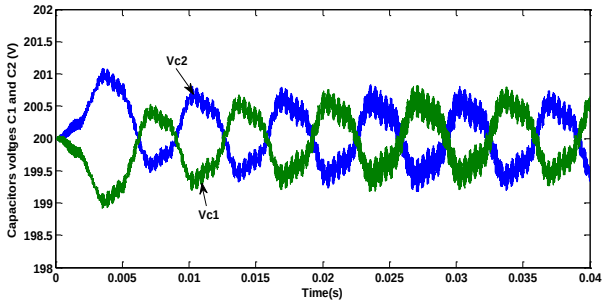

Figure 10 Capacitors voltage Vc1 and Vc2 (V) under first perturbation

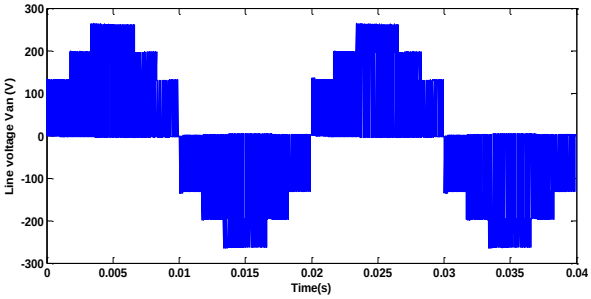

Figure 11 Van Line voltage under first perturbation

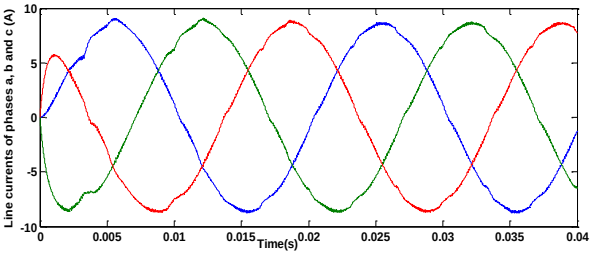

Figure 12 Line currents of phase a, b and c (A) under first perturbation

In the case of the second system perturbation corresponding to the introduce of asymmetry in the deriving signals duration (15 μs .) of transistors (S11 and S12 in sector 1, S12 and S13 in sector 4, S13 and S14 in sector 5). Figure 13 and 14 shows the new electrical waveforms obtained by our algorithm.

From these Figures, it is shown that voltage across NPC inverter capacitors do not diverge and oscillate around E/2 with a ripple value less than 1% of the applied voltage E. In our case the voltages variation across each capacitor is less than 1V. According to the given results, the voltage balance can be achieved quickly.

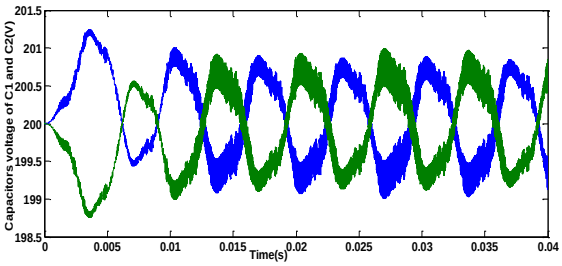

Figure 13 Capacitors voltage Vc1 and Vc2 (V) under second perturbation

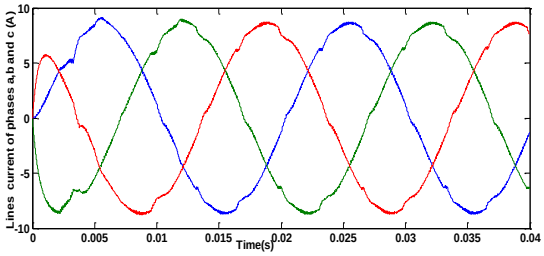

Figure 14 Line currents of phase a, b and c (A) under second perturbation

In Figures 12 and 14, we can see a distortion in the load current waveforms induced by the proposed algorithm.

Figure 15 shows the load current spectra obtained by a NPC converter without any perturbation (all semiconductors devices have the same static and dynamic characteristics and a symmetric control signals).

Figure 16 shows the load current spectra obtained by a NPC converter using the new algorithm when asymmetric control signals are used (default described above) which corresponds to the real experimental conditions. We can see the appearance of 5, 7, 11 and 17 order harmonics due to the distortion in load current.

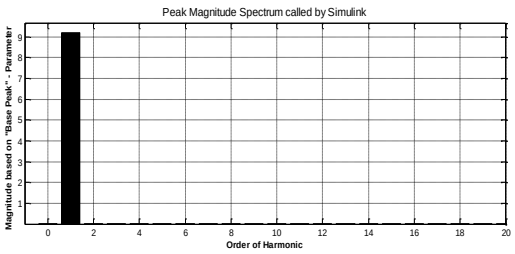

Figure 15 Spectra of the load current without default

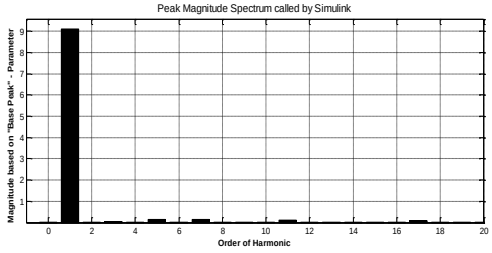

Figure 16 Spectra of the first load current with asymmetry in control

Using the proposed technique to balance voltages magnitude across each capacitor voltage is not the ideal solution but it can be considered as a simplified technique to stabilize these voltages variations. The harmonics distortion (THD) is less than 3%.

5. CONCLUSION

This paper proposed a simple approach to balancing the DC-link for three levels NPC inverter. The proposed technique is based on a additional control parameter used to adjust the distribution of the middle vectors applied times according to the capacitors voltages variations. In the presented new technique the voltages sensors are not used. Indeed, we used an observer to estimate the capacitors voltages because measuring voltages becomes expensive and impractical due to of the highs voltages and power levels handled in such applications. The modified SVM technique use a less switching vectors sequences, only 15 vectors (6 big vectors, 6 medium vectors, and 3 zero vectors) instead of refined SVM technique which uses 27 states vectors. The proposed technique minimizes the switching losses and makes the SVM easy to implement. The registered Total Harmonic Distortion of current waveforms is less than 3%.

6. REFERENCES

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