Hardware Description of Digital Adaptive IIR Filters for Implementing on FPGA

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ABSTRACT
The hardware description and implementation of adaptive infinite-impulse-response (IIR) filters for real-time applications is an important and challenging designing issue. The aim of this paper is hardware description of digital adaptive IIR filters for implementing on field programmable gate array (FPGA) chips. The direct architecture is considered for IIR filter designing and Equation-Error (EE) Least Mean Square (LMS) adaptive algorithm is employed for updating filter coefficients. Adaptive IIR filter is employed in interference cancellation and inverse system identification applications and the results are compared with finite-impulse-response (FIR) filter in terms of convergence speed, maximum operating frequency, chip area and power dissipation criteria. The VHDL hardware description language is used for providing hardware models and descriptions of algorithms and applications. The results achieved from QUARTUS II synthesize tool on a single STRATIXII chip, EP2S15F484C3, from ALTERA Inc. demonstrate that the adaptive IIR architecture has better performance than adaptive FIR architecture for inverse system identification application while for interference cancellation application adaptive FIR filter works better than adaptive IIR filter.

General Terms
Hardware Description, Adaptive Digital Filters, FPGA, VHDL.

Keywords
Adaptive IIR, Equation-Error LMS, Interference Cancellation, Inverse System Identification.

1. INTRODUCTION
The design of digital filters with fixed coefficients requires well defined thorough specifications of input and reference signals for suitable operation of filter. However, in many practical conditions and applications the specifications is not available, or is time varying. The solution for these applications is using digital filters with adaptive coefficients, known as adaptive filters [1, 2]. In general, any filter structure, FIR and IIR filters, could be used as an adaptive digital filter. The main advantage of IIR filters is producing equivalent frequency response to FIR filters with less number of coefficients and reducing design complexity and resource utilization such as reducing number of adding, multiplying and shifting operations for implementing the filter. This could be considered as a reason of using IIR adaptive filters. There are, however, a number of problems associated with the use of IIR adaptive filters. Fundamentally an adaptive IIR filter is unstable if poles of IIR filter stay outside of the unit circle and the convergence speed of IIR systems tend to be slow. Furthermore, an error surface with local minima or biased global minimum may be observed depending on the objective function. The IIR filters are more susceptible to coefficient quantization error than FIR filter, due to the feedback solution [3, 4, 5]. The hardware implementation and description of digital adaptive IIR filters is an important and challenging issue considering different optimization factors such as chip area, filter operating frequency and power consumption. In most cases IIR filters have been implemented by DSPs and ASICs using adapting architectures for filtering algorithms. Recently, the FPGA technology [6] is mainly employed for digital signal processing applications [7] due to the flexibility and efficiency of designing complex circuits and systems where the practical application of FPGAs are increased dramatically. There are interesting works in the literature confirming efficiency of FPGA technology for implementing different schemes and models of adaptive filtering applications [8]-[15]. Implementation of IIR filters on FPGA has some interesting advantages, such as full adaptation of FPGA structure to the filtering algorithm, high throughput, hardware utilization effectiveness and achieving high rate of calculating precision[16]-[19]. The introduction of VHSIC Hardware Description Language (VHDL) [20] provided a modeling and simulation environment for fast prototyping digital circuits and systems on FPGA using modern simulation, synthesizing and programming tools. The aim of this paper is hardware description of adaptive digital IIR filters for implementing on FPGA chips using direct IIR architecture and Equation-Error Least Mean Square adaptive algorithm. The performance of IIR filter is compared to FIR filter for Interference Cancellation and Inverse System Identification applications. The rest of the paper is organized as follows. Section 2 presents the adaptive IIR filtering algorithms including the direct form of implementing IIR filter for adaptive algorithms. The simulation results for all modules are presented in section 3 and the paper is concluded in section 4.

2. ADAPTIVE IIR FILTER ARCHITECTURE
This section presents the architecture of adaptive IIR filter including the least mean-square (LMS) algorithm and the Equation-Error architecture.

2.1 The LMS Adaptive Algorithm
The least mean-square (LMS) algorithm is a stochastic gradient descent method where the filter coefficients are updated using error signal information. Considering this approach, the next state filter coefficient vector $w(n+1)$ is a function of present state filter coefficient vector $w(n)$ and a factor proportional to the negative gradient. The following mathematical model describes the LMS algorithm.

$$w(n+1) = w(n) - \frac{\mu}{2}\nabla(n) \quad (1)$$

The μ parameter is the learning factor or step size of LMS algorithm that controls the stability and the rate of convergence of the algorithm and the gradient is represented by $\nabla(n)$.

2.2 Equation-Error LMS Adaptive Algorithm

Adaptive IIR filtering methods are commonly classified into the Equation-Error and the Output-Error architectures. The Equation-Error architecture has some interesting features such as unimodal error surface and guaranteed system stability compared to the Output-Error architecture. In spite of the advantages, Equation-Error approach faces some problems such as generating biased coefficients in the presence of noise and the slow speed of convergence. For overcoming the slow speed of convergence problem in adaptive IIR filtering, the recursive least squares (RLS)-type algorithms have been developed. Furthermore several algorithms have been introduced for noise removal of Equation-Error approach. The architecture of Equation-Error algorithm is shown in Figure 1 and the updating procedure of Equation-Error LMS algorithm is described as follows:

$$w(n+1) = w(n) + \mu e(n)u(n) \qquad (2)$$

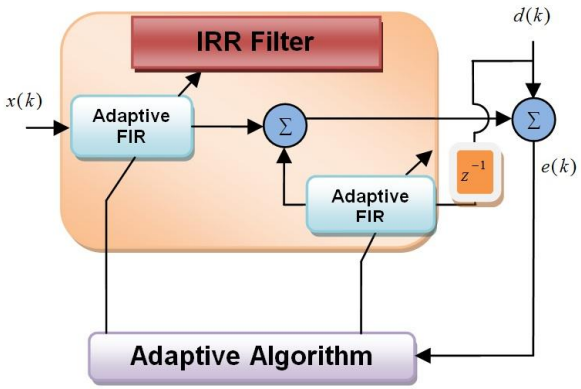


Fig 1: The diagram of Equation-Error algorithm

Configuration of EE-LMS algorithm is shown in Figure 2. This architecture is not actually recursive and consists of two FIR LMS filters. It is clear that such the Equation-Error solution is biased when the system is used in noisy conditions. The mathematical justification is that if the system were adapted with an exactly zero error, then $y(n) = d(n)$. In order that $y(n)$ approximated as $d(n)$ should allow adoption in conditions of zero noise.

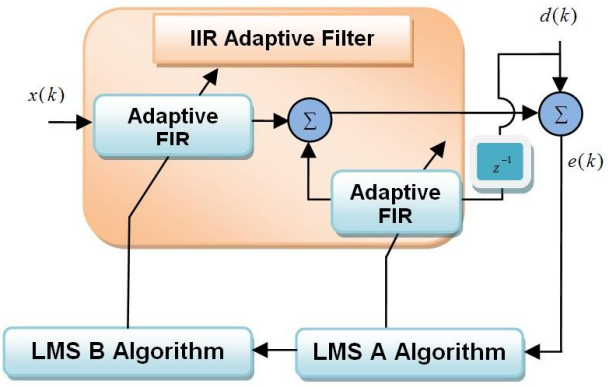


Fig 2: The Architecture of Equation Error LMS Algorithm

2.3 Architecture of Adaptive IIR Filter

Several architectures have been proposed for designing adaptive IIR filters such as direct form, lattice form, cascade-form, parallel-form and state-space structures. Among them, the direct form is most popular in the literature and mainly used for designing adaptive IIR filters. The block diagram shown in Figure 3 is a direct form of adaptive IIR filter which mainly consists of shift registers, adders and multipliers. As a hardware implementation standpoint one scaling for μ and 6 general multipliers are required. The samples of input signal are multiplied by the filter coefficients and the error signal is then gathered together in the adder block.

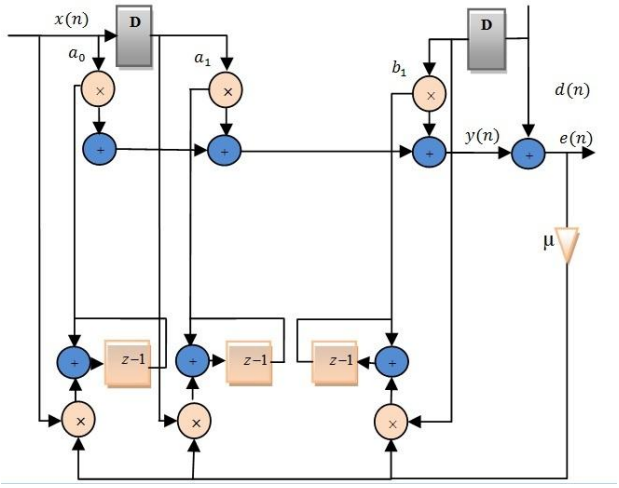


Fig 3: The Architecture of Direct IIR Filter

3. SIMULATION RESULTS: APPLICATION MODELING

In this section the simulation results of hardware description of adaptive digital IIR filters for implementing on a single FPGA chip are presented. The adaptive digital IIR filter is applied to interference cancellation and inverse system identification applications and the results are compared to the adaptive FIR filter in terms of convergence speed, chip area utilization, power dissipation and filter maximum operating frequency. In these simulation results the step-size parameter is assumed to be μ=0.25 and all coefficients are scaled by 128 due to fractional format of input signals. The digital adaptive filters are modeled and described by VHDL and synthesized on STRATIXII IC family chip number EP2S15F484C3 from

ALTERA Inc. The Quartus II and Modelsim tools are used for synthesizing and simulating of VHDL models respectively.

3.1 Interference Cancellation

Practically, there are different considerable interferences in real applications and systems which should be removed and cancelled from original signals. For example in communication systems, interference cancellation is an important issue for protecting the information-bearing signals where interference could be considered and modeled by a random White Noise or a 50/60 Hz power-line hum. Figure 4 shows a typical configuration scheme for interference cancellation where $d(n)$ denotes the primary signal, $x(n)$ is the reference signal, $y(n)$ is considered as adaptive filter output and $e(n)$ is the error signal which is also considered as the system output in the interference cancellation configuration. Therefore, after convergence, the signal $x(n)$ which represents the additive inverse of the interference is subtracted from $d(n)$. In this application, a communication signal is considered that consists of three components: the information-bearing signal which is a Manchester encoded sensor signal $m(n)$ with amplitude B =10, shown in Figure 5(a), an additive Gaussian noise $n(n)$, shown in Figure 5(b), and a 50 Hz power-line hum interference with amplitude A=50, shown in Figure 5(c). Furthermore, the sampling frequency is 4×50 = 200Hz.

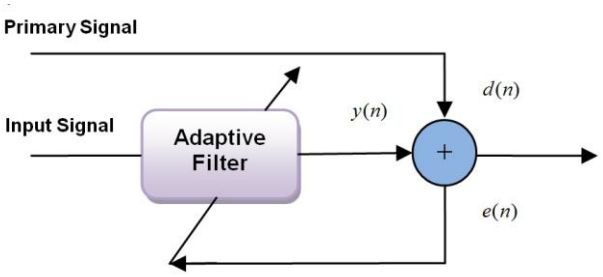


Fig 4: Description of a Typical Interference Cancellation System

The observed signal can therefore be formulated as follows which is shown in Figure 5(e).

$$d(n) = A\sin(\frac{\pi n}{2}) + Bm(n) + \sigma^2 n(n) \quad (3)$$

The reference signal $x(n)$, shown in Figure 5(d), which is applied to the adaptive filter input, is given as:

$$x(n) = \sin(\frac{\pi n}{2} + \varphi) \quad (4)$$

where $\varphi = \frac{\pi}{6}$ is considered as a constant offset.

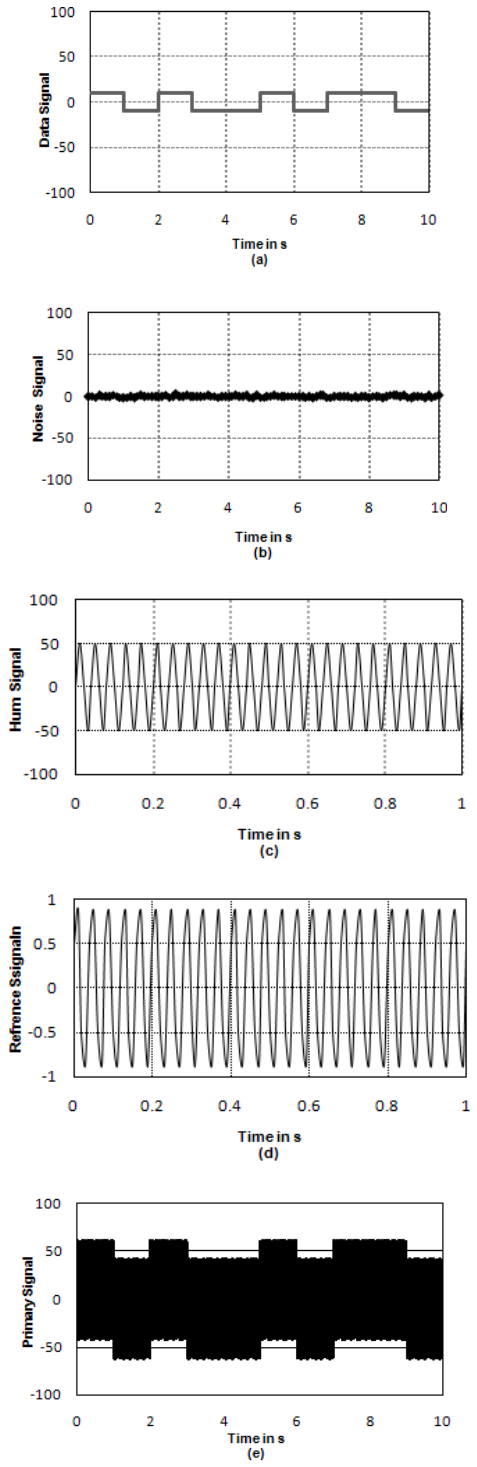
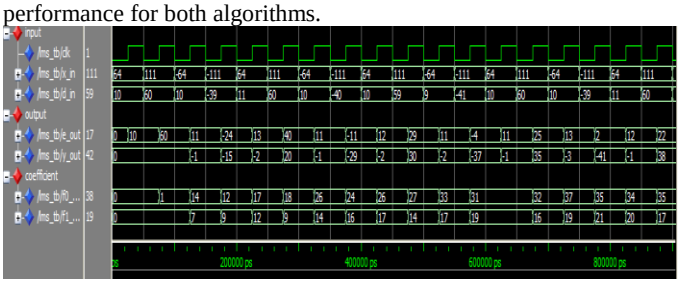


Fig 5:(a) Data signal (b) Noise signal (c) Reference signal (d) Hum. Signal (e) Primary signal

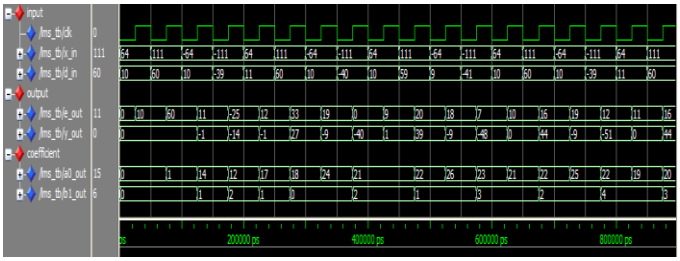
The timing diagram of the response of the adaptive filter, $y(n)$ and the overall system response, $e(n)$, to the reference signal $x(n)$ and the desired signal $d(n)$ is shown in Figure 6. The responses of the power-line interference cancellation system using LMS algorithm is shown in Figure 6(a) and using EE-LMS algorithm is shown in Figure 6(b), respectively.

The number of filter coefficients has an important effect on the system output. The number of coefficients for both filters

is considered to be 2, 3 and 5 coefficients and the simulation results achieved by Modelsim Software are shown in Figure 7(a) for 2 coefficients, Figure 7(b) for 3 coefficients and Figure 7(c) for 5 coefficients. As shown, increasing the number of coefficients would improve the system performance for both algorithms.



(a) Using LMS algorithm



(b) Using EE-LMS algorithm

Fig 6: VHDL simulation of the power-line interference cancellation

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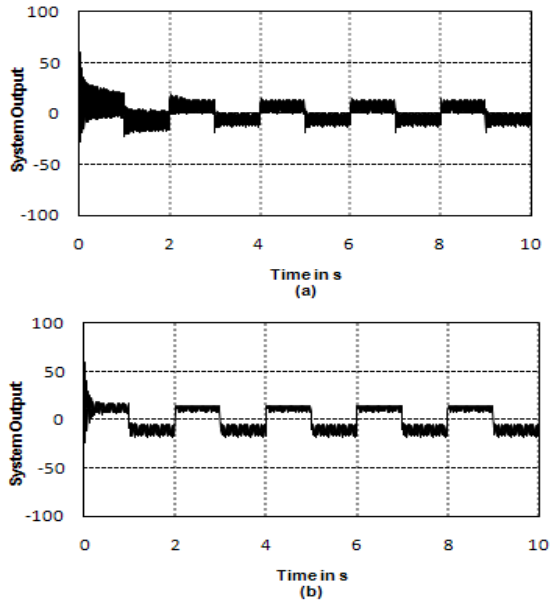

Fig 7(a): Simulation results (VHDL model) of the power-line interference cancellation with two coefficients: (a) Using EE-LMS algorithm (b) Using LMS algorithm

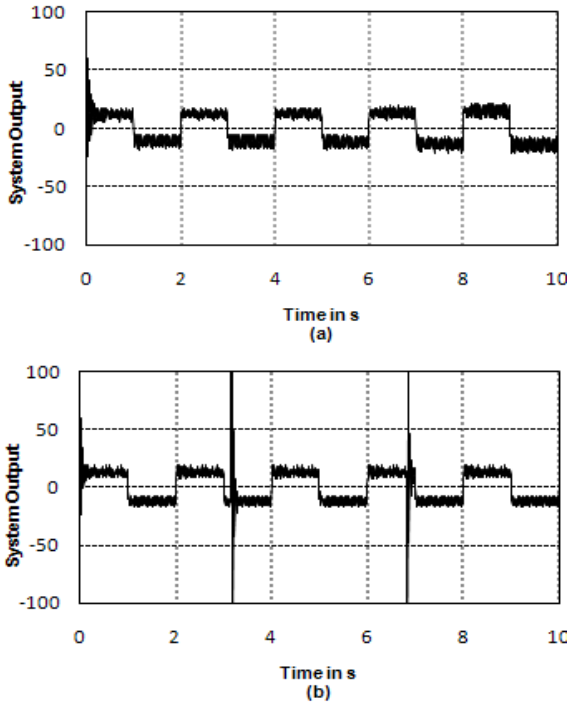

Fig.7 (b): Simulation results (VHDL model) of the power-line interference cancellation with three coefficient :(a) Using EE-LMS algorithm (b) Using LMS algorithm

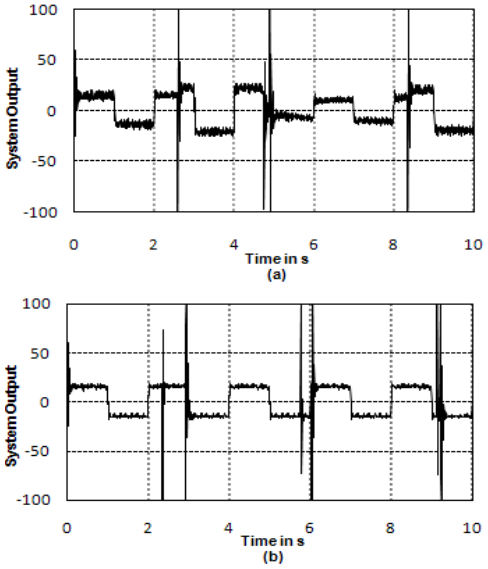

Fig7(c): Simulation results (VHDL model) of the power-line interference cancellation with five coefficient :(a) Using EE-LMS algorithm :(b) Using LMS algorithm

As shown in Figure 8(a) and Figure 8(b) the filter coefficients f_0_out , f_1_out for adaptive FIR filter and a_0_out, b_1_out for adaptive IIR filter are updated as long as the interference is removed from input signal and $e(n)$ is converged to data

signal. Furthermore, convergence speed of adaptive FIR filter is faster than that for adaptive IIR filter. For investigate the behavior of adaptive IIR filter the coefficients are obtained using the optimum Winer estimation [7] considering f_0_out =25 and f_1_out =43.3. If Winer estimation be considered as an optimal criterion then it is found that coefficients of adaptive IIR filter are biased, especially b_1_out as it is coefficient of recursive part.

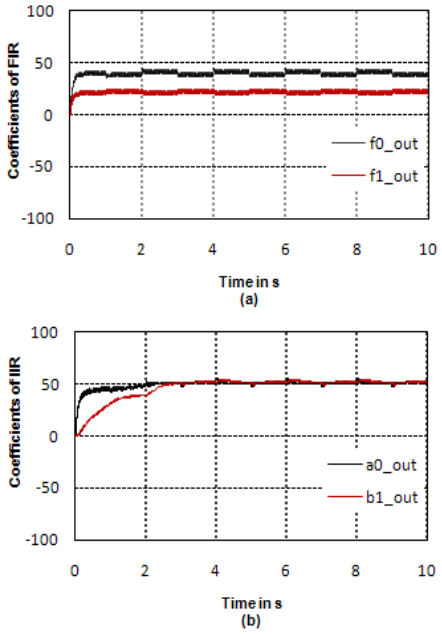

Fig 8: Filter Coefficients updating: (a) Using adaptive FIR filter (b) Using adaptive IIR filter

Optimization of filter designing parameters on FPGA is an important and challenging issue and synthesizing tools usually offer several optimization settings which affect the performance of filter, logic utilization, the power dissipation [21] and the maximum operating frequency of filter [22]. The results obtained from Quartus II tool are summarized in Tables 1-3.

Table 1. Maximum operating frequency (MHZ)

Numbers of Coefficient	2	3	5
Adaptive IIR	84.83	79.88	71.53
Adaptive FIR	84.82	81.25	68.65

Table 2. Power dissipation (MW)

Numbers of Coefficient	2	3	5
Adaptive IIR	325.78	326.22	326.75
Adaptive FIR	325.92	326.24	326.78

Table 3. Resource utilization

Chip Area		Total Register	ALUTS	DSP Element
Numbers of Coefficient of Adaptive IIR	2	24	42	4
	3	40	50	6
	5	72	98	10
Numbers of Coefficient of Adaptive FIR	2	32	42	4
	3	48	50	6
	5	80	98	10

3.2 Inverse System Identification

The system shown in Figure 9 illustrates the configuration of inverse system identification application. The input signal $d(n)$ enters the unknown system and the output of the unknown system $x(n)$ is the input of adaptive filter. After convergence, the adaptive filter transfer function approximates the inverse of the transfer function of the unknown system. For this scenario, an unknown system with following transfer function is considered.

$$H(Z) = 1 - 0.5z^{-1} \tag{5}$$

Using adaptive FIR filter, the inverse transfer function has many weights, as follows:

$$G(Z) = H^{-1}(Z) = 1 + 0.5z^{-1} - 0.25z^{-2} + 0.125z^{-3} - 0.0625z^{-4} + \ldots \tag{6}$$

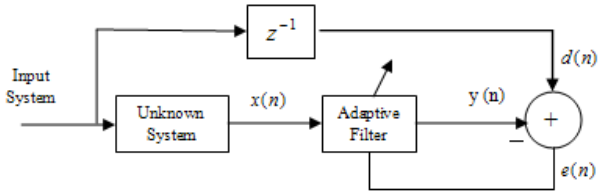

Fig 9: The block diagram of inverse system identification

Considering adaptive IIR filter, the inverse transfer function have only two weights:

$$G(Z) = H^{-1}(Z) = \frac{1}{1 - 0.5z^{-1}} \tag{7}$$

Therefore, for inverse system identification the EE-LMS algorithm with two coefficients based on adaptive IIR filter is applied, as follows;

$$y(n) = a_0 x(n) + b_1 d(n-1) \tag{8}$$

$$d(n) - e(n) = a_0 x(n) + b_1 d(n-1) \tag{9}$$

If $e(n) = 0$ then $d(n) - y(n) = 0$ that means $d(n) = y(n)$. Applying the EE-LMS algorithm:

$$D(Z) \cong a_0 X(Z) + b_1 z^{-1} D(Z) \tag{10}$$

$$G(Z) \cong \frac{D(Z)}{X(Z)} = \frac{a_0}{1 - b_1 z^{-1}} \tag{11}$$

The timing simulation result of is shown in Figure 10 and diagram of error signal and updated coefficients according to Modelsim simulation is shown in Figure 11, as observed $e(n) \cong 0$, thus $d(n) \cong y(n)$ and a_0_out=123/128=0.961≅1 and b_1_out =57/128=0.445≅0.5.

For input signal a sine wave is considered. Maximum operating frequency, logic utilization and the power dissipation is shown in Table 4. As observed adaptive IIR filter has better performance than FIR filter considering

greater maximum operating frequency, lower power dissipation and logic utilization in this application.

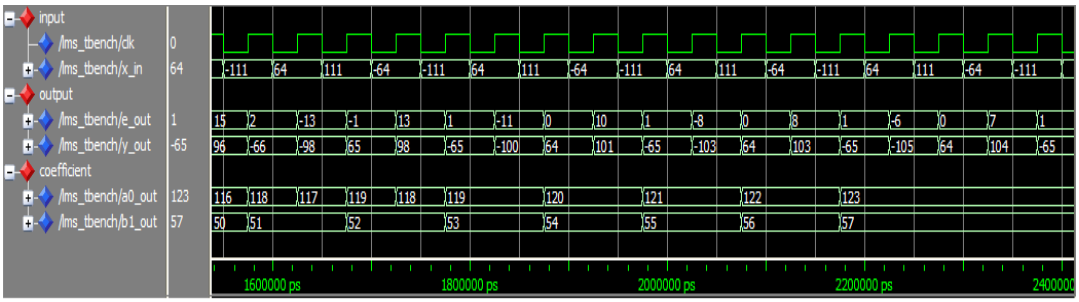

Fig 10: Timing diagram of VHDL model of inverse system identification

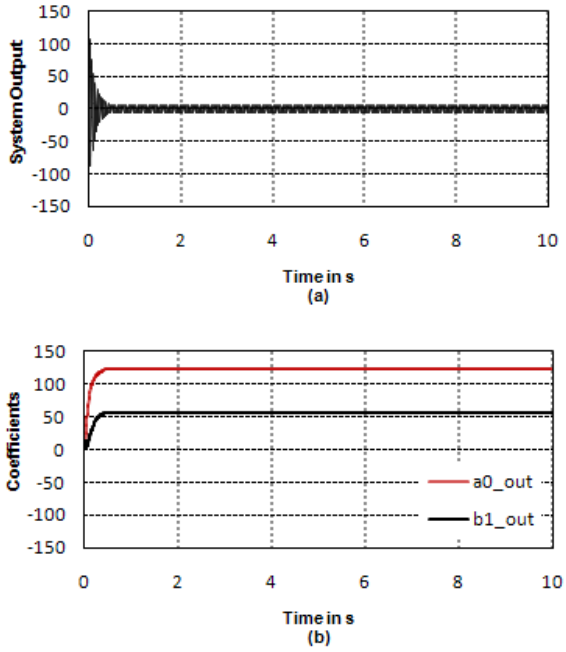

Fig 11: Inverse system identification using adaptive IIR filter: (a) System output (b) IIR filter coefficients

Table 4. Performance summary of filters

Resource	Adaptive IIR	Adaptive FIR
Total Register	32	264
ALUTs	59	490
DSP Element	4	60
Power(mw)	325.61	334.68
Speed(MHZ)	84.30	30.8

4. CONCLUSION

The hardware implementation of adaptive filters is an important issue in digital signal processing. In this paper hardware description of adaptive IIR filter on FPGA was proposed. Then behavior of IIR and FIR filters for interference cancellation and inverse system identification applications was compared in terms of convergence speed, maximum operating frequency, chip area and power dissipation. The results demonstrated that in interference cancellation application both filters approximately remove the interference but convergence speed of adaptive FIR filter was better than adaptive IIR filter and coefficients were optimal. While in inverse system identification application, adaptive IIR filter has better performance than adaptive FIR filter. As future works and directions, for improving filter operating frequency, the pipeline IIR filter could be considered using lattice and cascade structures of IIR filters.

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