# Logical Effort to Study the Performance of 32-bit Heterogeneous Adder

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## ABSTRACT
The method of Logical Effort is an easy way to estimate the delay in a CMOS circuit. In this work application of Logical Effort on transistor level analysis of 32-bit heterogeneous adder architecture is designed and presented. Heterogeneous architecture consists of concatenation of four different sub adders (Ripple Carry, Carry Look Ahead, Carry Skip and Carry Select Adder) to design an adder unit. The efficiency of the Logical Effort model is analyzed by circuit simulation using Tanner EDA Tool.

## Keywords
Absolute Delay, Electrical Effort, Heterogeneous Adder, Logical Effort, Stage Effort.

## 1. INTRODUCTION
Addition is one of the most common and often used arithmetic operations. Adder delay is critical in the design of high-performance processor. The delay is related to gate sizes and their terminal loads. The literature describes several adder configurations such as ripple carry, carry look ahead, carry skip and carry select. These single (homogeneous adder) has their own benefits and limitations with respect to performance parameters [1]. In order to design an optimized adder which provides area/delay tradeoffs, heterogeneous adder is presented and theory of Logical Effort is implemented to optimize delay.

The method of Logical Effort (LE) is an easy way to estimate the delay in a CMOS circuit. Logical Effort is a simple method that optimizes networks for speed.

The paper is presented as followed. Second section describes the theory of Logical Effort. Third section describes the heterogeneous adder architecture. The results of LE analysis and TSPICE simulation were shown in fourth section. Conclusion was given in the last section.

## 2. LOGICAL EFFORT MODEL
The theory of Logical Effort proposed by Sutherland and Sproull provides a method for fast back-of-the-envelope estimates of delay in a CMOS circuit. The model describes delays caused by the capacitive load that the logic gate drives and by the topology of the logic gate. As the load increases, the delay increases, but delay also depends the logic function of the gate. Inverters, the simplest logic gates, drive loads the best. Logic gates that compute other functions require more transistors.

The method of LE quantifies all effects to simplify delay analysis for individual logic gates and multi-stage logic networks. For modeling delays very initial step is to isolate the effects of particular integrated circuit fabrication process by expressing all delays in terms of a basic delay unit $\tau$. Thus the absolute delay is expressed as the product of unit less delay of a logic gate, d, and the delay unit that characterizes a given process [2, 3]:

$$d_{abs} = (d\tau) \quad (1)$$

Where, $\tau$ is technology independent parameter. The delay in logic is expressed as sum of two components, a fixed part called the parasitic delay, p, and second part defined as the effort delay, f, is proportional to the load on the gate's output. The total delay, measured in units of $\tau$, is the sum of the effort and parasitic delays. So

$$d = f + p \quad (2)$$

The parasitic delay of a logic gate is independent of the size of the logic gate and of the load capacitance. Effort delay is dependent on load and properties of logic gate driving that load. The effort delay of the logic gate is the product of these two factors.

$$f = g.h \quad (3)$$

Where g is Logical Effort and h is electrical effort. The Logical Effort represents how much worse the gate is producing output current as compared to inverter. It is independent of the size of the transistors in the circuit. Electrical effort is ratio of input and output capacitances. Thus combining equations 2 and 3, basic equation that models the delay through a single logic gate, in units of $\tau$ is:

$$d = gh + p \quad (4)$$

The backbone of logical theory is the calculation of Logical Effort (g). Iit is the ratio input capacitance of the gate to that of inverter that delivers same output current [4, 5, 6].

$$g = C_i/C_{inv} \quad (5)$$

Where Ci is the input capacitance of the logic gate and Cinv is capacitance of the reference inverter. The delay model of a single logic gate, as represented in equation 4, is a simple linear relationship as shown in Figure. 1.

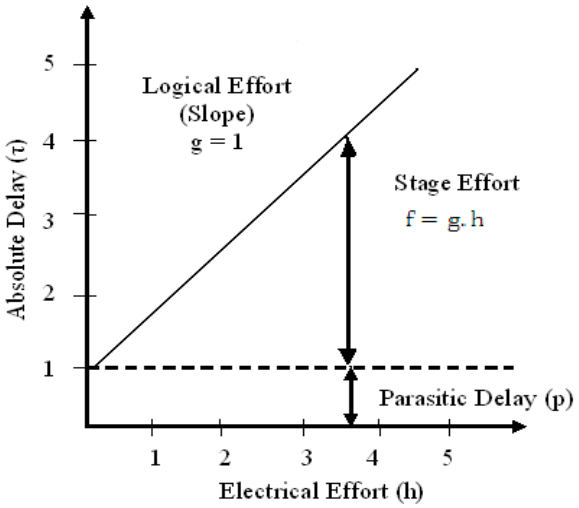


**Fig 1: Graphical representation of delay model**

Logical Effort also introduces branching to allow for the analysis of multi path circuits.

For proper understanding and further reading the reader should be familiar with the LE Delay model [7, 8, 9]. Logical Effort tells us that the delay of a path of logic is minimized when the path effort is distributed equally over all gates in the path. This state occurs when

$$\hat{f} = F^{1/N} \quad (6)$$

In such a case, delay of the path will be equal to:

$$\hat{D} = NF^{1/N} + P \quad (7)$$

## 3. HETEROGENEOUS ADDER

The architecture of a heterogeneous adder includes different types of adder implementations. 32-bit heterogeneous adder proposed in this work consists of four sub adders (SA), 8-bit carry look-ahead adder, 8-bit carry skip adder, 8-bit carry select adder and 8-bit ripple carry adder [10, 11].

Bit size selection for each sub-adder can be done on the basis of requirements (i.e. Area, Speed and Power constraints) of particular application where the design is to be implemented. For example, ripple carry adder cover small area and less power consumption but at the cost of large operation delay whereas carry skip adder gives high speed of operation but at the cost of large area. Therefore in order to optimize adder design as per requirement, 32-bit heterogeneous adder is designed as shown in Figure. 2.

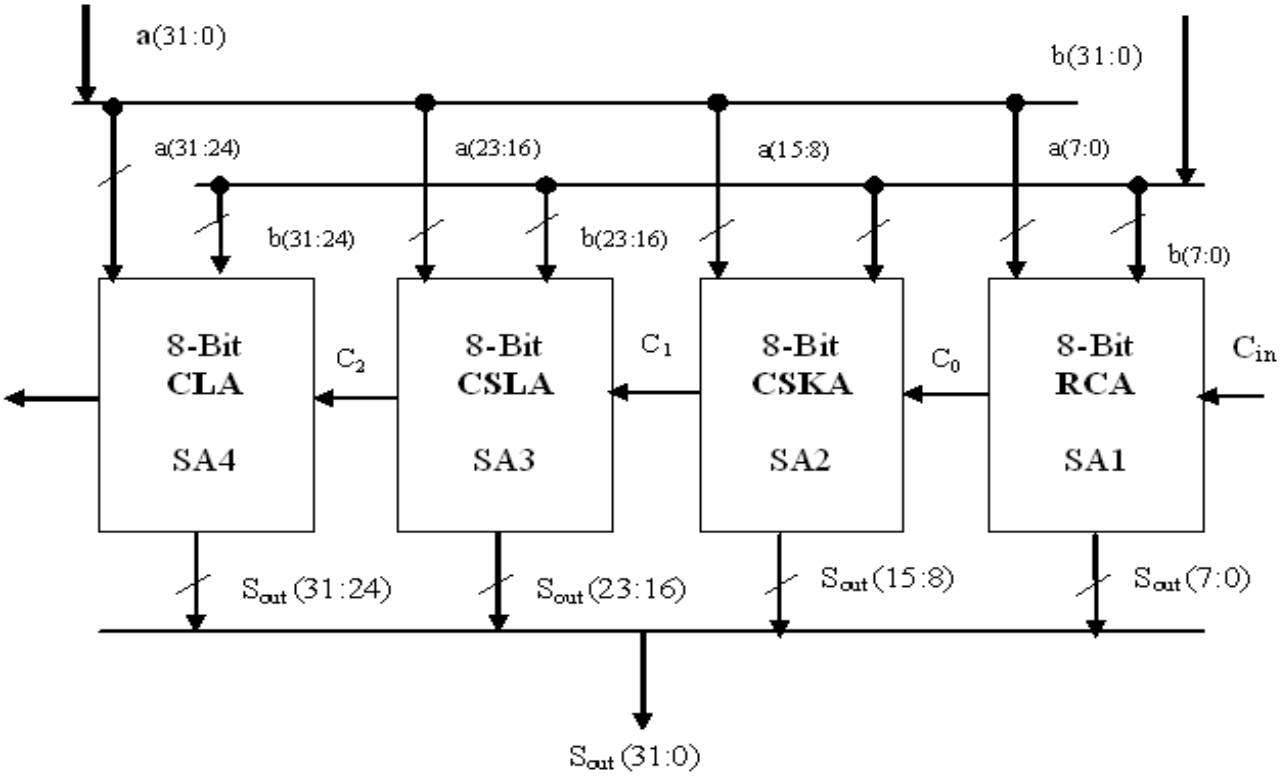


**Fig 2: 32-bit heterogeneous adder architecture**

## 4. SIMULATION RESULTS

The original Logical Effort model has been studied and tested on 32-bit adder architecture using 180nm and 90nm CMOS technologies. The simulation results shows that the LE delay model exceeds the original model on delay accuracy for 32-bit heterogeneous adder as shown in Table 1. Delay plot is shown in Figure 3.

**Table 1. Delay for 32- bit heterogeneous adder before and after optimization using logical effort.**

| CMOS Technology Node | Delay without using Logical Effort (ns) | Delay using Logical Effort (ns) |
|---|---|---|
| 180nm | 18.512 | 13.705 |
| 90nm | 18.109 | 13.584 |

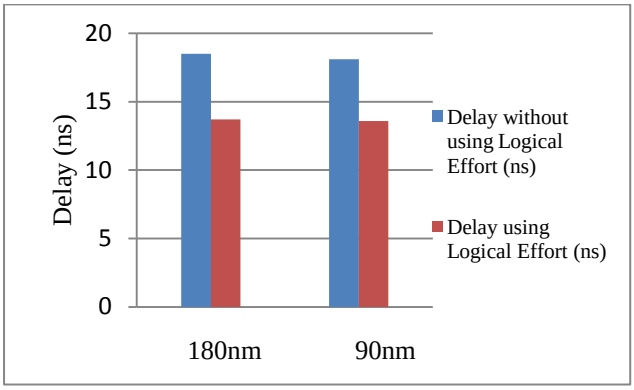


**Fig 3: Delay plot for 32-bit heterogeneous adder**

## 5. CONCLUSION AND FUTURE WORK

In this work use of Logical Effort delay model for performance comparison of 32-bit heterogeneous adder architecture was presented. It has a significant role in the processor to perform the faster arithmetical calculations. Simulation results shows that delay after implementation of Logical Effort theory is improved by 25% for 180nm and 23% for 90nm CMOS Technology.

This work can be extended to optimize power consumption in the adder circuit using the same theory.

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