Performance Comparison of Mesh and Folded Torus Network under Broadcasting, using Distance Vector Routing Algorithm

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ABSTRACT
In the modern technology of communication architecture, network on chip is widely used as communication architecture. Network on chip topologies are becoming a backbone of communication architectures. Network on chip provides a good integration of huge amount of storage on chip blocks as well as computational also. Network on chip handled the unfavorable conditions and it provides the scalability to the architecture. Mesh and folded torus architectures are most commonly used architecture for network on chip communication. Here, we compare the performance of Mesh and Folded torus network architecture on chip, on the basis of different parameters under broadcasting with the help of distance vector routing algorithm. To evaluate the performance of Mesh and folded torus network on chip in the simulation environment, we use the network simulator (NS-2) in the Linux platform.

Keywords
Network on chip, Performance, Mesh, Folded Torus, Latency.

1. INTRODUCTION
With the increasing the complexity of communication architecture and growing the demand of integration of computational and storage blocks on a single chip, the interest of researchers in this area, developed globally. Since it is a challenge to improve the system performance with limited area and power limitations [1, 2]. Besides the design specific routing, exchange the information through routing the packets in the network based on new age technology of networks, the scalability issues as well as reuse of design, make network on chips is worn as favorable than traditional architecture [3].

Many researchers are developing the research area as part concepts from the area of parallel computing and networks to sphere domain of VLSI. It is seems like imagination due to Network on chip and traditional networks are two different circumstances with conflicts in reference of requirements. Traditional networks are distinct from storage on chip due to non determinism and closeness. The design methodology of network on chip is found in [4, 5 and 6]. A decisive factor of chip, in on chip network topology, in term of some quality parameters are cost and energy consumptions as well as whole performance. After review of the different network topologies we find that there are grid based arrangement and match the VLSI design. Since network on chip is commonly used mesh and torus topologies to establish a network on chip architecture for communication [7, 8 and 9].

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There are different network on chip topologies has been proposed such as Mesh, Torus, Star, Octagon, SPIN, Folded Torus [10, 9, 11, 12, 13 and 14]. Torus topology is reduced the latency of mesh. The problem of excessive delay in torus topology is avoided in folded torus topology [15]. From the literature, mesh and torus topologies has given more attention of researchers for network on chip. In this paper, we compare the performance of mesh and folded torus topologies under broadcasting using distance vector routing algorithm in reference of different decisive parameters.

This paper has been organized as follows **Introduction** has been given in **section 1**. **Section 2** represents **related works**. **System model** is given in **section 3**. **Section 4** represents the results and discussion. Finally **conclusion and future work** is given in **section 5**.

2. RELATED WORK
Improving the performance of interconnection network is essential to success to increase the number of processing cores on a single chip. It is requires to increase the processing of data and communication. Although high communication performance requirements of many core processor can meet through asymmetrical topologies and it is suited for different variety of traffic patterns. Two topologies like torus named as xtorus and xxtorus, evaluate the performance on the basis of theoretical analysis, link entropy and path diversity and heterogeneous link design also as well as take the advantages of higher level of VLSI process [16]. A torus based hierarchical hybrid optical-electronic network on chip (THOE) and different techniques as optimization of floor plan, power control mechanism, low latency control protocols and hybrid optical-electrical routers and interconnects, hierarchical in nature is described and compare THOE with torus based optical network on chip as well as torus based electronic network on chip [17]. On chip networks faults, degrade their performance in communication and other parameters of works. A Markov model based analysis for terminal reliability of mesh and 2D torus is proposed in [18]. An analytical performance model using adaptive wormhole routing for n-D mesh topology is described in [19].

Mesh Topology is the most popular inter-processor communication networks which is used in current parallel supercomputers. Several approaches to optimize the power

efficiency by reducing the number of waveguide crossing point of optical network on chip in the floor plan. The floor plans of optical network on chip for 2D mesh and torus topology and design metrics for mesh as well as torus based optical network on chip is given in [20]. A highly scalable with fault tolerant interconnection networks of 6-D mesh/torus topology for large scale supercomputers architectures is discussed in [21]. Zigzag and simple mapping function of embedding mesh and torus topology on to degree four chordal rings is discussed and topological properties are also investigated in [22].

Mesh and torus network architectures are the most commonly used for network on chip topologies. So the performance of 3D mesh and 3D torus topology is analyzed in [23]. The comparison of hierarchical torus network (HTN) with H3D mesh, mesh and torus topology is given and also evaluate the performance of HTN under common traffic pattern [24]. The single routing node architecture, including packet format, routing and arbitration, routing algorithm and node routing direction, the programming and simulation of proposed architecture are designed [25]. The performance is compared on the basis of packet loss with source routing using different traffic generation mechanism with handshaking for parallel transmission concepts [26].

3. SYSTEM MODEL

We compare the performance of Mesh 3×3 and folded torus 3×3 network architectures or topologies on the basis of different parameters. To perform this task, we use the network simulator (NS-2). The network animator (nam) files of Mesh 3×3 and folded torus 3×3 topologies is given in figure 1 and figure 2.

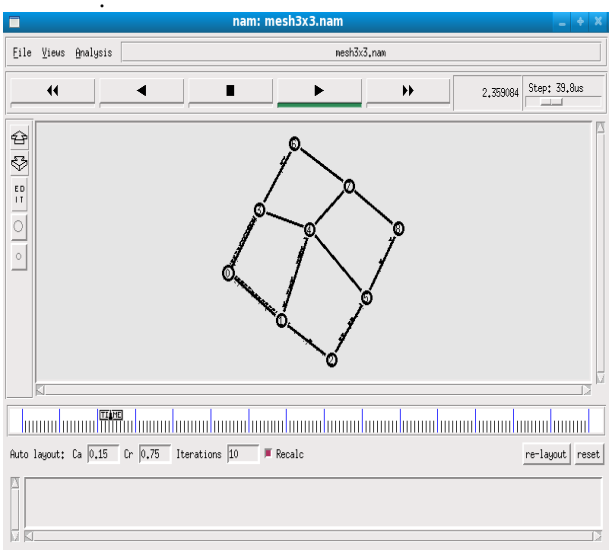


Figure 1: Network animation of Mesh 3×3.

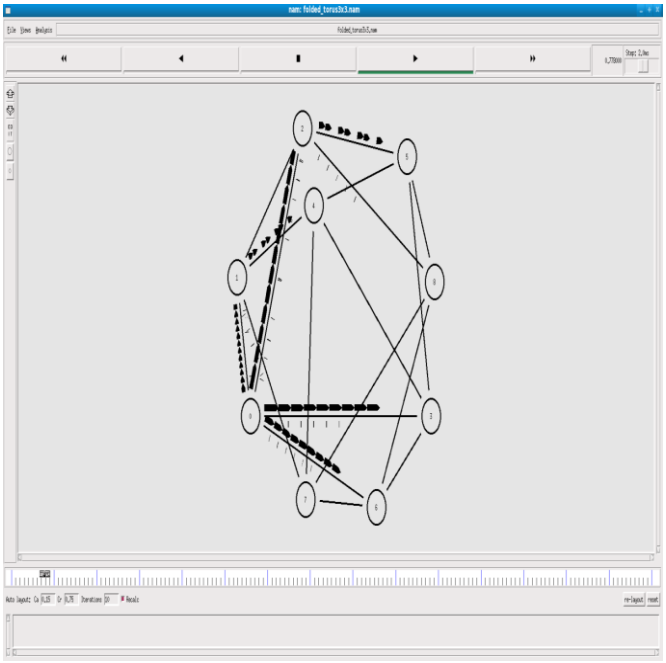


Figure 2: Network animation of folded torus 3×3.

4. RESULT AND DISCUSSION

We compute the results of the nodes of 9, 12, 16, 20, and 25 in mesh and folded torus topologies under distance vector routing algorithm. To compare the performance of two topologies named as mesh 3×3 and folded torus 3×3 on basis of some important parameters such as Throughput, Latency, Dropping Probability, Packet received on the end nodes under broadcasting using NS-2 Simulator.

(a) Throughput:

Throughput can be defined in the different ways, it depends on the basis of implementation. In the present scenario, the throughput can be defined as follows [15]

$$Throughput = \frac{Total\,Completed\,Message * Length\,of\,Message}{Number\,of\,blocks\,of\,IP * Total\,Time} \quad \text{.....(1)}$$

In the above formula, the number of messages arrived at their destination is called total completed message. The number of function IP blocks which in involved in the communication is known as number of block of IP. Length of message is taken in flits. Time is taken in between the occurrences of the first message generation and last message reception. These things have been taken in the program of NS-2 simulator. After execution of program, the simulation results show the comparison of mesh 3×3 and torus 3×3 topologies. The simulation result is in figure 3.

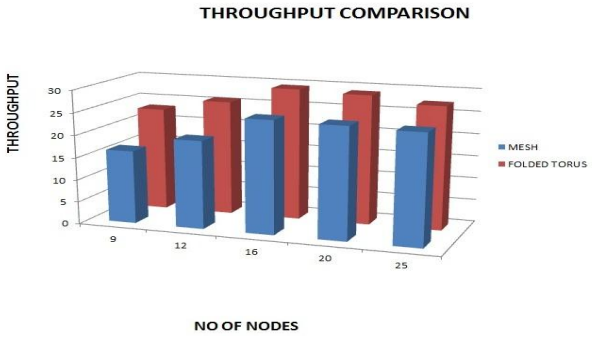


Figure 3: Comparison of Throughput of Mesh and Folded Torus topologies.

(b) Latency:

The time that elapses between the occurrence of a message header injection into the network at the source node, that include the queuing time in source, and the occurrence of the corresponding tail flit reception at the destination node [29] is known as latency. Since we take the transport of nodes in one place to another place, here we called this as transport latency. Simulation results are given in figure 4.

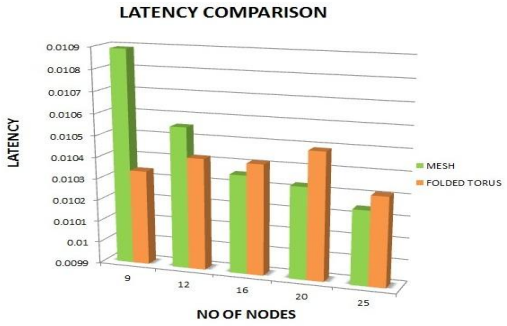
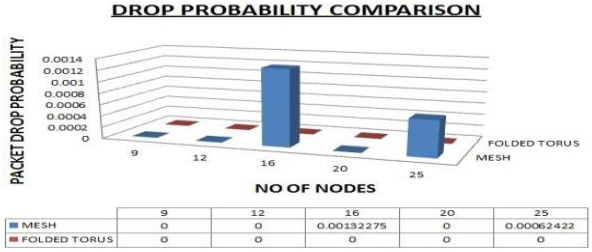


Figure 4: Comparison of Latency of Mesh and Folded Torus topologies.

(c) Dropping Probability:

According to probability theory, we find the dropping probability of packets as total no of packet drop which is divided by total number of dropped packets and total number of received packets at the destination nodes [27]. This may be as follows:

$$Probability\ of\ dropped\ packets = \frac{Total\ number\ of\ dropped\ packets}{Total\ number\ of\ (recieved\ packets + dropped\ packets)\ packets}$$



	9	12	16	20	25
MESH	0	0	0.00132275	0	0.00062422
FOLDED TORUS	0	0	0	0	0

Figure 5: Comparison of packet dropping probability of Mesh and Folded Torus toplogies.

(d) Total packet received on the end-node:

Here, we calculate how many packets are received on the destination nodes in mesh and folded torus topology.

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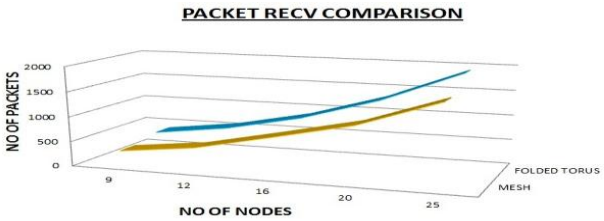

	9	12	16	20	25
MESH	276	443	755	1081	1601
FOLDED TORUS	392	580	884	1328	1927

Figure 6: Comparison of packet received at the end nodes of Mesh and Folded Torus topologies.

5. CONCLUSION AND FUTURE DIRECTIONS

Network on chips have overcome the Storage on chip disadvantages. Mesh and torus are two well-known and universal topologies among many presented Network on chip topologies. We carried out detailed comparisons of mesh and Folded torus topologies for different figures of merit such as latency, throughput, drop probability, packet receive by distance vector routing algorithm using broadcasting.

Torus always has better latency than mesh. However the cost we pay for this improvement is higher power consumption in the case of torus topology so we implemented folded torus topology which has less power consumption because we used less no of links in folded torus as compared to torus and mesh, folded torus has less latency than torus and mesh. Routing algorithms, number of nodes and number of links in a network have a direct effect on power Consumption and latency.

Finally, we selected the folded torus topology which has more throughputs, less latency, less drop probability and its packet receive ratio as compared to mesh. So we conclude that folded torus is better than mesh topology under broadcasting model using distance vector routing algorithm. For future work, the comparison between mesh and folded torus under different type of casting (broadcasting, multicasting etc.) in different scenario using other popular and efficient algorithms can be done.

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