Effects of Transistor Sizing on the Performance of PIFA and Low Noise Amplifier Co-Design

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ABSTRACT
The attributes of transistors such as length, width or oxide thickness are being scaled down when integrated circuits are fabricated. This process variation becomes important at smaller process nodes as the variation becomes a larger percentage of the full length or width of the device. This transistor sizing causes measurable and predictable variance in the output performance of all circuits. In this work, PIFA antenna with LNA co-design has been implemented using two different technologies. First technology used, is the industry standard 180-nm CMOS-based technology family which includes both high-speed analog radio frequency (RF) CMOS and leading-edge silicon germanium (SiGe) BiCMOS technologies. Second technology used is 45-nm CMOS-based technology which implements transistors with dimensions of 120nm.The PIFA is designed to be used in low GHz Smart Dust Wireless Sensor Network, where no conventional Electrically Small Antennas (ESA) can be applied directly. The reflection co- efficients, noise figure and noise sensitivity have been calculated for the design using both the technologies. The variation in the performance of the circuit and the benefits of transistor sizing has been discussed with simulated results.

Keywords
SDWSN, LNA, PIFA, ESA

1. INTRODUCTION
Smart Dust WSN (SDWSN) is one of the important members of Wireless Sensor Networks (WSNs). SDWSNs require highly integrated solutions because they comprise of a large number of nodes. In this paper, work in the area of low volume, power efficient antennas with low noise amplifiers has been done and the variation in the performance of the circuit and the benefits of transistor sizing has been seen.

2. PLANAR INVERTED F ANTENNA
PIFA is a combination of the inverted F antenna and the patch antenna. It has a wider bandwidth due to the radiating patch. The equivalent circuit comprises of inductance L1, capacitance C1 and conductance G1. N1 represents the electromagnetic coupling.

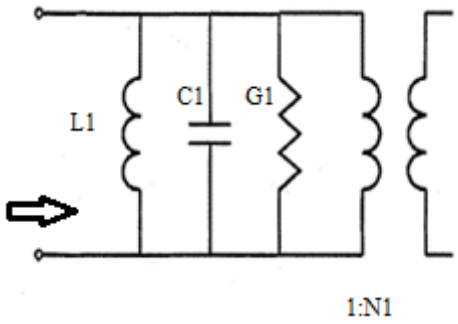

Fig 1: Circuit Model of PIFA[11]

3. LOW NOISE AMPLIFIER (LNA)
It is the initial stage of almost all the receiver architectures. It decides the noise level of the system. LNA consumes power to suppress noise and provide gain and linearity. So, active and passive component optimization techniques are employed to develop an efficient high voltage gain cascade LNA.

4. ANTENNA AND LNA CO-DESIGN
The input matching network of the LNA provides optimum admittance without introducing any extra noise sources in the input signal path, ideally. The bonding wires and the bonding pads appearing at the antenna-LNA interface are also included in the co-design when the antenna and the LNA are integrated. This co-design increases the antenna and system integration and saves chip area. Two circuits have been co-designed in this work using 120 nm and 180 nm technology.

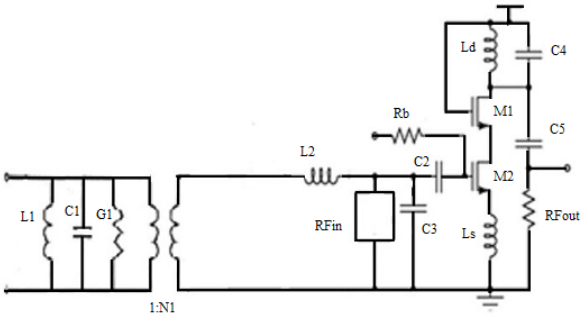

Fig 2: PIFA circuit with co-designed LNA network[10][11]

5. TECHNOLOGY USED
Two technologies have been used in this work. Industry standard 180-nm CMOS-based technology family includes both high-speed analog radio frequency (RF) CMOS and

leading-edge silicon germanium (SiGe) BiCMOS technologies. This was the first technology using a gate length shorter than that of light used for lithography.

Second technology used is 45-nm CMOS-based technology to implement transistors with dimension of 120nm.Process variation is the naturally occurring variation in the attributes of transistors (length, widths, oxide thickness) when integrated circuits are fabricated. It becomes particularly important at smaller process nodes (<65 nm) as the variation becomes a larger percentage of the full length or width of the device and as feature sizes approach the fundamental dimensions such as the size of atoms and the wavelength of usable light for patterning lithography masks. Process variation causes measurable and predictable variance in the output performance of all circuits but particularly analog circuits due to mismatch.

6. SIMULATION AND RESULTS

This schematic has been realized on CADENCE tool-VIRTUOSO which shows the co-design of PIFA with a low noise amplifier. The inductance of the transmission line has been incorporated as well. Through the analysis, the plots were obtained ,which show the value of noise figure, noise sensitivity factor and s-parameters over the frequency range of 1.25 Ghz to 3Ghz. Then the output parameters are analyzed and the noise and reflection co-efficients are determined.

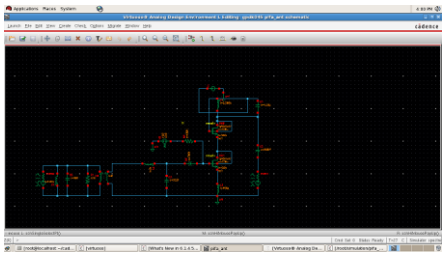

Fig 3:Schematic of PIFA- LNA Co-Design

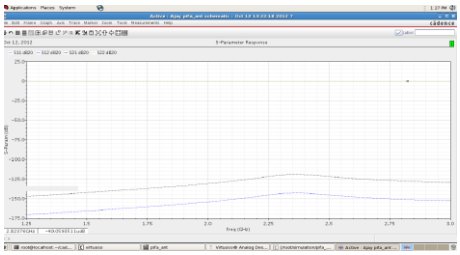

Fig 4: s-parameters of PIFA

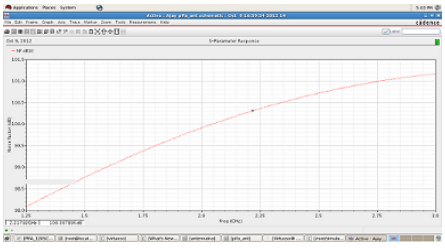

Fig 5: NF of PIFA

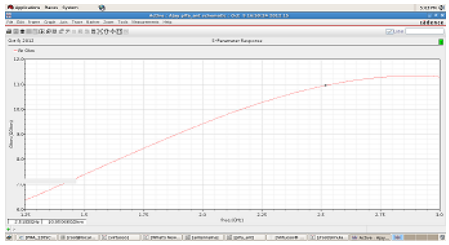

Fig 6: Rn of PIFA

Through this design implemented using 180nm technology, low noise figure and R_n obtained leads to less effect of noise. However the noise figure is not sufficiently low over the desired frequency range. To obtain better results transistor sizing was used.

PIFA antenna with LNA co-design using 45 nm technology to view the effect of transistor sizing on the output of a design was designed. The same circuit is designed with smaller transistors to improve the performance of the design. Through the analysis the plots were obtained, which show the value of noise figure, noise sensitivity factor and s-parameters over the frequency range of 1.25 GHz to 3 GHz.

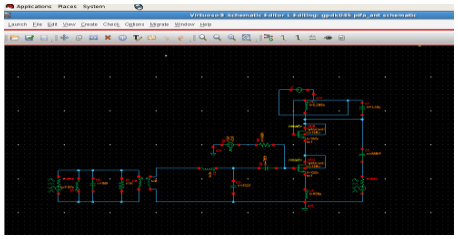

Fig 7: Schematic of PIFA-LNA Co-design

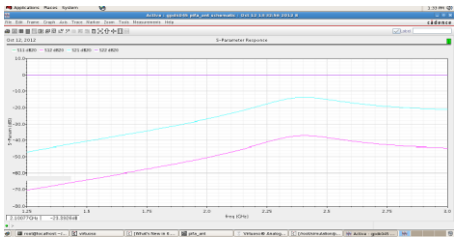

Fig 8: s-parameters of PIFA

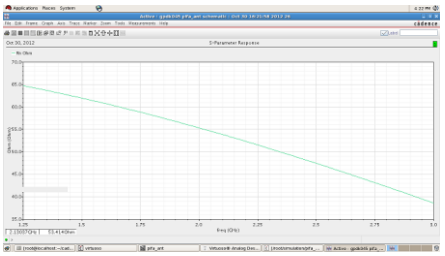

Fig 9: Rn of PIFA

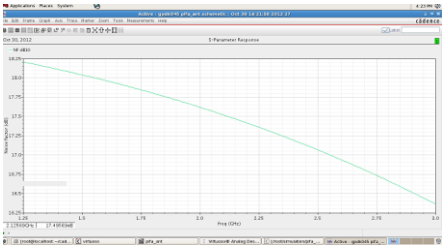

Fig.10. NF of PIFA

NF approaches NF_{min} over the desired frequency range. This design has an extremely low NF. Another advantage of this design is that R_n around the operation frequency is very low. This design is robust to noise due to this low R_n, which enables the low noise amplifier to function properly across all the process variations.

Table 1. Comparison table

Parameters	PIFA(180nm)	PIFA(120nm)
$s_{11(max)}$	-211.9214ndb at 1.25069GHz	-32.12udb at 1.25206GHz
$s_{11(min)}$	-246.4177udb at 2.37GHz	-57.826mdb at 2.405GHz
$s_{12(max)}$	-142.673db at 2.37GHz	-36.905db at 2.4011GHz
$s_{12(min)}$	-170.598db at 1.25188GHz	-70.275db at 1.25069GHz
$s_{21(max)}$	-119.228db at 2.36475GHz	-13.45307db at 2.4007GHz
$s_{21(min)}$	-147.099db at 1.25307GHz	-46.82116db at 1.25069GHz
$s_{22(max)}$	-21.4867mdb at 1.25105GHz	24.161mdb at 1.25651GHz
$s_{22(min)}$	-22.16mdb at 3GHz	-44.02mdb at 2.40437GHz
$R_{n(max)}$	11.29743GΩ at 3GHz	64.765Ω at 1.25068GHz
$R_{n(min)}$	6.397957GΩ at 1.25612GHz	38.617Ω at 3GHz
$NF_{(max)}$	101.167811db at 2.99754GHz	18.20973db at 1.25069GHz
$NF_{(min)}$	98.0917694db at 1.25207GHz	16.36433db at 3GHz

7. CONCLUSION

The plots and the table show the values of the input port reflection co-efficient of 180nm and 120nm technology based PIFA design. The values show that 120 nm technology yields better results for s_{11} parameters. The values of reverse voltage gain are higher when the circuit is designed using 120nm technology. The forward voltage gain obtained is higher for the design using 120nm technology. The values show that the minimum value of output port reflection co-efficient is very low in case of 120nm CMOS design as compared to 180 nm CMOS design. Thus, 120nm CMOS technology gives better result. The values show that the design using 120nm technology is extremely less sensitive to noise as compared to the design using 180nm technology. The noise for PIFA based on 120 nm technology is lower than that of 180 nm. Thus 120nm technology yields better result for noise figure. So, by comparing all the parameters for the two technologies, it has been concluded that miniaturization of transistors improves the performance of the system.

8. REFERENCES

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