Design and Simulation of High Speed, Low Powered ADC for Serial link Receiver

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ABSTRACT

This paper presents design & Simulation of High Speed, Low Powered ADC for Serial link Receiver. This ADC based receiver uses a low gain analog and mixed mode pre-equalizer in conjunction with the non-uniform reference levels for ADC. This combination compensates for both front-end non-ideality and the channel response while maintaining low ADC resolution and hence enables low power consumption. This receiver is based on a low power design of Analog to Digital converter, thus lowering the power consumption of overall system. Tanner tool 13.0 is used for the simulation of the proposed design. From the simulation results it has been observed that the modules used in the proposed ADC lowers the power consumption.

Keyworks-Serial link receiver, digital equalizer, Sequence detector, Analog-to-Digital Converter

1. INTRODUCTION

Implementing serial I/O receivers based on Analog-to-Digital converters (ADCs) and digital post-processing has drawn growing interest with technology scaling, but power consumption remains among key issues for such digital receivers in high speed applications. The wireless communication industry has seen a tremendous growth in last few decades. The ever increasing demand to stay connected at home, work and on move, with data and voice applications, has continued the need for more sophisticated end-user devices. A typical smart communication device these days consists of radio system that can access the mixture of mobile cellular services (GSM,UMTS,etc), indoor wireless broadband services (WLAN-2,11b/g/n), short range and low energy personal communication (Bluetooth), positioning and navigation systems (GPS),etc.

A smart device capable of meeting all such requirements has to be highly flexible and should be able to reconfigure radio transmitters and receivers as and when required. Futher the radio modules used in these kind of devices, should be minimizing the BER as the objective function to maximize the receiver voltage margin. This technique enables near-optimal BER performance and requires almost no additional hardware compared to traditional adaptation approach. In addition the device should be economical in terms of cost and energy requirement. Because of the emergence of no. of companies and their selling competition the cost has been comparatively reduced but the energy power consumption still remains the key issue. A common trend in digital communication has increased the use of digital signal processings. There has been a growing interest in incorporating CMOS Analog-to-Digital converters (ADCs) as frontend of high speed serializes/deserializers (ser/Des) and Electronic Dispersion Compensation (EDC) of optical links.While the speed and resolution are achievable in CMOS technologies, the challenge is achieving low power dissipation so that the I/O links can be integrated in large ASICs.

This paper focuses on the design of a low power ADC module for serial link receiver. The proposed I/O receiver for serial link application contains a low gain Analog Front End (AFE) to pre-shape the signal. The requirement of both high-speed and digital processing is dramatically relaxed which can reduce the power and also maintain thebenefits of digital receiver. This research also introduces an adopted variable-reference for ADC that can compensate for undesired nonlinearity of frontend, mismatch between interleaving paths, and optimally locate the slicing level to maximize the voltage margin for received signal. Furthermore a new adaptation strategy of I/O link equalizer and Clock Data Recovery (CDR) is presented based on minimizing the BER as the objective function to maximize the receiver voltage margin. This technique enables near-optimal BER performance and requires almost no additional hardware compared to traditional adaptation approach.

2. ADC-BASED RECEIVER

In recent years, the applications which use the data rate around 10Gbps, the ADC based receivers have given a good comparable power/ performance. This paper proposes a low-gain mixed-mode or analog mode pre-filtering. This pre-filtering is in conjunction with an ADC –based receiver. With the help of this ADC-based receiver the signal can be pre-shaped and can reduce the amount of digital signal processing in it. This paper has further performed an analysis by how ADC with non-uniform quantization levels can improve performance and power efficiency. The benefits of low-gain Analog Front-End (AFE) are also discussed here.

This paper implements a low power requirement so uses analog Continuous-Time High Pass Filter or a mixed mode approach can also be done. Since a common trend in digital communication has been the increasing use of digital signal processing. The digital signal representation enables greater flexibility and more powerful signal processing techniques to achieve lower BER.

ADC-based receiver has ease of programmability, Extensibility for different channel characteristics and robustness to process variations. But challenges face the adaptation of ADC-based receiver. For ADC resolution number of conversion levels depends on the link characteristics. Design trade-offs and power considerations for ADC architecture in flash-mode, can be employing a large offset tuning range.

In pipeline mode, more highly interleaved designs using pipelined ADC can reach a higher no. of bits for same input capacitance. The reference levels are not fully programmable and hence cannot be used for loop-unrolled architecture.

Design trade-offs and power considerations in concern with timing recovery have some drawbacks:

1. With ISI the phase information has a poor distribution.

2. The binary data are decided after a long latency which dramatically reduce the bandwidth of loop and incur large jitter and less phase tracking.

3.ANALOG AND MIXED-MODE FRONTEND

Any receiver circuitry, which is meant for low gain and high-loss serial link application usually, adopts simple frontend circuitry. This simple frontend circuitry is use to perform pre-filtering. A Continuous-Time Linear Equalizer (CTLE) a very common building block for receiver pre-filtering, in a mixed mode receiver [5].

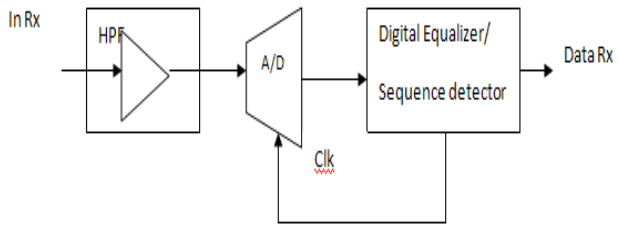

Figure 1: General ADC-based receiver

Figure 1 shows a general ADC-based receiver architecture which comprises of a HPF/FIR filter whose input in turn is fed to digital equalizer/sequence detector.

A CTLE performs basically two main functions; it contains variable DC gain to adjust received signal swing and variable high frequency boosting to provide equalization. This CTLE block is used to pre-shape the signal. Also sometimes a variable gain amplifier is used to adjust signal swing. This adjustment of signal swing would properly drive ADC[6].

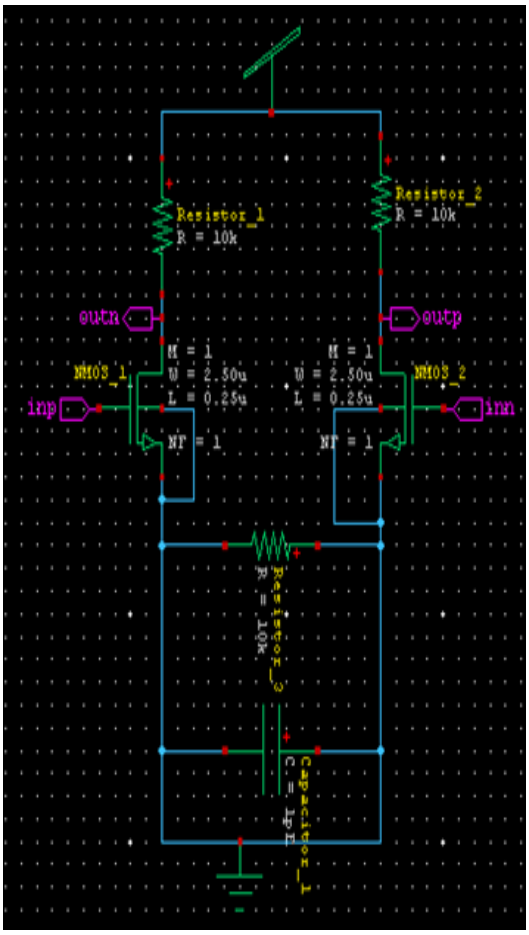

Figure 2. Circuit implementation of HPF

The Figure 2 shows the actual circuit implementation of actual HPF which is required for pre-processing the signal for ADC block. Before being fed to serial link receiver, signal is fed to HPF block, which is a pre-processing block of power optimized serial link receiver. This is the very first component in AFE, which is continuous-time HPF (high pass filter) and it is realized by three CML stages with variable degeneration resistors and capacitors. Here, it has total three stages out of which first two stages are used to provide a wide tunable range of both DC and high frequency boosting. The third stage is used to drive 300 fF loading of interleaved T/H circuitry. The HPF circuitry used here has a great advantage in power consumption i.e. it requires very less power, which is the main aim of proposed paper.

The HPF is to apply power-efficient receiver pre-filtering which consumes only 6 mW in 1.1V supply.

Optional FIR can also be implemented with a little power cost when combined Sample-and –Hold or Track-and -Hold circuit of ADC. By combining HPF and FIR, a good equalization is achieved. Here AFE can perform more than 10dB equalization. The equalization leads to around 1-2 bit saving in the required ADC resolution [7]. As the sampling speeds and input bandwidths are continuously increased, the circuits within the ADC are required to perform faster and maintain certain performance. This becomes difficult to achieve since the performance degrades at high-speeds and affects the dynamic range of ADC.

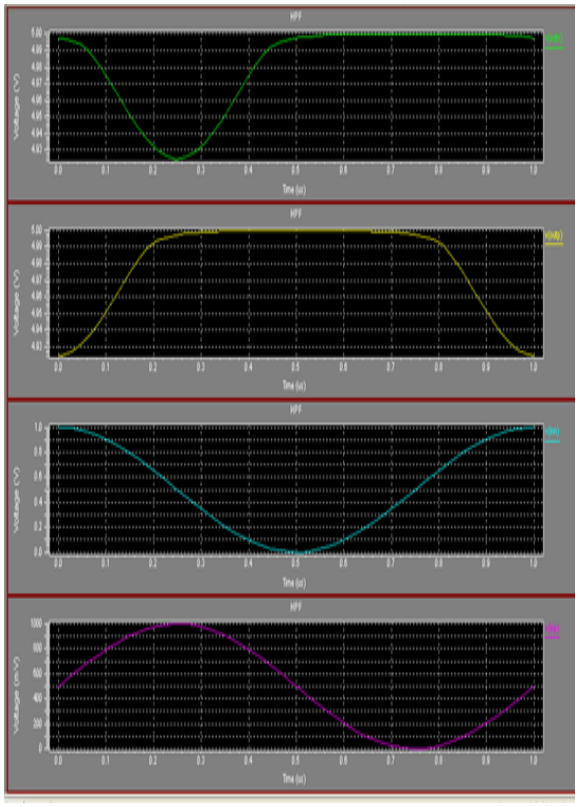

Figure 3: Waveforms for HPF

TABLE 1.Simulation results for HPF

Time(ns)	VinP(V)	VoutP(V)
0.0	0.5	4.93
0.1	0.8	4.95
0.2	1	4.99
0.3	1	5
0.4	0.8	5
0.5	0.5	5
0.9	0.2	4.95

TABLE 2.Simulation results for HPF

Time(ns)	Vinn(V)	Voutn(V)
0.0	1	≈5
0.1	0.8	≈4.98
0.2	≈0.6	4.93
0.3	≈0.3	4.93
0.4	≈0.1	≈4.98
0.5	0	≈5
0.6	0.1	5

Figure 3 represents HPF output. By taking various voltage values and ranges, we can observe that for lower frequencies, the simulation is distorted and not ideal. (For about 100MHz). But as the frequency ranges are increased, the waveforms are nearly ideal. (Passes 500MHz and above). The waveforms are found to be ideal till 1GHz. The waveform shown above gives the simulation results obtained from .sp files in T-spice. These are showing the outputs.

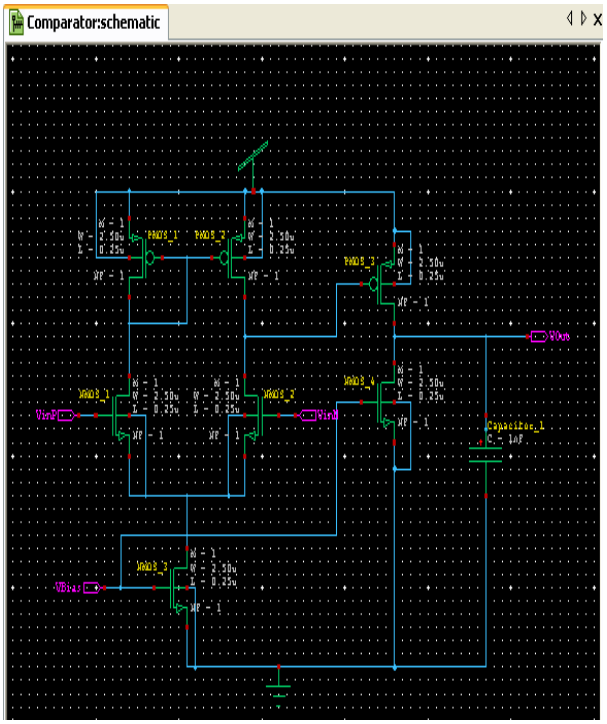

Figure 4: Schematic of comparator

Figure 4 is the schematic of comparator, which is the 2nd module of the proposed design. This module has basically two inputs VinP and VinN. The comparator compares the two input values of VinP and VinN. When input value VinP is greater than VinN, then VOut is less because at the output there is implementation of inverter. Similarly when input VinP is less then VinN the VOut of the comparator is more.

The ADC which is introduced in this paper will be requiring four such comparators if we are using four bit data. So a cascade of four such comparators is the next step of this paper. Then deciding certain threshold values for comparison would be next step. And ultimately combining the whole circuit is last step of the proposed module. Fig.5 shows the simulation results obtained from .sp files in T-spice.

Table 3. Simulation results for Comparator

V(VinP)	**2.40V**
V(VinN)	**2.60V**
V(Vout)	**2.90V**

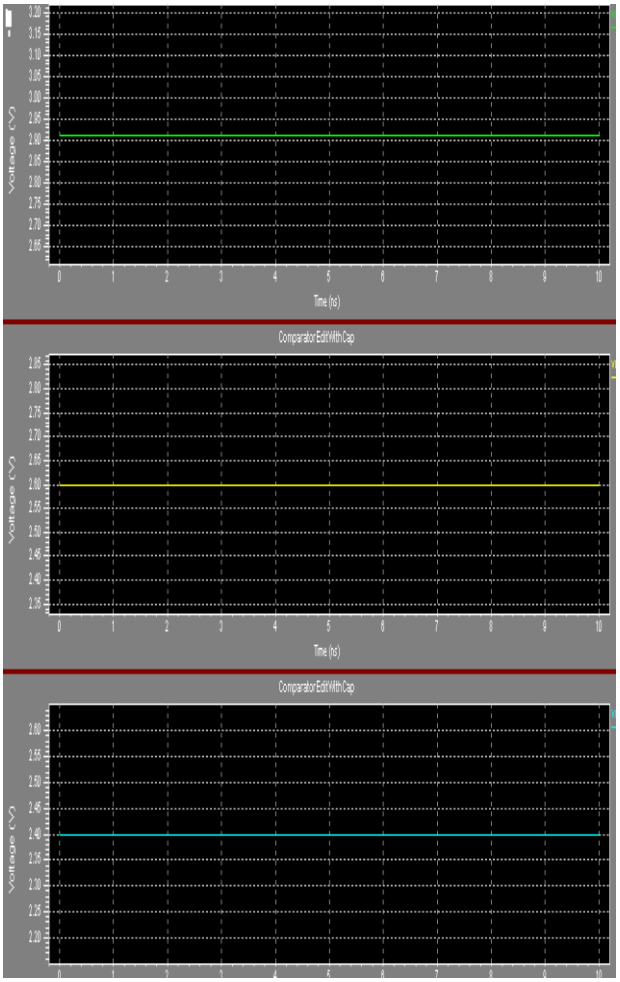

Figure 5: Waveforms for comparator.

4.CONCLUSION

This paper presents design & Simulation of first two modules of High Speed, Low Powered ADC using Tanner tool 13.0 for Serial link Receiver. The two modules has been implemented i.e. the HPF and the comparator for Serial link Receiver. From the simulation results it has been observed that the modules used in the proposed ADC lowers the power consumption.

The work is going on for the combination of comparators and threshold values for High Speed, Low Powered ADC for Serial link Receiver.

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