Design and Simulation of Low Power CMOS Adder Cell at 180nm using Tanner Tool

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ABSTRACT

In this Research Paper, the focus is on the analysis and simulation of the Adder cell which is slightly different as compared to the existing circuits and optimized for Average Power Dissipation. In this paper the adder cell is modified circuit in such a way that it controls the overall capacitances during the Sum and Carry evaluation and will optimize the total capacitance that results in the decrease of the Average Power dissipation. The circuit is characterized by using HSPICE in a 180 nanometer (nm) with supply voltage of 1.8 volt and threshold voltage is 0.40 volts.

Keywords

Full Adder, Tanner Tool, CMOS circuit, VLSI

1. INTRODUCTION

Arithmetic circuits [1], like adders and multipliers, division circuits, are one of the basic components in the arithmetic circuit design of VLSI circuits. Digital ADDERS are the most commonly used components in many digital arithmetic circuit designs that are utilized to implement most of other arithmetic operation. Depending upon the arrangement of the components, there are different types of ADDERS are available in the literature. Particular Adders architecture is chosen based on the application. The power dissipation in adder is a very important issue as it reflects the total power dissipated by the circuit which divided into components like switching power, short circuit power dissipation, and leakage power dissipation. and hence affects the total performance of the device. Most DSP processors incorporate a multiplication unit to implement algorithms such as correlations, convolution, and filtering and frequency analysis these multipliers are made up of adders. All the multipliers which are used in the DSP processors are included different type of Adders. There are many algorithms in the DSP processing where the adder lies in the critical delay path and ultimately determines the performance of the algorithm. The power dissipation of arithmetic operation is of great importance in DSP as well as in the general processors today. Recently, many adder circuits styles have been invented and developed, each having pros and cons in different fields.

2. PREVIOUS FULL ADDER

1. **Damu Radhakrishnan [2]** presented a techniques to reduce the power dissipation in VLSI circuits has been identified as a critical technological advancements and transmission gates appeared in the literature recently. But they were all designed mostly by intuition and cleverness of the designer. Hence they presented formal design procedure for the minimal transistor CMOS XOR-XNOR cell. Their design is fully compensated for threshold voltage drop in MOS transistors. This new cell can reliably operate when the power supply voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. A formal design approach for a full adder cell using the new XOR-XNOR cell is also presented.

2. **Keivan Navi and Omid Kavehei** [3] in February 2008 presented new low power and high performance adder cell using a new design style called using Bridge design style of the MOS transistor. The bridge design style enjoys a high degree of regularity, higher density than conventional CMOS design style as well as lower power consumption, by using named bridge transistors. Their new design style uses some transistors, Named bridge transistors, sharing transistors of different paths to generate new paths from supply lines to circuit outputs They presented the Simulation results by using 90nm technology based on the CMOS circuits. They used HSPICE to verify the circuits and presented the superiority of the resulting of their proposed adder circuits against conventional CMOS 1-bit full-adder in terms of power and delay. They have done the characterization of their circuits by varying the different voltages supply ranging from 0.65v to 1.5v with 0.05v steps. The main focus of their design work is basically on the power delay product and dynamic power dissipation also they have presented the improvement in th overall delay of the circuit. According to their simulation results on HSPICE EDA tool, 90 nm CMOS process technology at room temperature, and under given conditions, shows the improvements of 41.5%. At the lower voltages (0.65v) there is impressive improvement of the dynamic power dissipation is being presented but static power dissipation is no longer has been shown in this paper.

3. **Ilham Hassoune and Denis Flandre [4]** in 2010 presented a technique in adder to improve the noise margin and also reduction in the average power they basically use optimized level shifter at the output of the adder circuit and also they had used low power XOR and XNOR circuits to optimize the whole adder circuits however they have shown that their circuit also need complement and original input of the input signal which somewhat increases the area of the silicon chip.

4. **Monico Linares-Aranda and Mariano Aguirre-Hernandez [5]** they present a paper in 2011 and investigated two techniques of high-performance and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). They have done the comparison among other full-adders available in the literature and reported is having a low PDP, in terms of speed, power consumption and area. All the full-adders were designed with a 0.18micro-meter CMOS technology. They have deeply examined the full adder truth table and found that when C = 0 then SUM is equal to the A XOR B and when C = 1 then SUM is equal to A XNOR B Thus, a multiplexer can be used to obtain the respective value taking the input C as the selection signal. Following the same criteria, the carry is also evaluate in the

same way as when C = 0 then carry is equal to (A AND B) and when the signal C =1 then carry is equal to A OR B. in this way C is basically used as a select line of the MUX in their design. So they have designed the ADDER cell based on the above observation and use the multiplexer to select the different things.

3. METHODOLOGY

The approach in this paper is adopted to modify small things in the Adder cell and then compare this cell to the latest cell in the literature. The circuit of adder which is presented [5] uses one XOR gate and one XNOR gate which is shown in the fig 1

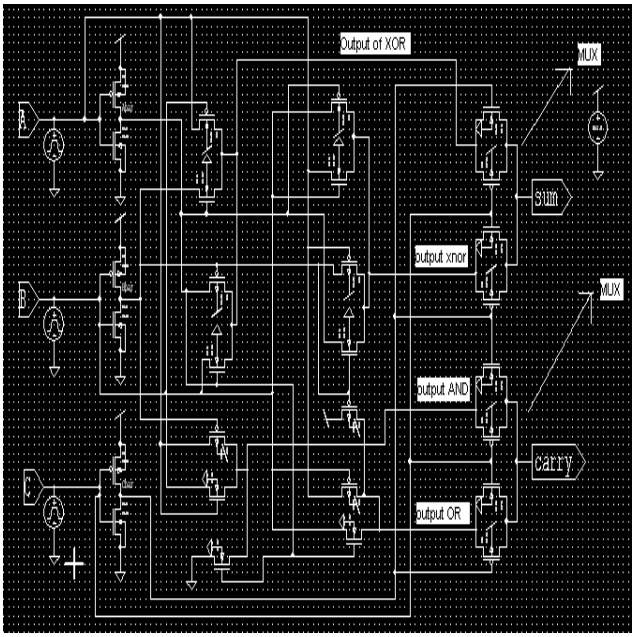


Figure 1: Low Power Adder Cell by Using Mux

In fig 1 it is clear that this adder architecture [5] uses the MUXES to select the particular outputs from the XOR, XNOR, AND and OR. In this way the two inputs will pass through the critical path of the circuit and the third input will just use the select lines of the mux which is shown in the fig 1 in this way this circuit is having a delay optimized as compare to the basic adder. This circuit uses 28 transistors which is same as the basic adder cell but further improvement is possible as shown in the fig 2

The schematic of the modified adder cell is shown in the fig 2 here one modification is in the design of AND gate and the other modification is in the inclusion of the not gate instead of the XNOR gate which is shown in the fig 2 these two modification results out a better result of the power dissipation

This type of circuit arrangement is giving the same output which we were getting from the previous circuit but transistor count is 27 instead of 28 which was the case of the previous design so it consume lesser silicon area. This will further increase reliability of the circuits because reliability is directly proportional to the total silicon area.

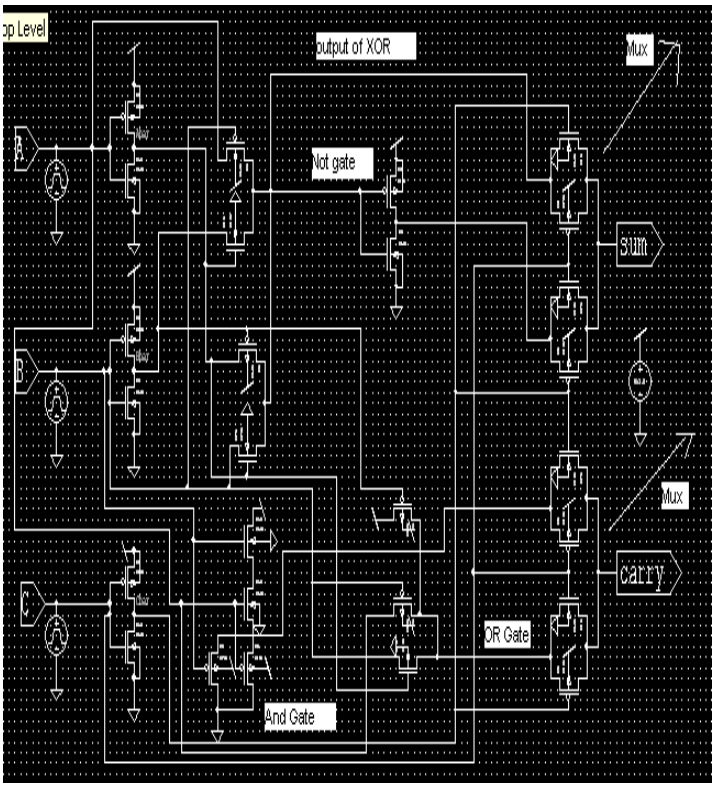


Figure 2: Modified Adder Cell

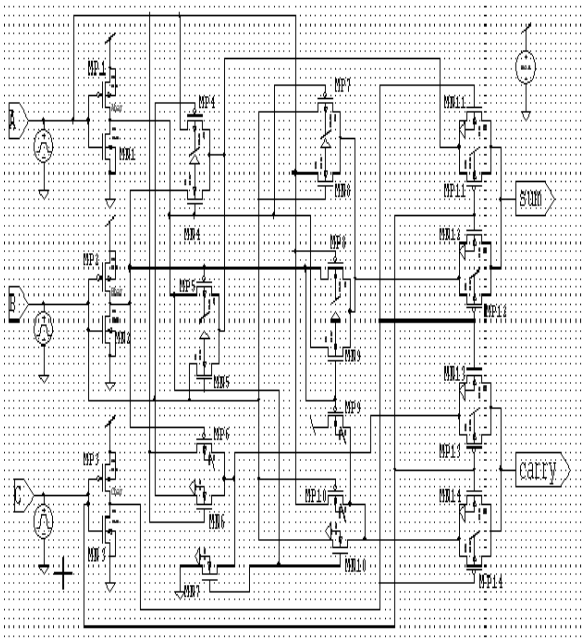
The basic advantages of this new logic structure adder are as follows.

1. No signals internally generated that control the selection of the output multiplexers. Instead, the C which is the input signal having a full voltage swing and no extra delay, is used to drive the multiplexers, it also reduces the overall propagation delays because signal doesn't pass through the capacitance of the drain and source.

2. The capacitive load for the C input has been reduced, as it is connected to a few transistor gates and no longer to some drain or source terminals, so it is used where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall propagation delay for larger modules where the C signal falls on the critical path can be reduced. And if this adder structure is to be connected into the big multipliers then it further reduces delays in multiplier.

3. The propagation delay for the SUM and CARRY outputs can be tuned up individually by adjusting the XOR and XNOR and the AND and OR gates, this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications. Besides this lesser power dissipation and the delay is also the basic advantages which we are getting from this new architecture.

4. W/L ration



One of the important design criteria in the VLSI design is the W/L ratio of each and every MOS transistor used in the circuits because it is the only design parameter which can control all the parameter of the design carefully selection of the W/L ratio of each transistor can help the optimization of the circuits in this paper L is fixed for all the MOS transistor that is 180nm to get the maximum speed this is taken as small as possible here in this paper W is somewhat different for different transistor it is varied by using the analysis of simulation and then it is fixed when the output results gets satisfactory. The W of the Base adder cell is given as here

MP = PMOS transistor and MN = NMOS transistor

MP1 = MP3 =MP6 =6u

MP2 =6u

MP4 = 4u

MP9=1u

MP9 = MP13 =MP14 = 3u

MP6=MP7 = 1u

MP8=MP9= 8u

MP10=1u

MP11=MP12=MP13=MP14 = 10u

And Width of the NMOS transistor is given as

MN1 = MN3 = 3u

MN2 =MN4= 2u

MN1 = 1u

MN6 = 4u

MN11= MN12= MN13= MN14=6u

MN10=0.5u

MN7 =MN8=MN9=5u

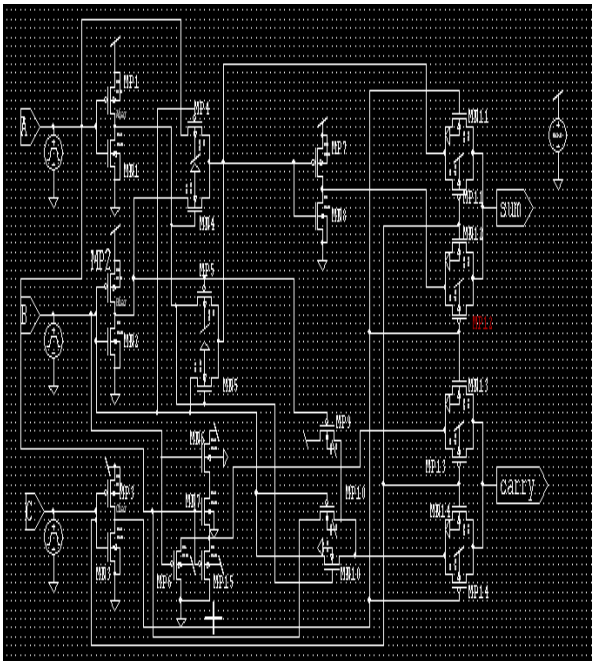


Figure 3: W/L ratio of the Modified Adder Cell

The W of the Modified Low power adder cell is given as here

MP = PMOS transistor and MN = NMOS transistor

MP1 = MP3 =MP6 =3u

MP2 = MP5 = MP11=MP12=6u

MP4 = MP9=1u

MP9 = MP10 = MP13 =MP14 = 3u

MP7 = 10u

MP15= 8u

And Width of the NMOS transistor is given as

MN1 = MN3 = MN6 = 1.5u

MN2 =MN8= 5u

MN4 = MN5=MN10= MN11= MN12= MN13= MN14=0.5u

MN7 = 2.5

5. RESULTS

We compare the performance of Full Adder [5] with the modified Full Adder. For the purpose of Modified ADDER cell designs 180nm technology, TANNER tool [6][7] as well as MICROWIND tool[8] is used. The performance of both Adder Cells is compared in terms of Average power dissipation.

5.1 Average Power Dissipation

Table 2 shows the Average Power Dissipation of base Adder and Modified Adder.

Table 1 Average Power Dissipation

Type of adder	Average power dissipation
Adder in base paper	681uw
Modified adder	550uw

Above results shows that modified adder cell consume 23% less average power as compared to the base adder cell

6. PHYSICAL LAYOUT

The physical layout [9] design of different MOS transistor of ADDER is designed in MICROWIND Tool. The MICROWIND program design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. And area of both the adder cell is then estimate from the Layout which is given in the section below: --

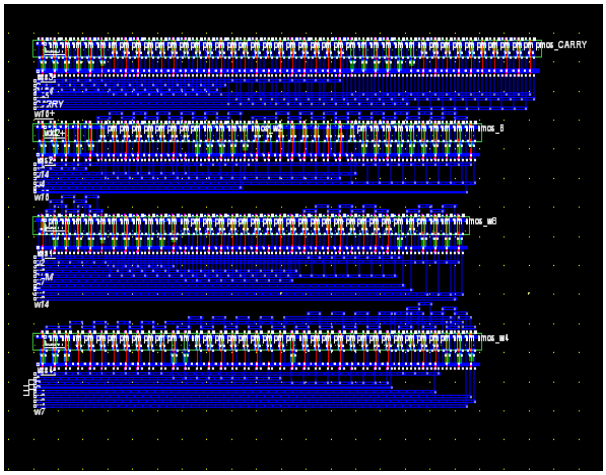


Figure 4 Layout of Base Adder

Fig 4 above shows the layout of the adder cell in the base paper designed in the MICROWIND tool and the area of this layout is 2349 micro meter square.

The fig 5 shows that the area of the modified adder cell is 2100.5 micro meter square which is approximately 10% lesser than the adder in the base cell so in this way new modified adder cell while consuming lesser power and also consume 10% lesser silicon area.

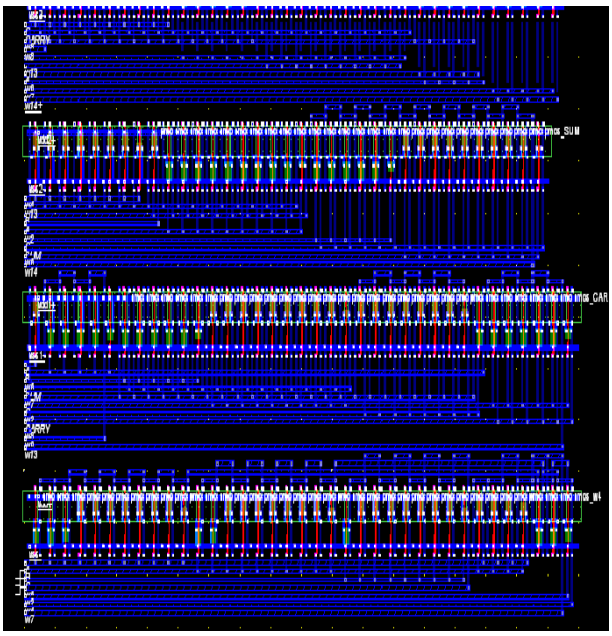


Figure 5: Layout of Modified Adder Cell

7. CONCLUSION

Focus of this Paper was mainly on low power and high performance CMOS based full adder design. It reduces Average Power Dissipation approximately 23% as compared to the base cell adder in the base paper. It also presents an area efficient approach to low power, because transistor is having a lesser width requirement so overall silicon area is also lesser as compared the base adder cell.

CMOS based full adder was designed in Tanner EDA tool using 180nm technology and analysis of dynamic power dissipation and delay was done in T-spice and Layout design was done in MICROWIND EDA tool and also area analysis is performed in MICROWIND EDA tool.

8. FUTURE SCOPE

As a future scope of the work, Power of the circuit can be further reduced like if someone optimize the leakage power and also short circuit power dissipation in the circuit can be reduce which can be the future work of this paper. Also, there is one important modification can be done in noise margin which is lesser in this new modified designed of the adder one can extend the work for improving the noise margin of the circuit so that this adder circuit can be used in cascaded system design like multiplier and division circuits

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