Charge Redistribution based 8 bit SAR ADC

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ABSTRACT

An 8-bit 10 MS/s SAR A/D converter is presented. In the circuit design, a capacitor switched D/A Converter architecture, Dynamic latched comparator architecture and low power SAR logic are utilized. Design challenges and considerations are also discussed. This proposed converter is implemented based on 0.29um CMOS logic process. With a 3.3 V analog supply and a 5 V digital supply, the differential and integral nonlinearity are measured to be less than 0.36 LSB and 0.69 LSB respectively. With an input frequency of 625 KHz at 10 MS/s sampling rate and the power dissipation is measured to be 6.62 mW.

Keywords

Analog to Digital Converters (ADC), Digital to Analog Converter (DAC), Successive Approximation Registers (SAR), Comparator, Latch.

1. INTRODUCTION

Analog to Digital Converters (ADCs) are a popular component in nearly all electronic circuits that are used to convert one form of voltage information to another. They are most heavily needed in communications devices, such as cellular phones. One important requirement for such portable devices is low power consumption. One possible ADC configuration which typically yields low power is the Successive Approximation Register (SAR) converter, presented here.

A SAR works by performing a binary search on a given input voltage. That is, it compares the sampled-and-hold Input to a trial voltage and based on the comparison, determines if it was correct or not. The output of the comparison is fed into a SAR control logic (SAR) that determines which half of the current solution space the input is in, and selects the MSB accordingly. The solution space is now halved, and the comparator tries another trial voltage, this process repeats until the voltage is converted to the desired resolution. See Figure 1.

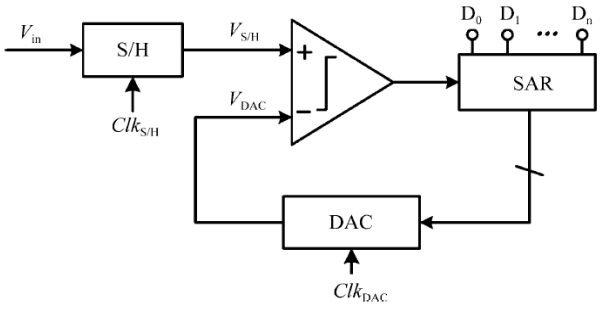

Figure 1: Typical SAR ADC Architecture

The SAR control logic tries an initial guess to begin with, which is then compared to the input voltage via a clocked comparator.

The output of the comparator is fed back into the SAR control logic and tells it whether its initial guess was too high or too low. If VOUT is high, then the trial voltage was too low, so the MSB is set to "1," and the SAR control logic continues on to the next bit. Otherwise, VOUT is low and this means the bit should be set to "0." Operation continues this way until all bits are realized.

The circuit in the above figure is for illustration purposes only; the actual circuit implemented uses switched capacitors. This is for several reasons. First, the capacitors act not only as the DAC but also as the Sample and Hold components. Secondly, the resolution of the ADC will be limited partly by capacitor mismatch, which is quite good in modern CMOS processes. Lastly, it turns out that capacitors lend themselves very nicely to implementing the SAR function.

2. CIRCUIT DESCRIPTION

Our circuit is based largely on a method outlined by Gray and McCreary which uses a binary-weighted switched capacitor array [1]. Fig. 2 corresponds to the following method of operation. This operation is based on the sizing of the capacitors. Whenever a capacitor is switched on in this configuration, all of the capacitors to the right of it add up in parallel to the same value as the switched capacitor. Using this configuration, voltage division can be performed by storing charge on the top plate of the capacitor array.

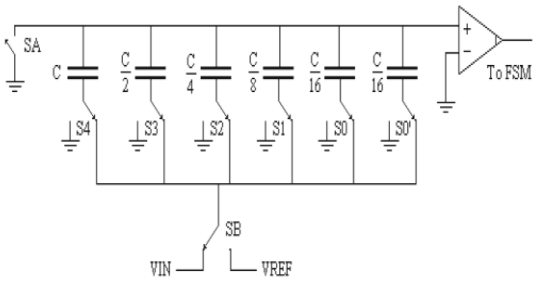

Figure 2: Basic Switched Capacitor DAC (5 bit illustration).

As seen in Fig. 3, during sample mode switch SA is closed and the top plates are connected to V_{REF}. The bottom plates are then connected to V_{IN}, which stores a total charge of $-2C \cdot V_{IN}$ on the capacitors. Then in hold mode (see Fig. 4), switch SA is opened. This causes the top plates to float. All of the switches on the bottom plates are then switched to ground,

which causes the voltage on the top plates to drop to $-V_{IN}$ to conserve charge.

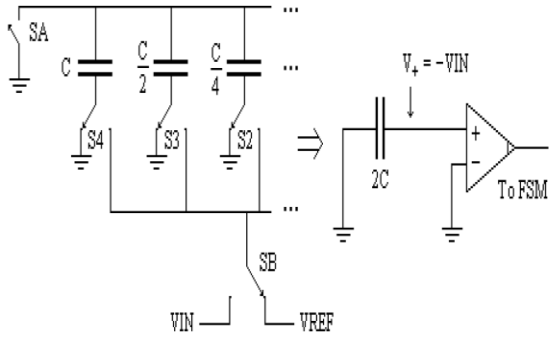

Figure 3: Sample Mode.

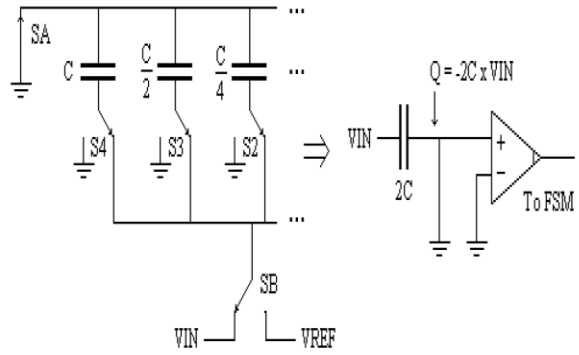

Figure 4: Hold Mode.

The ADC then goes into redistribution mode. During this cycle, the bottom plate of the MSB is switched to V_{REF}., causing the top plate of the capacitor array to rise to $-V_{IN}+V_{REF}/2$. The comparator determines whether this value is above or below 0V. If the estimate was too high, the SAR control logic will open the switch on the MSB. If the estimate was too low, the SAR control logic will keep the MSB switch closed and move on to the MSB-1 switch. This process is repeated for all of the remaining bits. Using this method, the redistribution mode takes *n* clock cycles to resolve *n* bits.

Throughout the design of the ADC, we made several choices to reduce the power consumption as much as possible. For example, we decided to use a single-ended implementation instead of a fully-differential one. This decreased the amount of circuitry needed and hence power decreased by about half. This is also the reason why we did not utilize any offset-cancellation techniques, as they would have increased power consumption. Furthermore, any offset from the comparator will only shift the DC response of our ADC, but will not introduce any non-linearity.

We based our comparator core off of a design by Razavi and Wooley [2]. We chose this design partly because it only uses one clock signal during its operation. This reduces the load on the clock and also eliminates any problems with clock skew that is associated with a dual clock design. Furthermore, this design provides outputs that are strong enough to drive an SR Latch. This reduces the power consumption because some other comparator cores would require buffers to be able to drive the SR Latch. One last benefit that this comparator provides is the fact that the enable transistor completely shields the core from the input during regeneration phase. This will be discussed further in Section III.

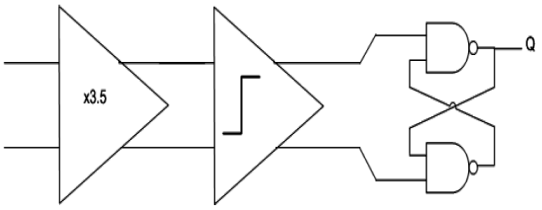

Figure 5: Overall block diagram of our comparator

3. CIRCUIT ANALYSIS

3.1 Comparator Operation

The overall block diagram of our comparator can be seen in Figure 5. The latch-only comparator (Fig 6) is referred to [3] due to its low power configuration. When latch is low, the reset switches M7/M8 and M9/M10 are ON. They pre-charge the output nodes and the drains of the differential pair (M1/M2) to V_{DD}. At the same time M11 is OFF and cut the current path from V_{DD} to ground. During this reset mode, the only time when the comparator consumes power is the moment V_{DD} charges output capacitance.

When latch goes high, the reset switches are cut off. As M11 turn on, the current starts flow in the differential pairs. M3/M5 and M4/M6 constitute cross-coupled inverters. The path which receives more current discharges the output more quickly. When this voltage is lower than V_{THN}, the corresponding gate-connected NMOS is turned off and allows V_{DD} to fully charge its output capacitance. After regeneration is completed, one output is at V_{DD} and the other becomes ground. In this situation, there is no supply current. Therefore, the comparator consumes power only during the regeneration.

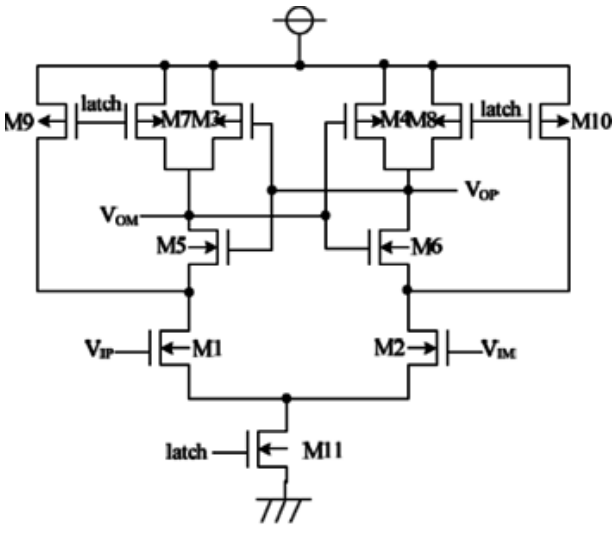

Figure 6: Latched comparator

The transistor sizing is shown in Table 1. Due to the channel modulation effect and large mismatch error for using minimum transistor length, the length of the differential pair is set as three times of the minimum length, and others are two times of it.

Table 1 Design parameters of the dynamic latch comparator

Device	Width	Length	Unit
M1/M2	18	0.26	µm
M3/M4	0.9	0.26	µm
M5/M6	0.45	0.26	µm
M7/M8/M9/M10	0.9	0.26	µm
M11	0.45	0.26	µm

It is important to note that the size of the differential pair (M1/M2) is critical to the comparator's performance. By enlarging the width, the gain is increased, thus improving the resolution. Meanwhile, the input offset mainly caused by transistor mismatch can also be reduced due to its inverse proportion to the multiple of width and length [4]. While the drawback is a larger kickback noise generated due to the parasitic capacitance.

3.2 Isolation Switches

The cross-coupled inverters of the comparator introduce large voltage variations during regeneration (Fig 7). The variations are then coupled to the input voltages through the parasitic capacitance of the input pair. If the proceeding stage doesn't have zero output impedance, it will be disturbed by these variations, thus degrading the accuracy of the ADC. This phenomenon is called kickback noise [5].

To avoid this noise source, an isolation switch is added between the differential pair and the preceding stage. The switch is simply a NMOS transistor with minimum size. It is controlled by the inverse of the latch signal. See Fig 8, when latch goes high, the comparator starts regeneration, and the isolation switches are cut off in order to protect the input signals from disturbance caused by kickback noise.

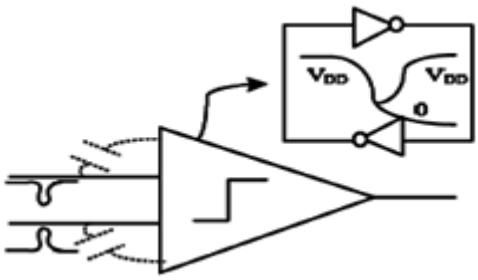

Figure 7: Kickback noise generation

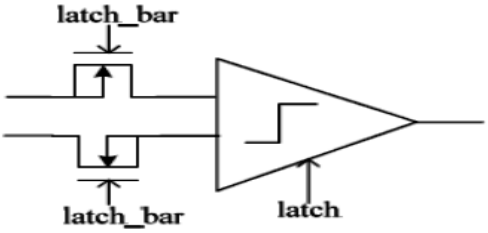

Figure 8: Isolation switch with comparator.

3.3 Output Buffer and SR Latch

The buffer followed the comparator is a simple inverter with minimum size and appropriate P/N ratio. Two cross-coupled NAND gates constitute a SR latch at the final stage, shown in Fig. 9. The SR latch helps to keep the comparison result constant for a whole period of clock cycle. Otherwise the comparator output is always pre-charged to V_{DD} at the reset mode Unnecessary signal level change will consume extra power.

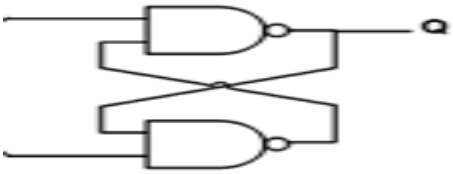

Figure 9: SR latch.

3.4 Successive Approximation Register

The successive approximation register is based on ring counter and shift register presented in [6]. SAR supports three main operations: First, it shifts the initial guess "one" to the right by one bit; secondly, it loads the result from the comparator by the positive triggering of next nearest bit; thirdly, it holds the determined bits. After 9 clocks, SAR outputs a pulse, which means that one whole conversion is completed. The signal EOC in the above figure is generated to indicate the start of the next sampling.

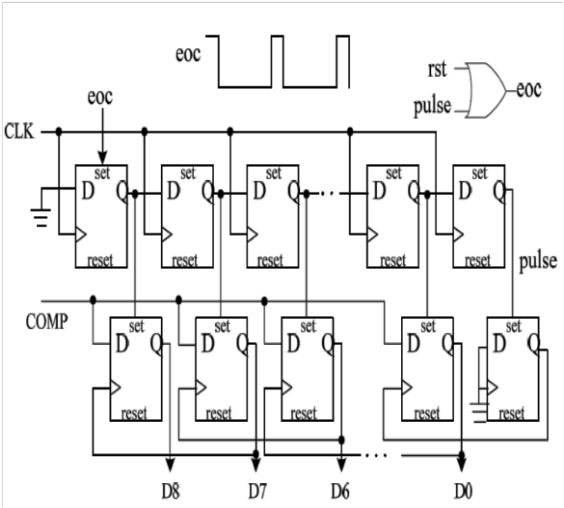

Figure 10: Block diagram of SAR

4. RESULTS

The circuit was implemented and was simulated using cadence; the waveform in Fig. 11 shows the analog signal and corresponding DAC variation, comparator output and the SAR control logic output.

Figure 11 Simulation of Final SAR ADC Block

5. CONCLUSION

A dynamic latch comparator is chosen for its lowest power consumption. However, it generates more kickback noise which deteriorates the input resolution and degrades SNR. To overcome this problem, isolation switches are added before the input stage of comparator, thus keeping the input signals from disturbing by this noise. Moreover, a latch is followed after the comparator to keep the previous output unchanged in the whole clock cycle. Such operation avoids unnecessary charge and save power.

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The non-redundant SAR proposed by Rossi uses less flip-flops, but when this architecture is implemented in this work consumes less power for its more complicated sampling signal generator.

6. REFERENCES

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