A New Three Phase Seven Level Asymmetrical Inverter with Hybrid Carrier and Stepped Reference

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ABSTRACT

This paper presents new hybrid modulation strategies for the chosen three phase seven level Asymmetrical Multi Level Inverter (AMLI) with Stepped reference. Performance indicesused are Total Harmonic Distortion (THD), Form Factor(FF),Crest Factor(CF),Root Mean Square(RMS) value of output voltage and DC bus utilization. The combination of inverted sine carrier and triangular carrier is used as hybrid carrier to produce triggering pulses for the power switches used in the proposed three phase seven level AMLI. This paper also investigates the potential of using hybrid carrier with the existing strategies such as Phase Disposition Pule Width Modulation (PDPWM),Phase Opposition Disposition PWM(PODPWM),Alternate Phase Opposition Disposition PWM(APODPWM)and Variable Frequency PWM (VFPWM) techniques for carrier. The simulation is done in MATLAB/SIMULINK and the results are presented for all modulation strategies. It is observed that hybrid PDPWM provides relatively better DC bus utilization and creates relatively less distortion for m_a=0.7-1

Keywords

CMLI, PWM, THD, PD, POD, APOD, PS, CO, VF, Hybrid Carrier

1. INTRODUCTION

In recent years, multilevel inverters are becoming increasingly popular for high power applications due to their improved harmonic profile and increased power ratings. Various multicarrier pulse width modulation techniques are proposed so far by several researchers. Multi Level Inverter (MLI) topologies can work at higher voltage and higher power than conventional two level converters. In addition, multilevel conversion reduces the output variables harmonic distortion and sometimes, in spite of the devices count increment, the conduction losses can also be decreased by increasing the number of levels. The reduction of harmonic distortion is achieved by increasing the number of levels of output voltage. This will further reduce the switching losses by reducing the inverter carrier frequencies. The harmonic content can also be reduced by using several pulses in each half cycle of output voltage. To reduce even more the switching frequency without degrading output spectrum, slope of the triangular or inverted sine carrier waveforms can be controlled in the modulation strategies such as the Phase Disposition (PD). Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) Variable frequency (VF).The generation of gating signals for turning ON and OFF transistors is usually done by comparing a reference signal with carrier wave. The carrier frequency f_c determines the number of pulses per half cycle. The modulation index (m_a) controls the output voltage. Tolbert et al [1] have derived a procedure to find all sets of switching angles for which the fundamental is produced while the 5^{th} and 7^{th} are eliminated. Sun and Yun [2] have proposed a hybrid PWM method for the new topology that has different cells working in different switching frequencies in order to achieve low switching losses. Palanivel and Dash [3] have developed various carrier based pulse width modulation techniques which can minimise the total harmonic distortion and enhance the output voltage for a five level inverter. Shanthi and Natarajan [4] presented the use of Control Freedom Degree (CFD) combination. The effectiveness of the Pulse Width Modulation (PWM) strategies developed using CFD are demonstrated by simulation. Du et al [5] discussed about the control of seven-level Hybrid Cascaded Multi Level Inverter (HCMLI) with fundamental frequency switching control and how its modulation index (m_a) range can be extended using triplen harmonic compensation. Xiao et al [6] have proposed a strategy to minimize harmonics and achieve zero error tracking. Tolbert et al [7] explored the benefits and discussed control schemes of the cascade inverter for use as an Electric Vehicle (EV) motor drive or a parallel Hybrid Electric Vehicle (HEV) drive and the diode-clamped inverter as a series HEV motor drive. Josh and Jerome [8]have stated that the power quality improvement can be achieved by reducing the harmonics at the output voltage of the inverter. Colak et al [9] have done intensive studies and have proposed carrier based sinusoidal space vector and sigma delta PWM methods in open loop control of inverters. Seyezhai and Mathur [10] have reduced the switching losses and improved the power quality using variable frequency inverted sine PWM strategy. Lau et al [11] have found analytical solutions for determining the spectral characteristics of multicarrier based multilevel PWM pulses for the inverters.Carrier-based PWM modulation for reduction of THD and losses in multilevel inverters was studied by Barreto et al [12]. Yousefpoor et al [13] have found an optimization algorithm to get a reduced THD. Batschauer et al [14] explored the hybrid multilevel inverter with half bridge circuit with unidirectional power flow. Cougo et al [15] have analysed and found that the Phase Disposition (PD) method is the best method to reduce the current imbalance in multilevel inverter. This paper investigates new hybrid carrier PWM stratergies using stepped reference for chosen three phase AMLI.

2. THREE PHASE ASYMMETRICAL MULTI LEVEL INVERTER (AMLI)

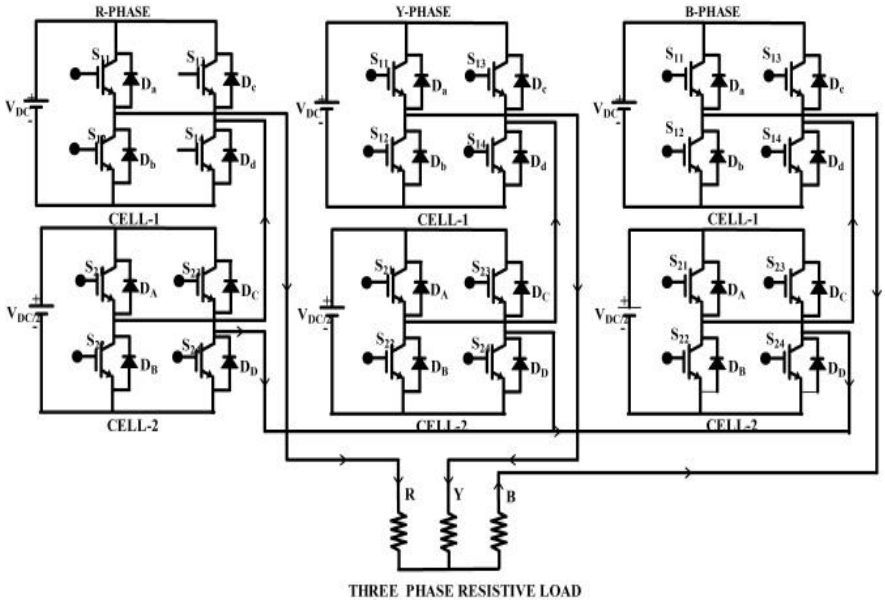

Figure 1 A three phase asymmetrical cascaded seven level inverter

Several inverters are series connected, with different topologies and different input voltages. Hence they are said to be AMLIs[10]. A seven level output voltage is achieved with two bridges in asymmetrical inverter whereas only five level output voltage will be achieved with two such bridges in case of conventional cascaded MLI[8]. In AMLI more voltage levels can be achieved with lesser number switches.Figure1 shows the chosen asymmetrical three phase inverter. Each cell has two pairs of complementary switches S_{11} and S_{22} and S_{12} and S_{21}. There are six cells used in the three phase inverter each leg containing two cells each[1].

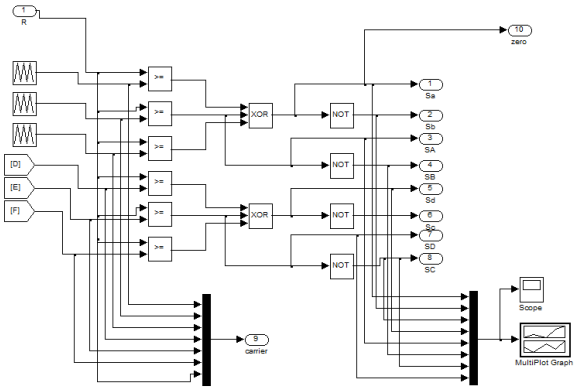

Figure 2 Sample PWM generation logic using SIMULINK model developed

3. MODULATION STRATEGIES

Several multilevel modulation strategies like PD, POD, APOD and VFPWM.are discussed in this section.The high number of switches composing a multilevel converter may lead to the conclusion that complex algorithms are necessary. The modulation algorithm used to drive the multilevel converter has to be aimed to give the output voltage level required for each leg through the translation in the proper switch configuration. The algorithms can be hardware or software implemented. The amplitude modulation index m_a and frequency modulation index m_f are shown below.

Amplitude modulation index $$m_a = \frac{2A_m}{(m-1)A_c}$$

$$m_f = \frac{f_c}{f_m}$$

The above equations are to find m_f and m_a forPD,POD,APOD and VF PWM strategies.

m=Number of levels

f_c= Frequency of carrier

f_m= Frequency of modulating wave

A_m=Amplitude of modulating wave

A_c=Amplitude of carrier

Stepped reference is used in this work along with hybrid carrier combination of triangular and inverted sine carrier

3.1 Phase Disposition (PD) Method

In this method[15] carriers are the same in frequency, amplitude and phases, but they are just

different in DCoffset to occupy contiguous bands as shown in Figure. 3. For this technique, significant harmonic energy is concentrated at the carrier frequency $f_c$but because it is a co-phase component, it does not appear in the line voltage. It should be noted that the other harmonic components are centeredon the carrier frequency as side bands[11]. An example of the carriers that is used in a two module seven level PWM inverter is shown in Figure.3.There are six distinct carriers, all in phase with one another and with the same magnitudes A_c.The difference between the carriers is that they are all displaced by DC offset. The reference waveform has peak to peak amplitude A_m, frequency f_m and its zero is centered in the middle of the carrier set. The reference (V_c) is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off . With reference to Figure 1 and the upper bridge , the modulation rules are:

If $V_{ref} > V_c$, then the switch S_{11} – on, S_{22}- off.

If $V_{ref} < V_c$, then the switchS_{11} –off,S_{22}- on.

where

V_{ref} = Reference voltage

V_c= Voltage of carrier

The resultant gate control is obtained by comparing each of the carriers to the related part of the reference which in turn controls a specific gate and the switching pattern for PDPWM[15]. The carrier on the positive side is triangular carrier and there is inverted sine carrierin the negative side.Hence the stratergy is named as hybrid carrier stratergy

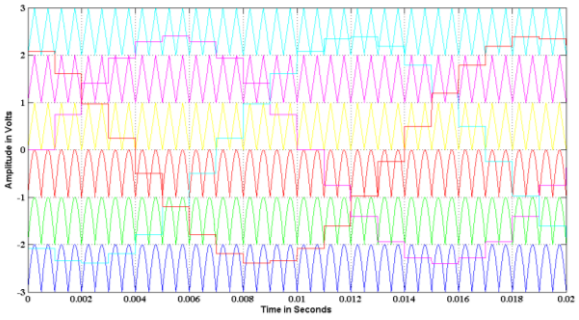

Figure 3 Carrier arrangements for hybrid carrier PDPWM strategy (m_a=0.8)

3.2 Phase Opposition Disposition (POD) strategy

With the POD method the carrier waveforms above the zero reference value are in phase. The carrier waveforms below are also in phase but are 180 degrees phase shifted from those above zero[2].The POD method yields quarter wave symmetry for even m_f and odd symmetry for oddm_f.Figure 4 shows the multicarrier arrangement for POD method for m_a=0.8and m_f =40.

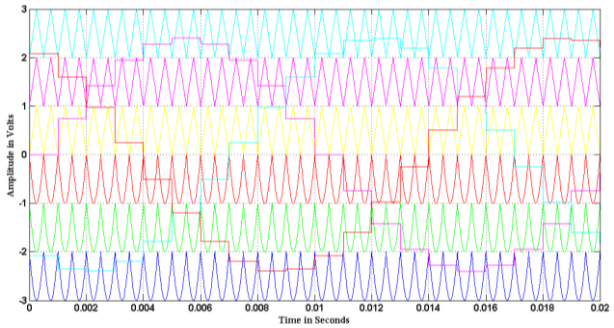

Figure 4 Carrier arrangements for hybrid carrier PODPWM strategy (m_a=0.8)

3.3 Alternate Phase Opposition Disposition (APOD) strategy

In case of Alternate Phase Disposition (APOD) modulation[5], every carrier waveform is in out of phase with its neighbor carrier by 180 degree. Since APOD and POD schemes in case of three level inverter are the same, a seven level inverter is considered to discuss about the APOD PWM scheme[8]. When the number of levelsn = 7, there are n – 1 = 6 carrier waveforms arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180.The converter switches to + V_{dc} when the reference is greater than all the carrier waveforms. The converter switches to +V_{dc} /2 when the reference is less than the uppermost carrier waveform and greater than all other carriers. The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lower most carriers.The converter switches to -V_{dc}/2 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers. This method requires each of the six carrier waves haveeven symmetry for even m_f and odd symmetry for oddm_f.Figure5 shows the carrier arrangements for APODPWM hybrid carrier strategy m_a=0.8 and m_f =40 fora seven level inverter to be phase displaced from each other by 180 degrees[10] alternately.

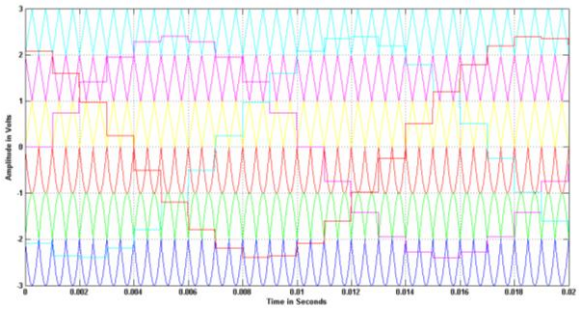

Figure 5 Carrier arrangements for hybrid carrier APODPWM strategy (m_a=0.8)

3.4 Variable Frequency (VF) PWM strategy

The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches in sub harmonic PWM using constant frequency carriers. In order to equalize the number of switches for all the switches, variable frequency PWM strategy is used as illustrated in Figure 6. The VFPWM scheme is more favorable than the conventional PWM technique for use in asymmetric

multilevel inverter. The carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches.Figure6 illustrates the carrier arrangements for VFPWM hybrid carrier strategy for m_a=0.8 and m_f =40.

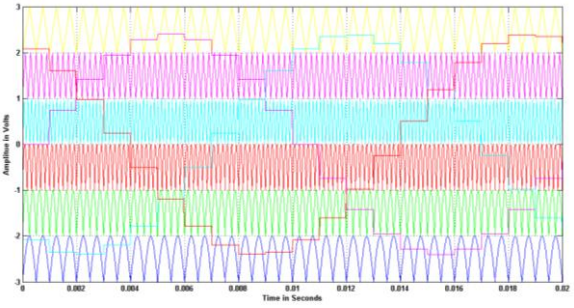

Figure 6 Carrier arrangements for hybrid carrier VFPWM strategy (m_a=0.8)

4. SIMULATION RESULTS

PWM circuit to generate the gating signals for the multilevel inverter switchesis shown Figure 2. To control a three phase multilevel inverter withseven output voltagelevels six carriers are generated and compared at each time to a set of three reference waveforms. One set of carrier wave is above the zero reference and another set below the reference. These carriers are same in frequency, amplitude and phases except in VFPWM but they are just different in DC offset to occupy contiguous bands.The frequency of reference signal determines the inverter output frequency and its peak amplitude controls the modulation index. The variation in modulation index changes the RMS output voltage of the multilevel inverter. By varying the reference signal frequency as well as modulation index, the output voltage is varied.Hence there can be voltage control.Figure 7-10 show the total harmonic distortion for m_a=0.8and for various modulation strategies. The output voltage for the simulated circuit for various modulation strategies are shown in Figure.11-14. The least %THD is achieved only in PDPWM modulation strategy as shown in Table 1. The maximum DC bus utilization is also achieved in the PDPWM modulation strategy which is dominant and is shown in the Table 2.Table 4 showsthat distortion factor is very relatively less in case of PODPWM strategy hence by using this technique we can achieve lesser switching losses and hence the life of the switch increases.Table 5 shows Form Factor (FF)The Crest Factor (CF) is a measure of peak current(I_s) as compared with its RMS value I_s. CF is often of interest to specify the peak current rating of the devices and components. The values for CF is shown in Table.3. The Distortion Factor (DF) for various m_a are shown in Table 4 and it shows the amount of harmonics that remains in the output voltage after the second order attenuation. Table 5 shows FF.The following parameter values are used for simulation: V_{dc1} =100V V_{dc2} =50V and R(load) = 100 ohms for each phase.Figure 15 illustrates the sample pulse generated for the three phase AMLI with hybrid carrier PDPWM strategy with stepped reference.Figure 16 shows the pictorial representation for %THD vs m_a for various PWM strategies. A bar chart for RMS voltage (fundamental) vs m_a is plotted and shown in Figure 7.

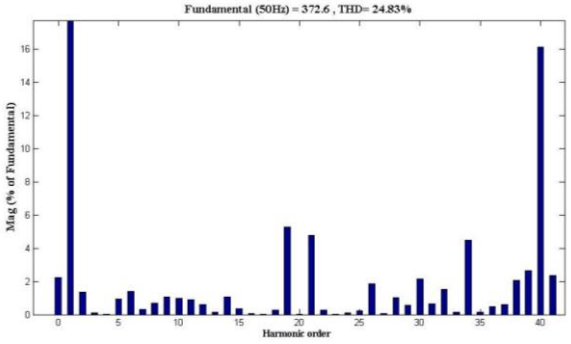

Figure 7 Harmonics for the hybridcarrier PDPWM for m_a=0.8 with stepped reference

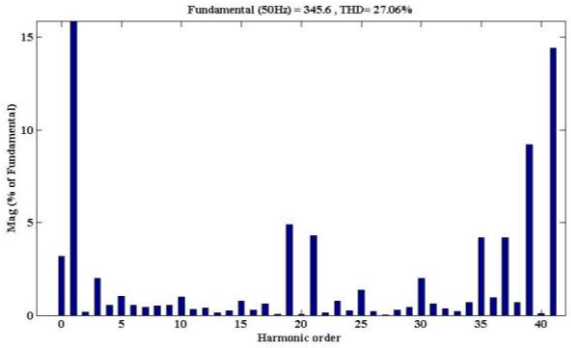

Figure 8 Harmonics for the hybrid carrier PODPWM for m_a=0.8 with stepped reference

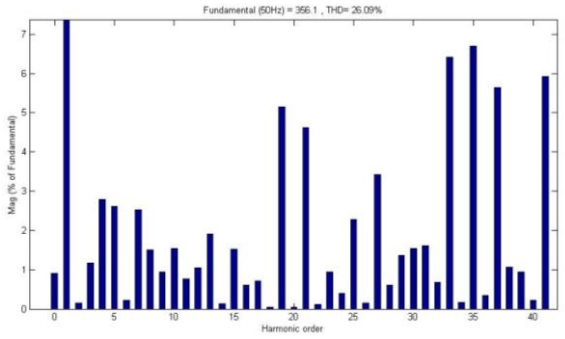

Figure 9 Harmonics for the hybrid carrier APODPWM for m_a=0.8 with stepped reference

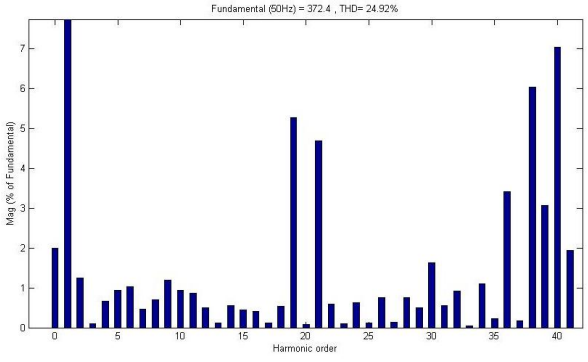

Figure10 Harmonics for the hybrid carrier VFPWM for m_a=0.8 with stepped reference

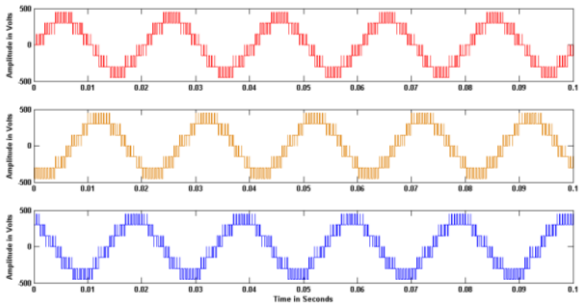

Figure 11Output voltage generated by hybrid carrier stepped referencePDPWM strategy

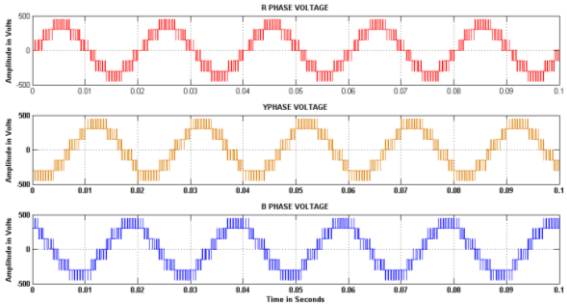

Figure 12 Output voltage generated by hybrid carrier stepped referencePODPWM strategy

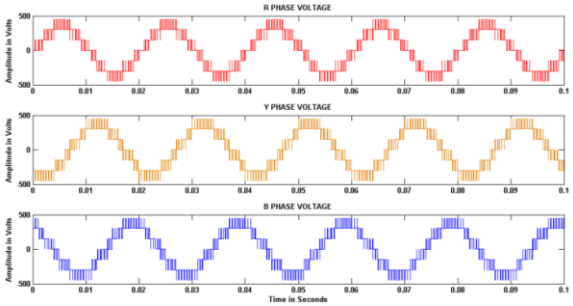

Figure 13 Output voltage generated by hybrid carrier stepped referenceAPODPWM strategy

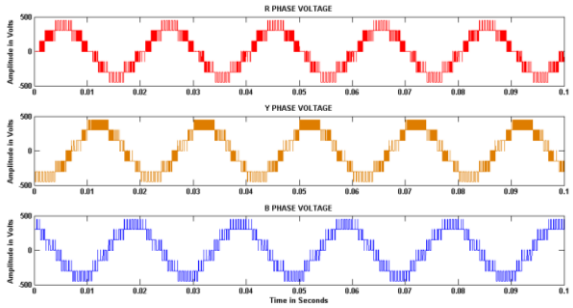

Figure 14 Output voltage generated by hybrid carrier stepped referenceVFPWM strategy

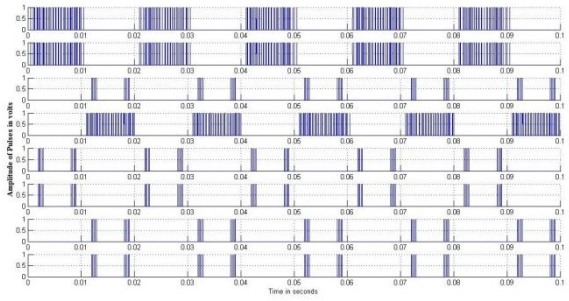

Figure 15 Sample pulse pattern for three phase AMLI with hybrid carrier PDPWM strategyusing stepped reference

Table 1

%THD (fundamental) of output voltageof AMLI for various values of m_a

m_a	PD	POD	APOD	VF
1	18.17	21.24	20.44	18.21
0.95	20.92	23.91	23.43	20.98
0.9	22.99	25.35	25.09	22.96
0.85	24.12	25.71	25.69	24.08
0.8	24.83	27.06	26.09	24.92
0.75	26.2	28.16	27.14	26.21
0.7	26.42	27.99	27.26	27.4

Table 2

RMS (fundamental) values of output voltageof AMLI for different PWM stategies and various values of m_a

m_a	PD	POD	APOD	VF
1	322.6	303.8	310.8	322.3
0.95	308.5	298.5	292.5	308.5
0.9	254.8	273.8	278.3	294.2
0.85	279.7	260.5	264.5	278.8
0.8	263.5	244.4	251.8	263.3
0.75	249.1	230.4	239.2	249.3
0.7	228.9	214	224.2	222.1

Table 3

Crest Factor (CF) values of output voltageof AMLI for different PWM stategies and various values of m_a

M_a	PD	POD	APOD	VF
1	1.414	1.427	1.414	1.414
0.95	1.414	1.416	1.414	1.414
0.9	1.636	1.416	1.414	1.414
0.85	1.414	1.414	1.414	1.414
0.8	1.414	1.414	1.414	1.414
0.75	1.414	1.414	1.414	1.416
0.7	1.414	1.414	1.414	1.446

Table 4

Distortion Factor (DF) values of output voltageof AMLI for different PWM stategies and various values of m_a

m_a	PD	POD	APOD	VF
1	3.03E-03	3.70E-03	4.23E-03	3.41E-03
0.95	3.39E-03	3.31E-03	3.21E-03	2.56E-03
0.9	3.46E-03	2.33E-03	2.53E-03	3.18E-03
0.85	3.79E-03	3.31E-03	2.87E-03	3.32E-03
0.8	2.53E-03	2.13E-03	3.47E-03	2.27E-03
0.75	2.57E-03	1.75E-03	3.15E-03	1.97E-03
0.7	2.57E-03	2.28E-03	1.16E-03	1.70E-03

Table 5

Form Factor (FF) values of output voltageof AMLI for different PWM stategies and various values of m_a

m_a	PD	POD	APOD	VF
1	7.05E+01	2.56E+01	4.41E+01	5.58E+01
0.95	4.28E+01	2.36E+01	3.71E+01	3.77E+01
0.9	2.83E+01	2.27E+01	4.17E+01	3.19E+01
0.85	2.83E+01	2.78E+01	5.78E+01	2.64E+01
0.8	3.19E+01	2.22E+01	7.81E+01	3.55E+01
0.75	2.44E+01	2.46E+01	6.38E+02	2.46E+01
0.7	2.73E+01	2.53E+01	1.30E+02	2.37E+01

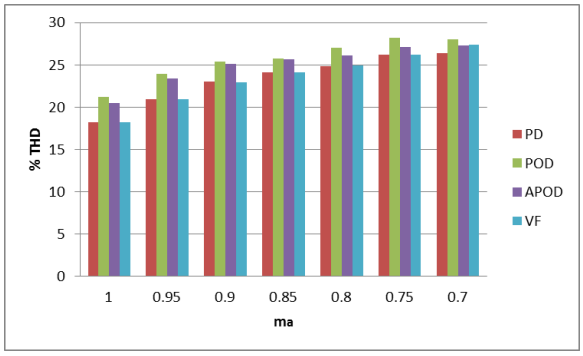

Figure.19 % THD Vs m_a

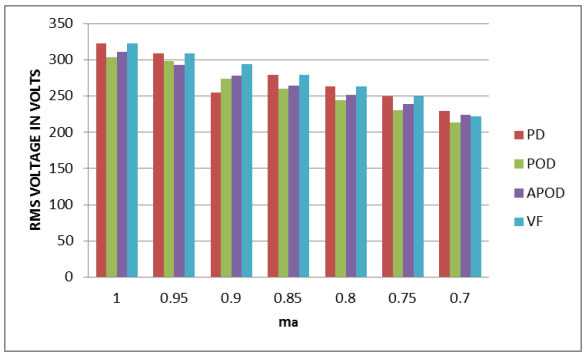

Figure.20 RMS voltage Vs m_a

5. CONCLUSION

The three phase seven level AMLI uses reduced number of switches with unequal DC sources as input to the inverters. Strategiessuch as PDPWM, PODPWM, APODPWM and VFPWM strategies where used with the proposed hybrid carrier and stepped reference modulation strategy and it is found that the %THD is relatively less in the hybrid PDPWM and the COPWM strategies. It is also observed that hybrid PDPWM provides relatively better DC bus utilizationfor m_a=0.7-1

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