

Conditional Precharge Dynamic Buffer Circuit

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ABSTRACT

In this paper, footless domino logic buffer circuit is proposed. It minimizes redundant switching at the dynamic and the output nodes. This circuit passes propagation of precharge pulse to the dynamic node and avoids precharge pulse to the output node which saves power consumption. Simulation is done using 0.18μm CMOS technology. We have calculated the power consumption, delay and power delay product of proposed circuit and compared the results with existing circuits for different logic function, loading condition, clock frequency, temperature and power supply. For capacitance 500fF, our proposed circuit reduces power consumption by 72.69%, 26.35% and 24.03% as compared to standard footless domino, SP-Domino and SSPD techniques.

Keywords

Buffer, Domino circuit, Power consumption, Delay, Precharge pulse.

1. INTRODUCTION

Domino logic circuits are used in wide applications such as memory [1], microprocessor [2], adder [3] etc. It has superior advantage over static logic circuit, it require less area and reduces output load capacitance hence enhance the speed. Realization of wide fan-in gates using static logic circuit requires long stack of pMOS and nMOS which is not practical, it increase the delay and area. But domino logic use dual phase namely precharge and evaluation to implement complex circuit with single evaluation network [4]. Domino circuit has drawback of high power consumption due to clock loading and reduce noise margin due to charge sharing and charge leakage. Charge sharing and charge leakage is compensated by adding keeper transistor.

Buffer is essential to drive the output of domino circuit into the next stage [5]. Static CMOS logic circuit consumes power during the toggling of the output state. Domino logic circuit consumes power due to the unwanted redundant switching at dynamic and output nodes. This redundant switching of domino logic circuit consumes more power as compared to static CMOS circuit. Different circuits are proposed in the literature to deal this issue. Single phase domino logic [6] and static switching pulse domino [7] logic reduces the redundant switching at both dynamic and output node. True single phase clock domino logic (TSPC) [8], [9], limited switch dynamic logic (LSDL) [10] and pseudo dynamic buffer (PDB) [11] reduces the redundant switching only at output node.

Power dissipation of the domino circuit is divided into three components [5]:

$$P_{Total} = P_{Dynamic} + P_{Leakage} + P_{Short\ Circuit} \quad (1)$$

$P_{Dynamic}$ is the power consumed during capacitance charging and discharging, $P_{Leakage}$ is the total leakage power of the circuit and this power increases as the technology is scaled down, and $P_{Short\ Circuit}$ is the power dissipated when direct current flows from power supply to ground.

$$P_{Dynamic} = \alpha \times C \times VDD^2 \times F_{CLK} \quad (2)$$

Where α is the redundant switching at the output and dynamic node, it depends on the gate topology and inputs, C is the capacitive load at the evaluation node, F_{clk} is the clock frequency.

$$P_{Leakage} = I_{Leakage} \times VDD \quad (3)$$

Where $I_{Leakage}$ is the combination of subthreshold and gate oxide leakage current.

$$P_{Short\ Circuit} = \alpha \times I_{SC} \times VDD \quad (4)$$

I_{SC} for domino logic gate is the contention current that flows between the evaluation network and pMOS keeper during evaluation mode. This power dissipation must be kept low for better operation of the domino circuit.

In this paper, we propose switching-aware technique which minimizes redundant switching at the dynamic and output nodes, and the circuit behaves like static CMOS circuits. Pull up network consist of combination of a PMOS and NMOS transistor. Dynamic node is conditional precharge to high voltage only when both the transistors of pull up network turns ON and the pull down network turns OFF simultaneously at the start of each clock high for short duration of time. Using this technique, it allows the propagation of precharge pulse to the dynamic node and avoids the precharge pulse to the output node. The remainder of the paper is organized as follows. Previous proposed techniques are described in section 2. Proposed circuit is described in section 3. Simulation results are presented in section 4, and conclusion is presented in section 5.

2. PREVIOUS WORK

Standard footless domino logic circuit is shown in Fig.1. When input is kept high, the operation of the circuit is characterized in two operating phase is shown in Fig.2.

During precharge phase, M1 turns ON, dynamic node is charged to high voltage and output is discharged to low voltage. During evaluation phase dynamic node is discharged to low voltage and output is charges to high voltage. When input is kept low, dynamic node maintain high in both operating phase. Here propagation of precharge pulse is needed at the dynamic node and prevented at the output node to make the circuit stable. This redundant switching increase the power consumption.

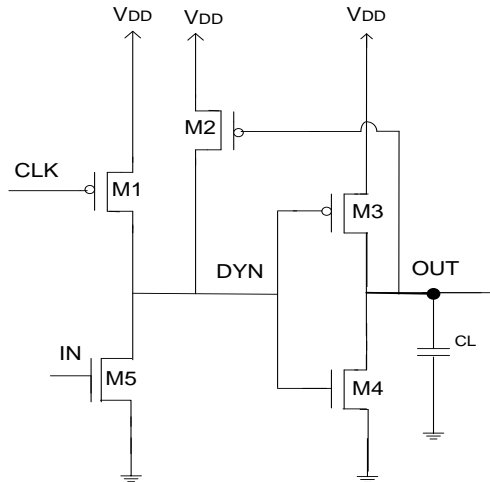


Figure 1. Standard footless domino circuit.

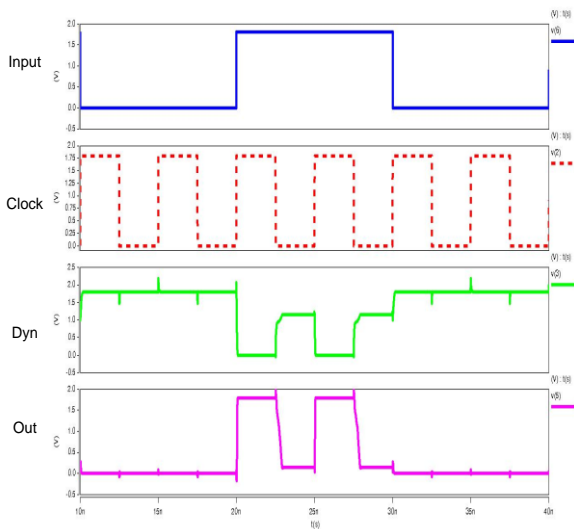


Figure 2. Voltage characteristics at various node of standard footless circuit.

Circuit techniques have been proposed in the literature such as single phase SP-Domino logic, static switching domino logic. Main idea regarding these circuit designs is to reduce redundant switching at both dynamic and output nodes.

2.1 Single-Phase SP-Domino Logic

Single phase domino logic is similar to the clock delayed domino logic [13] is shown in Fig.3 and its voltage

characteristics is shown in Fig.4. The latest arriving of input does not arrive before the rising edge of the delayed clock [6]. The gate has single phase as both pull up and pull down network of the dynamic node occurs during the evaluation phase. Transistor M1 works as pull up and keeper. Pulse generator produce signal P which turns ON M1 unconditionally at the start of evaluation cycle. If both transistor M1 and M10 turns on simultaneously, small contention current flows between them for short duration of pulse P at the gate of M1. If the transistor M10 turns OFF at the start of evaluation phase, M1 charged the dynamic node to high voltage. If the value of dynamic node is low at the end of pulse signal P, M7 remains OFF and P is pulled up high by transistor M4. Charging operation of the dynamic node starts after the pulse signal returns to low voltage. The logical expression for pulse P is

$$P = \overline{CLK_i \cdot CLK_j + DYN} \quad (5)$$

Where CLK_i and CLK_j are clock delayed signal and its delayed inverse.

Design of SP-Domino has several flaws. Size of M1 has lack of flexibility. If the size of M1 increases, keeper ratio increases. Keeper ratio is defined as the ratio of current driving capability of transistor M1 to the transistor M10. High keeper ratio increases the contention current and the delay. High keeper ratio has unsymmetrical rise and fall time of the output signal. To have symmetric rise and fall time, K must be a fixed value.

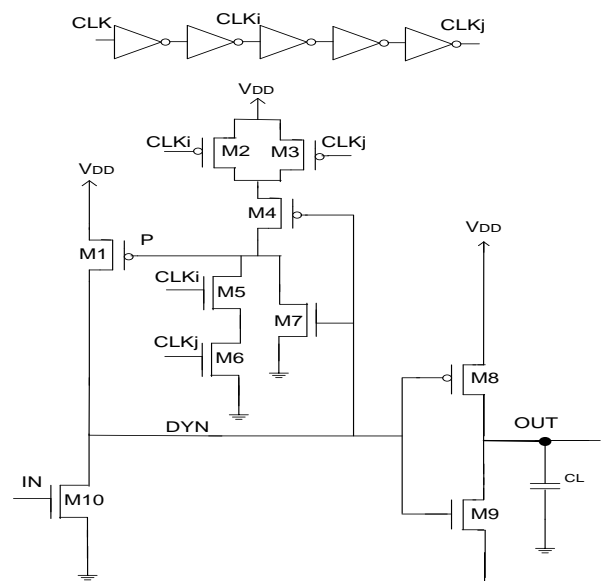


Figure 3. Single phase SP-Domino circuit.

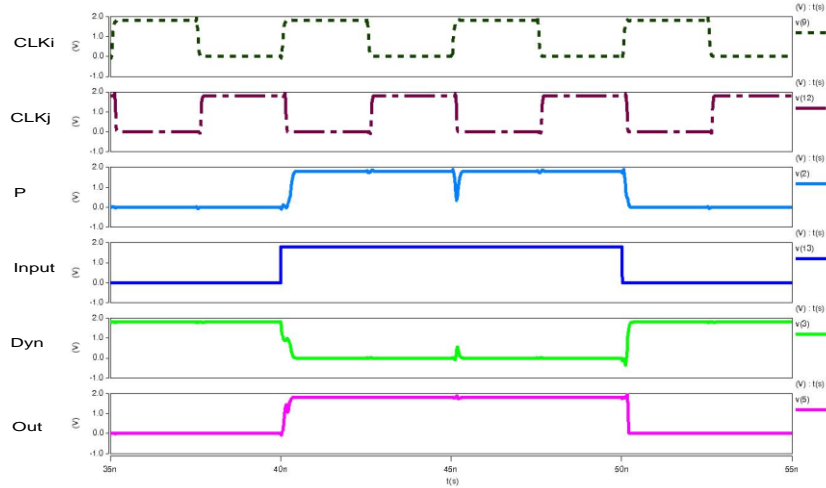


Figure 4. Voltage characteristics at various node of single phase domino logic.

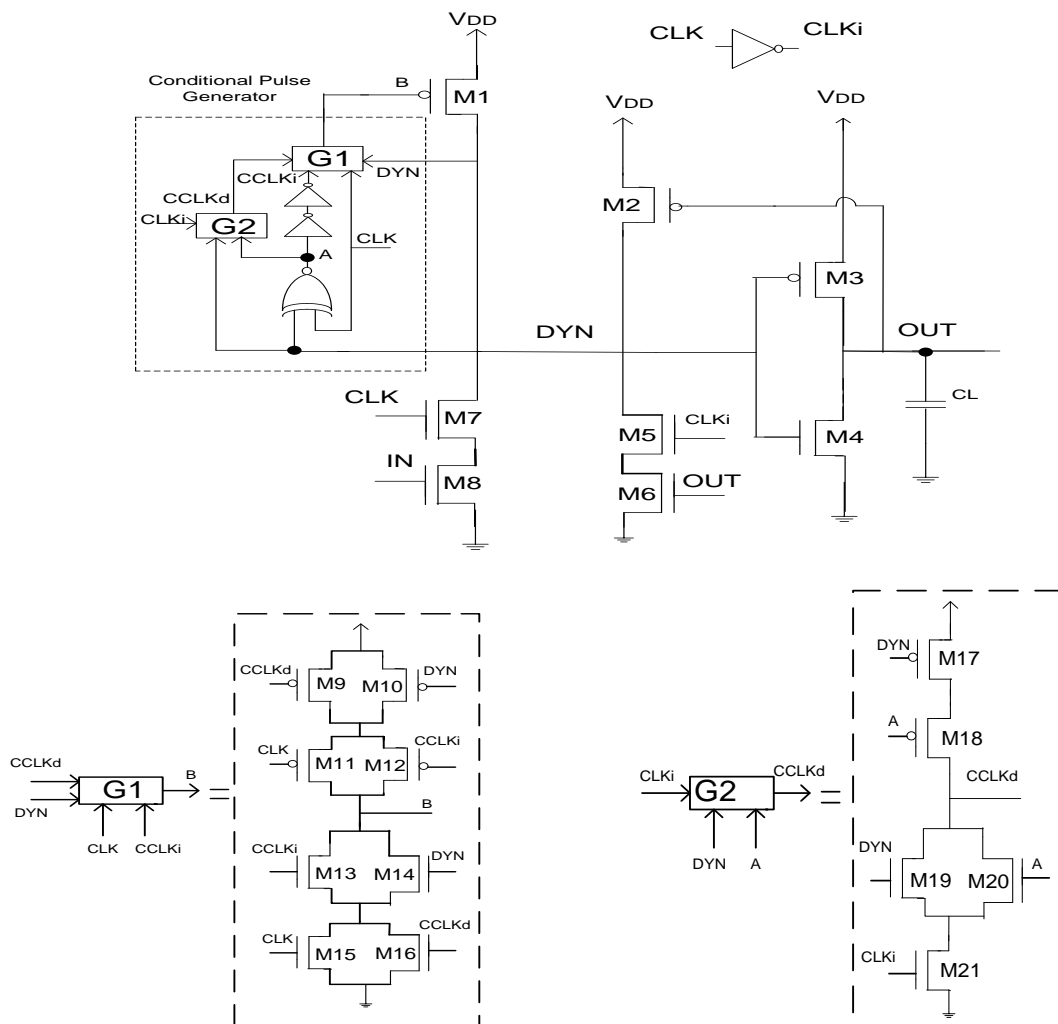


Figure 5. Dynamic buffer implemented with the SSPD technique. G1 and G2 are the two gates of the pulse generator.

2.2 Static switching pulse domino (SSPD)

SSPD is similar to SP-Domino with static input and output characteristics [7]. SP-Domino uses single transistor as pull up and keeper but in case of SSPD employs separate transistors M1 and M2. Both transistors M1 and M2 never ON simultaneously. SP-Domino has lack of flexibility in designing the size of transistor M1 to get symmetrical rise and fall delay of the output. SSPD allows independent tuning of rise and fall delays.

SSPD technique employs a conditional pulse generator (CPG) is shown in Fig.5 and its voltage characteristics is shown in Fig. 6. The CPG generate pulse, M1 turns OFF only when the dynamic node has been discharged or held low in last evaluation cycle and Keeper M2 turns OFF. If the dynamic node is not discharged, M1 is OFF by CPG. M8 is ON providing contention current by the keeper. CPG internally generate two additional clock phases $CCLK_d$ and $CCLK_i$. Their behavior is related to the clock signal (CLK) and dynamic node. The two clock phases utilized by the block G1 in CPG to produce pulse B. Drawback of this technique is that it require complex conditional pulse generator. The logical expression for pulse B is

$$B = \overline{CLK \cdot CCLK_i + DYN \cdot CCLK_d} \quad (6)$$

Where $CCLK_d$ and $CCLK_i$ are the conditionally generated delayed and inverse phases of the original clock CLK.

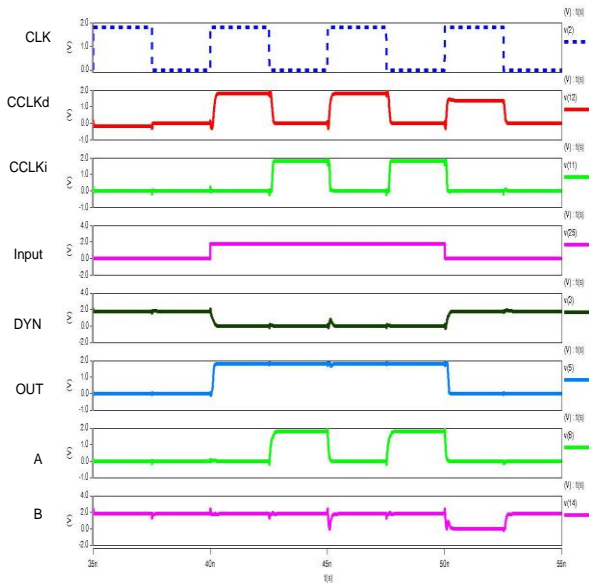


Figure 6. Voltage characteristics at various node of static switching pulse domino.

3. PROPOSED WORK

The proposed buffer circuit has static input and output characteristics, its circuit diagram as shown in Fig. 7. Voltage characteristics at different node as shown in Fig.8. Combination of PMOS M1 and NMOS M2 works as function of pull up network and M3 as keeper-transistor. Input of M2 is clock (CLK) and M1 is non-inverting delayed clock (CLKd). Timing diagram of clocks is shown in Fig.9. Dynamic node is conditional precharge to high voltage only when both the transistors of pull up network turns ON and the M6 turns OFF simultaneously at the start of each clock high for short duration of time T_d . Using this technique, it allows

the propagation of precharge pulse to the dynamic node and avoids the precharge pulse to the output node.

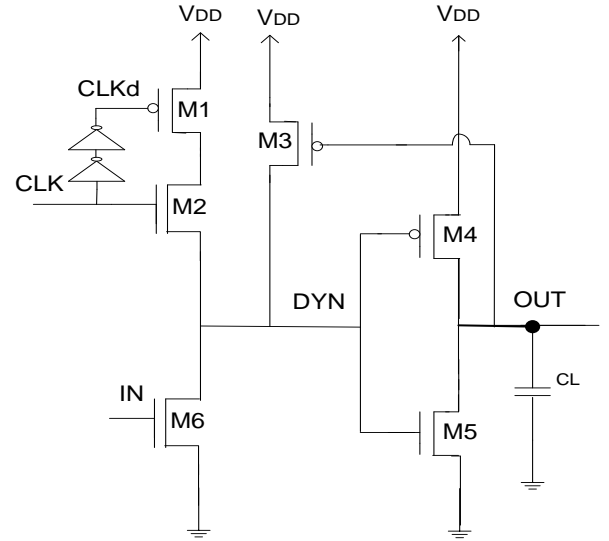


Figure 7. Circuit diagram of proposed circuit.

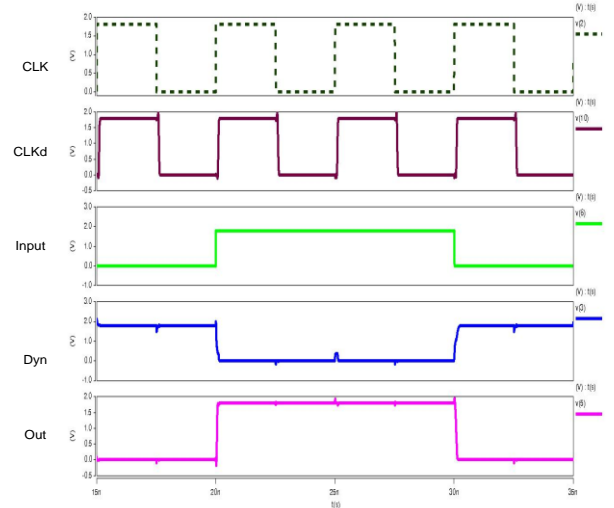


Figure 8. Voltage characteristics at various node of proposed circuit.

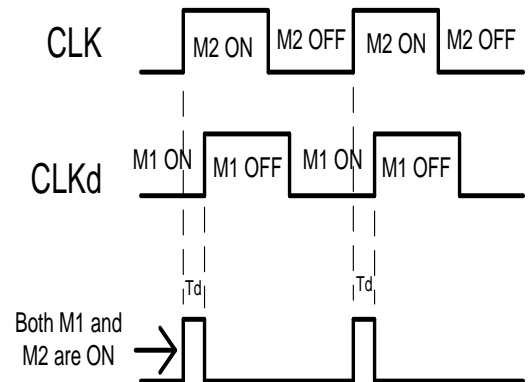


Figure 9. Timing diagram of clocks.

Operation of the circuit is explained by considering the input logic. During clock is low, dynamic node holds the previous value regardless of the input of the circuit.

Case 1: When input is high, at the start of clock high, for a short period of time T_d , CLK is high and delayed clock CLKd is low. M1, M2 and M6 are turned ON provides contention current to the pull down network as shown in Fig.10. Size of M6 is large enough to discharge the dynamic node to low voltage. After the delay of time T_d , both CLK and CLKd is high and M1 turns OFF as shown in Fig.11. Thus no further contention current flows to the pull down network and dynamic node remains at logic low.

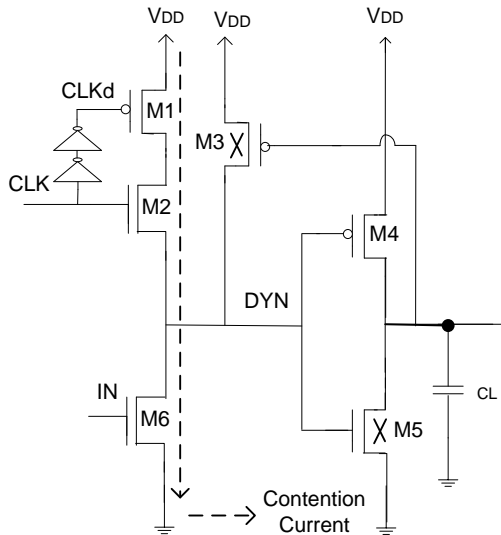


Figure 10. Operation of the proposed circuit when the input is high for short period of time delay T_d .

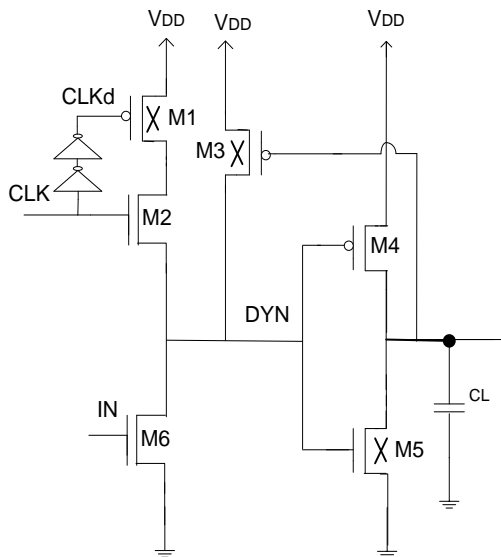


Figure 11. Operation of the proposed circuit when the input is high after the time delay T_d .

Case 2: When input is low, at the start of clock high, CLK is high and delayed clock CLKd is low. M1 and M2 turned ON simultaneously charged the dynamic node to logic high as shown in Fig.12. For the rest of the clock high, both CLK and CLKd are high, M1 turns OFF as shown in Fig.13. Dynamic node remains at logic high.

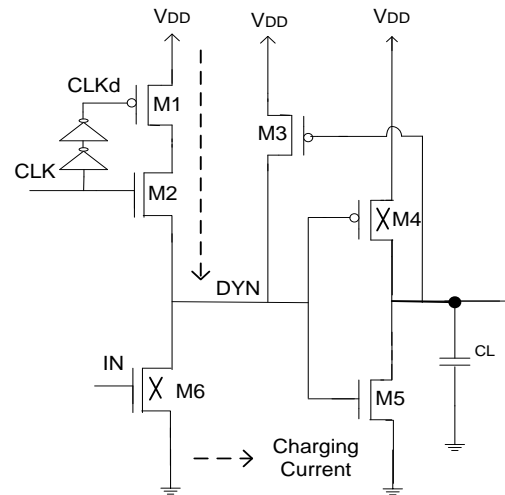


Figure 12. Operation of the proposed circuit when the input is low for short period of time delay T_d .

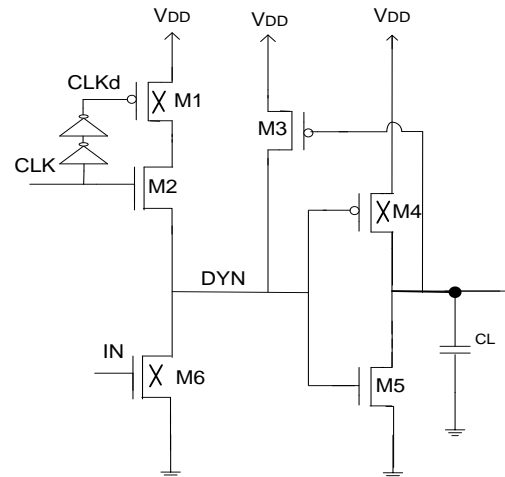


Figure 13. Operation of the proposed circuit when the input is low after the time delay T_d .

4. SIMULATION RESULTS

The proposed circuit and the existing circuit such as standard footless domino, single phase SP-Domino and static switching pulse domino are simulated using HSPICE in the high performance 180nm predictive technology [11]. The supply voltage in the simulations is 1.8V and clock rate is 200MHz and with 50% duty cycle (clock period is 5ns). Rise and fall time of the clock rate is set equal to 10ps. Transistor size is set by $W_{PMOS} = 27L_{min}$, $W_p/W_n = 2$ for whole circuit. Worst case delay is determined from input to the output node V_{out} . Power consumption is determined when input is high voltage. Standby power is measured when input of the circuit is low.

Comparison of power saving for various logic functions of proposed domino circuit with standard footless domino circuit is tabulated in Table 1. In this comparison, clock frequency, input frequency and load capacitance were set to 200MHz, 50MHz and 100fF. From the table, OR gates logic functions save more power as compared to AND gates logic functions.

Table 1. Comparison of Power Saving with Different Logic Function in 0.18 μ m (VDD=1.8V, Clock Frequency=200MHz, Input Frequency=50MHz and load capacitance=100fF).

Logic Function	Standard footless Circuit (μ W)	Proposed Circuit (μ W)	Power saving by proposed circuit (%)
A	394.95	51.10	87.05
A.B	263.86	51.72	80.39
A+B	391.33	52.59	86.55
A.B.C	200.82	53.02	73.59
A+B+C	400.14	54.07	86.48
A.B.C.D	177.74	56.20	68.38
A+B+C+D	403.58	56.04	86.11

Comparison of power consumption of proposed circuit and existing circuits with clock frequency 200MHz where load capacitance is varied as shown in Fig.14. As a result, at higher load capacitance, our proposed circuit saves higher power consumption as compared to existing circuits. For capacitance 500fF, our proposed circuit reduces power consumption by 72.69%, 26.35% and 24.03% as compared to standard footless domino, SP-Domino and SSPD techniques. Our proposed circuit has better delay as compared to SP-Domino and SSPD techniques except standard footless domino circuit as shown in Fig.15. Our proposed circuit has better power delay product and at higher load capacitance its saving is large as compared to existing circuits as shown in Fig.16. Proposed circuit has better standby product as compared to SP-Domino technique and have higher value as compared to other exiting techniques as shown in Fig.17.

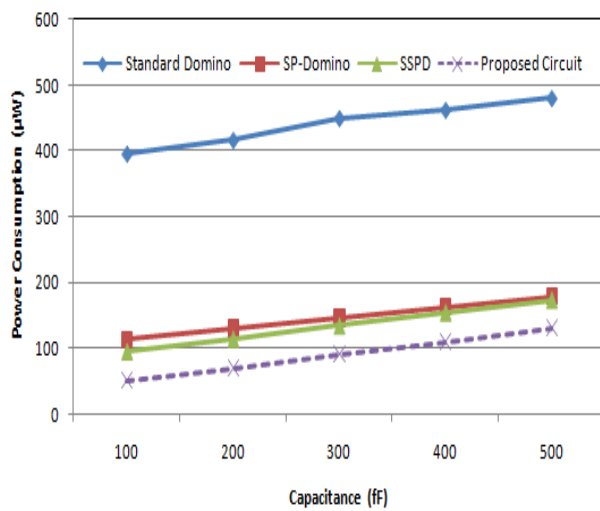


Figure 14. Power consumption versus capacitance.

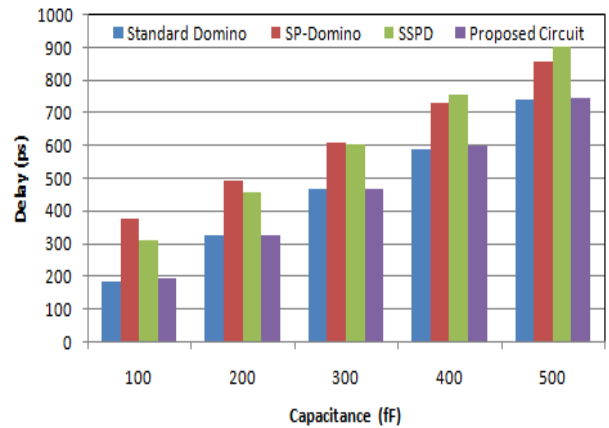


Figure 15. Delay versus capacitance.

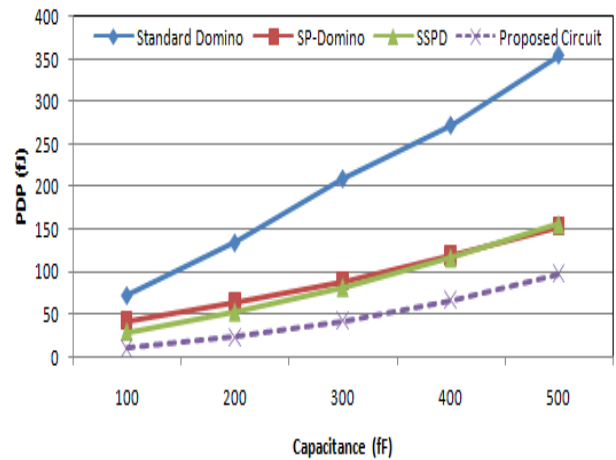


Figure 16. PDP versus capacitance.

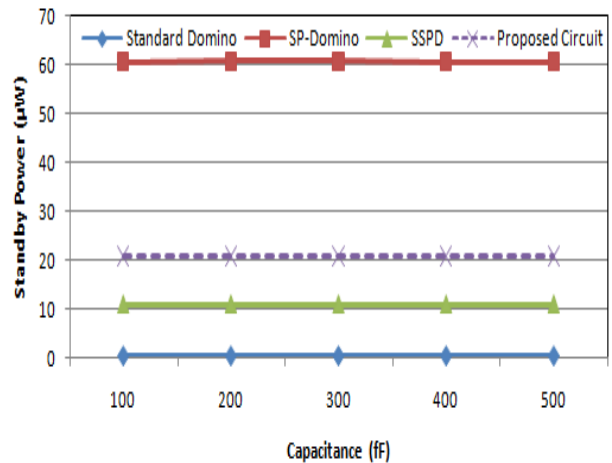


Figure 17. Standby power versus capacitance.

Fig.18 shows the comparison of power consumption of proposed circuit and existing circuits, load capacitance is set 100fF for different clock frequency. It shows power consumption increase as clock frequency increases, maximum power saving is achieved at higher operating frequency. For operating frequency 500MHz, our proposed circuit reduces power consumption by 78.45%, 59.86% and 50.26% as compared to standard footless circuit, SP-Domino SSPD circuit.

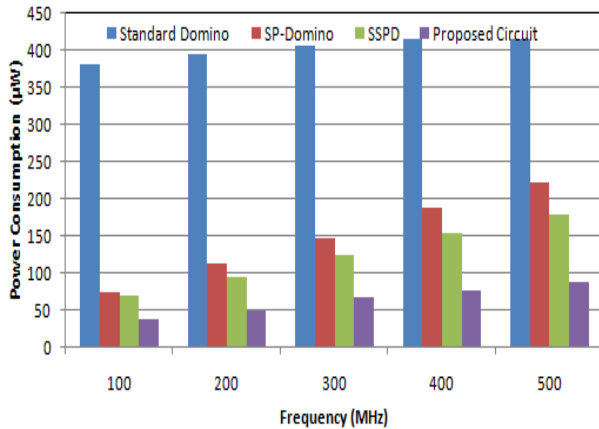


Figure 18. Power consumption versus frequency.

Table 2. Comparison of power consumption (µW) of proposed circuit with the existing circuits.

Temperature (°C)	Standard Domino	SP-Domino	SSPD	Proposed Circuit
30	389.56	112.95	95.19	51.09
50	382.81	112.75	93.89	51.31
70	359.59	112.84	93.33	51.58
90	339.88	112.75	94.04	51.54
110	322.35	112.76	93.88	51.81

Table 3. Comparison of delay (ps) of proposed circuit with the existing circuits.

Temperature (°C)	Standard Domino	SP-Domino	SSPD	Proposed Circuit
30	185.11	376.58	312.52	197.39
50	196.42	385.81	331.49	208.26
70	208.13	398.51	352.47	219.80
90	220.35	415.11	374.42	232.19
110	233.77	432.91	398.93	245.37

Table 4. Comparison of delay (ps) of proposed circuit with the existing circuits.

Temperature (°C)	Standard Domino	SP-Domino	SSPD	Proposed Circuit
30	72.11	42.53	29.74	10.08
50	75.19	43.50	31.12	10.68
70	74.84	44.96	32.89	11.33
90	74.99	46.80	35.21	11.96
110	75.35	48.81	37.45	12.71

Table 2 illustrates the relationship between the power consumption and temperature for proposed circuit and existing circuits, clock frequency and load capacitance were set 200MHz and 100fF. It shows proposed circuit has independent on temperature variation. At 110°C, proposed circuit reduces power consumption by 83.92%, 54.05% and 44.81% as compared to standard footless circuit, SP-Domino

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circuit and SSPD circuit. Similarly, in Table 3 delay versus temperature is illustrated. Our proposed circuit suffer little delay penalty as compared to standard footless circuit and improves as compared to the other existing techniques. Table 4 shows PDP versus temperature, our proposed circuit has minimum PDP as compared to existing techniques.

Fig.19 illustrated the power consumption for proposed circuit and existing circuits for different power supply voltages. The clock frequency is set 200MHz and load capacitance is set 100fF. Our proposed circuit shows better power saving at higher power supply.

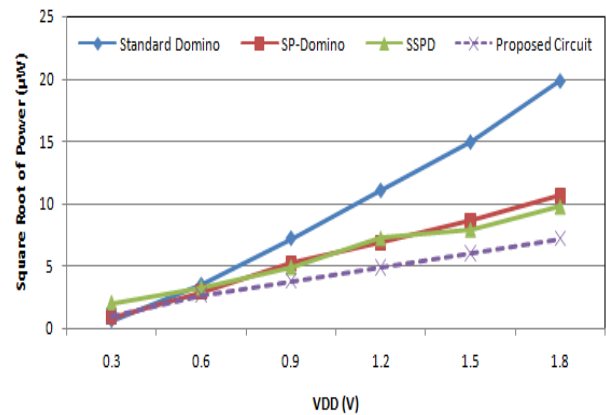


Figure 19. Power consumption versus power supply.

5. CONCLUSION

Buffer circuit is essential to drive the output of the present stage into the next stage. Standard domino has redundant switching at dynamic and output node, this increases the dynamic power consumption of the circuit. In this paper a new circuit is proposed to work the domino as buffer. Pull up network of proposed circuit has combination of PMOS and NMOS transistor, and utilizes delayed clock. Dynamic node is conditional charged to high voltage only when both the transistors of pull up network turns ON and the pull down network turns OFF simultaneously at the start of each clock high for short duration of time. This technique passes the propagation of precharge pulse to the dynamic node and avoids to the output node, reduces the dynamic power consumption.

Proposed circuit and the existing circuits are simulated are simulated in 0.18µm using HSPICE. Performance of the proposed structure is compared with existing circuits for different clock frequency, loading condition and temperature. Our proposed circuit saves higher power consumption as compared to existing circuits. For capacitance 500fF, our proposed circuit reduces power consumption by 72.69%, 26.35% and 24.03% as compared to standard footless domino, SP-Domino and SSPD techniques. For operating frequency 500MHz, our proposed circuit reduces power consumption by 78.45%, 59.86% and 50.26% as compared to standard footless circuit, SP-Domino circuit and SSPD circuit.

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