Optimization of Pie-gate Bulk FinFET Structure

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ABSTRACT

In this paper we propose a novel Pie gate bulk FinFET structure for logic applications suitable for system-on-chip (SOC) requirements. The influence of gate at bottom to junction depth, misalignment was examined for deeper junctions and shallower junctions. It has shown that bulk FinFET with source/drain to body (S/D) junctions shallower than gate at bottom has equal or better subthreshold performance than SOI FinFET. Further, we extend the concept of heavy body doping in bulk FinFETs of Pie-gate structure. The characteristics of such bulk FinFET structure is analyzed by 3D device simulation and compared with SOI FinFET.

General terms

Bulk Fin-shaped field-effect transistor (FinFET), short-channel performance, SS, DIBL, sentaurus TCAD device simulator**.**

Keywords

Shallower junction, Punchthrough stopper, pie gate structure

1. INTRODUCTION

Double- gate SOI MOSFETs[1] have shown excellent down-scaling characteristics and high-performance when compared to the conventional single-gate device structures, due to better gate controllability of the channel. FinFET is a self-aligned double-gate transistor [2]. It is the most viable implementation of double-gate MOSFET structure because of its simplicity and compatibility with conventional planar CMOS technology [3]. FinFET is available in two forms one of them is Bulk or body-tied FinFET and other is SOI FinFET. The bulk FinFET has gained attention mainly due to its ability to be integrated with standard bulk CMOS technology [4, 5]. Also, the bulk FinFET shows better immunity to negative bias- temperature (NBT) stress [6].

Although, SOI wafer [7, 8] has shown excellent short channel characteristics, it has some disadvantages over bulk FinFETs such as high wafer cost, high defect density, heat transfer problems and may suffer from floating body problem[9]. The Bulk FinFET shows excellent promise but they do not have performance as good as SOI FinFET [10]. So, it is important to optimize bulk FinFET performance as in SOI FinFET. The earlier bulk FinFET structures[11,12,13] use a heavily doped upper Fin/channel doping and a heavier lower fin doping to control the short-channel effects (SCEs) but this results in a channel mobility degradation causing a lower I_{ON}/I_{OFF} ratio. Therefore different Bulk structures are studied can compared for non uniform doping profiles. Further, Bulk FinFET of heavy body doping i.e. Punchthrough stopper [14] and Pie-gate bulk FinFET i.e. isolation oxide with source/drain-to-body (S/D) junctions shallower than gate at bottom [15] is reported as Fig 1. Here, Pie-gate structure (Fig 2) is basically represented by misalignment (ΔX_j=negative) between the S/D junctions and the bottom of the gate electrode. Deeper gate electrode (shallower junctions) has an enhanced control over the bottom of the Fin and its electrostatic control also serves as a punch-thorough stopper which enhances the device subthreshold performance [15].

2. DEVICE STRUCTURE

The device structure has been made with 3-D TCAD structure editor [16]. The double-gate FinFET designed is of 32nm channel length, oxide thickness 1.1nm, 11nm Fin width, 60nm Fin height and SiO2 as gate oxide material with 1.0V supply. Device is also simulated and optimized for different bulk doping profile. Calibration of TCAD tool is done properly before simulations

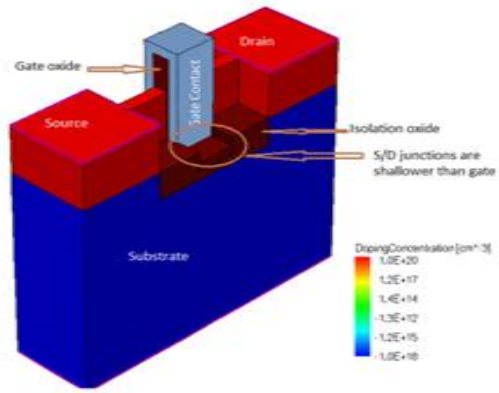


Fig 1: 3-D structure of TG FinFET

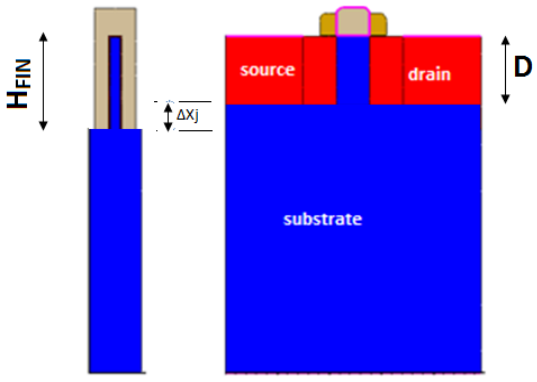


Fig 2: Cross-sectional view of pie gate FinFET structure

3. RESULT AND DISCUSSION

Conventional Bulk FinFET with low channel doping (1E16) has DIBL of 371 mV/V and Subthreshold slope of 328 mV/Decade. High channel doping is used to reduce off state current to improve performance of Bulk FinFET. The Bulk FinFET with high channel doping (1E18) shows significant improvement having DIBL of 42.69 mV/V and subthreshold slope of 74.24 mV/decade as Table 1. But this will results in significant mobility degradation and high parasitic capacitances. Therefore non uniform doping is better solution for this problem.

Table 1. Subthreshold performance with different channel doping

Channel doping(cm^{-3})	DIBL(mV/V)	SS(mV/decade)
1.00E+16	371.63	328.39
1.00E+17	58.62	78.02
1.00E+18	42.69	74.24
1.00E+19	34.83	68.23

3.1 Non uniform channel doping of Bulk FinFET

To control short channel effects (SCEs) following doping profiles are studied in our work:

Profile (I)- In this profile heavy channel doping is used in upper Fin region and relatively heavier channel doping in lower Fin region as in Fig 3(a)

Profile (II) – It has undoped/moderately doped channel with a heavier doping in the lower Fin region as in Fig 3(b).

Profile (III) – It has undoped/moderately doped channel with the heavier doping in the lower Fin region that is extended deeper into the bulk as in Fig 3(c).

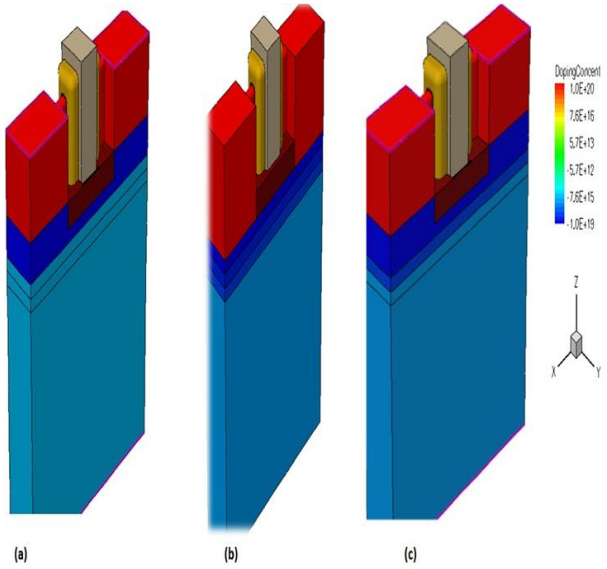


Fig 3: 3-D view of (a) Doping profile (I) (b) Doping profile (II) (c) Doping profile (III)

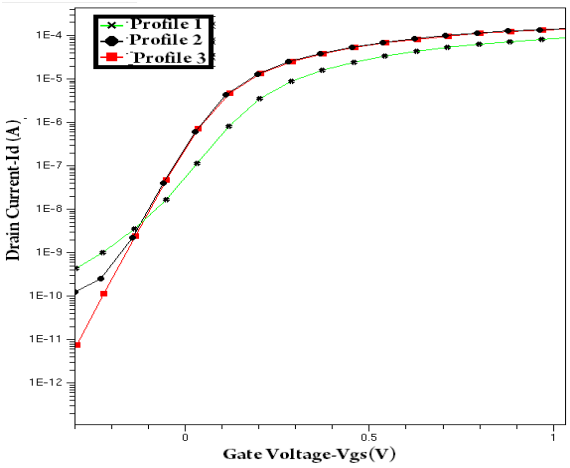


Fig 4: Subthreshold performance of Bulk FinFET using different channel doping profile

Profile III with low channel doping in active Fin(higher Fin) and high doping in lower Fin as well as in body, significantly improves the performance Fig 4. Subthreshold slope of profile reported in [14] is 78 mV/Decade and DIBL of device is 46 mV/decade which is a significant improvement over uniform low channel doping as discussed earlier.

3.2 Heavily doped Bulk FinFET

The high body doping is studied to improve bulk FinFET performance through punch through stopper which is used to reduce the punch through effect. As a result the drain and source depletion regions will become smaller and will not establish a parasitic current path. In this section of work, Bulk FinFET with heavy body doping (punch through stopper doping)[14] simulated for optimum value of doping. Table 2, gives the performance analysis of Bulk FinFET with different body doping. Further, it gives the optimum value of doping level for suitable I_{ON}/I_{OF} ratio.

Table 2. Performance of Bulk FinFET for different body doping

Body Doping (cm^{-3})	1×10^{16}	1×10^{17}	1×10^{18}	1×10^{19}
SS (mV/decade)	88.2	84.7	78.1	82
DIBL (mV/V)	83.1	77.2	71.1	69.3
I_{ON} (A)	0.28	0.13	0.12	0.06
I_{OFF} (A)	9×10^{-7}	8×10^{-8}	1×10^{-9}	4×10^{-7}

Fig 5. verifies the effect of band to band tunneling for heavy body doping FinFET structures. From low body doping to moderate body doping performance is improving with increase in body doping but significant degradation in performance is noticed for very high body doping. From graphs and I_{ON}/I_{OFF} analysis moderate body doping (1×10^{18}) is considered best for high performance applications.

Since a higher bulk doping increases the subthreshold swing at the same time, this method is not the most efficient one to reduce drain-source leakage.

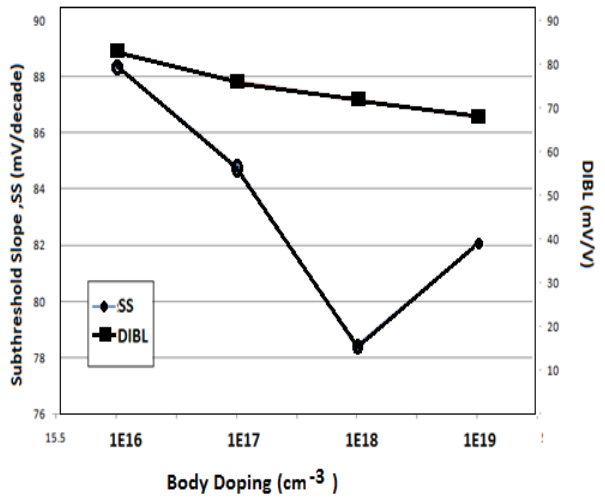


Fig 5: Plot showing optimum body doping value for DIBL and SS

3.3 Pie Gate Bulk FinFET with Punch through stopper

The pie gate Bulk FinFET, with misalignment of bottom of gate and source/drain body junction depth is simulated. ΔX (nm) is the amount of misalignment. Positive value of ΔX indicates that source/drain body junction is deeper than bottom of gate. Negative value indicates opposite behavior. The Bulk FinFET having shallower source/drain junction than bottom of gate (negative ΔX) shows better performance than normal Bulk FinFET (ΔX=0) as reported in [15]. Table 3 shows that the subthreshold performance is improved with negative value of misalignment ΔX. We can further improve the performance by changing the doping profile of Fin and body with pie-gate structure.

Table 3. Subthreshold performance with negative value of ΔX

Parameter	channel doping cm-3	DIBL(mV/V)	SS(mV/decade)
Misalignment	**1×16**	107.71	119.06
Δx=10nm	**1×17**	38.44	75.5
	1×18	36.48	72.53
	1×19	34.22	87.58
Parameter	**channel doping cm-3**	**DIBL(mV/V)**	**SS(mV/decade)**
Misalignment	**1×16**	80.56	88.92
Δx=20nm	**1×17**	24.93	69.83
	1×18	26.49	72.68
	1×19	25.55	88.79

For lightly doped Fin DIBL of Bulk FinFET having ΔX=-10 is 108 mV/V and Subthreshold slope is found to be 119 mV/decade for ΔX=-20 these values are 80.5 mV/V and 89mV/decade respectively. For Highly doped Fin DIBL of Bulk FinFET having ΔX=-10 is 36 mV/V and Subthreshold slope is found to be 72.53 mV/decade for ΔX=-20 these values are 26.5 mV/V and 72.68 mV/decade respectively. Graph showing relation between channel doping and SS is shown in Fig 6. Higher value of ΔX improves short channel performance of Bulk FinFET but for low Fin doping the performance is not satisfactory.

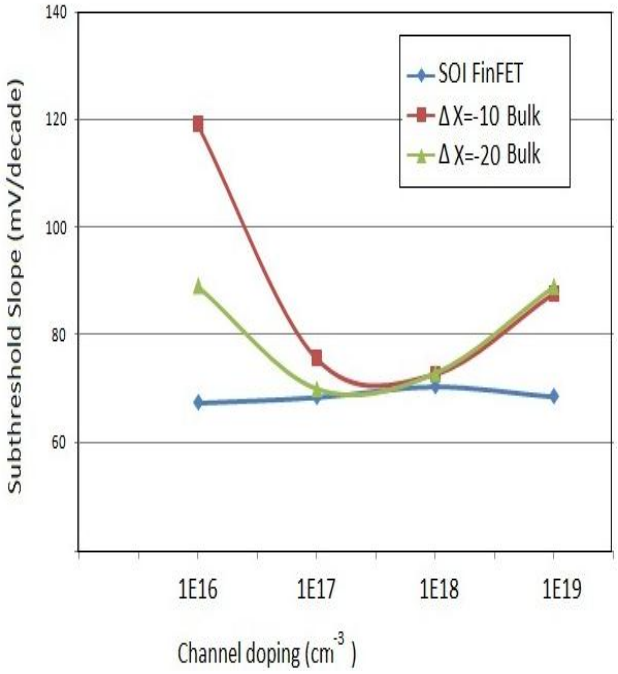


Fig 6: Effect of channel doping on Subthreshold Slope of pie gate Bulk FinFET and SOI FinFET

The new pie gate FinFET is doped with punchthrough stopper doping and characterized the performance. The heavy body doping bulk FinFET is simulated for ΔX=0nm, ΔX=-10nm & ΔX=-20nm. For ΔX=-10nm SS is 70.62 mV/decade and DIBL is 28mV/V. For ΔX=-20nm SS is 60 mV/decade and DIBL is 25.6 mV/decade. It is clear that performance of device is significantly better than previously reported profile and also its value is compared with SOI FinFET. A graph of DIBL and Subthreshold slope is plotted for different bulk structures Fig 7 & Fig 8. The subthreshold performance is also studied with variation in channel doping with different Fin structures(Fig 6). It is observed that device with heavy Bulk doping with misalignment ΔX=-20nm has subthreshold performance is almost similar to the SOI FinFET. All the simulations are done to keep the performance of the device according to the IRTS [17] requirements.

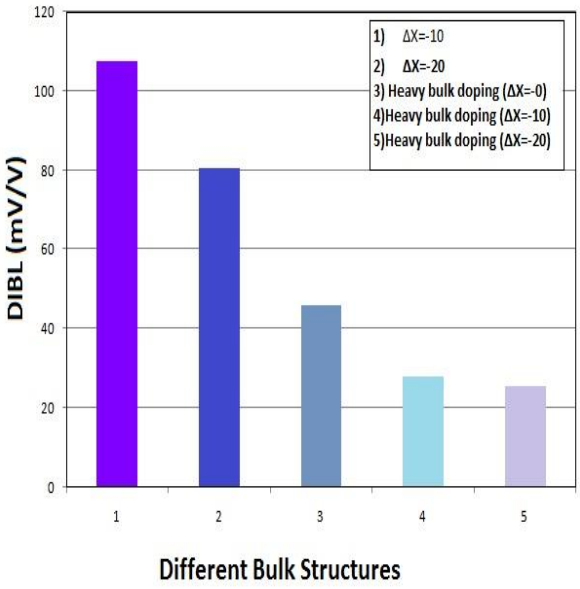


Fig 7: DIBL Characteristics for different bulk FinFET structures

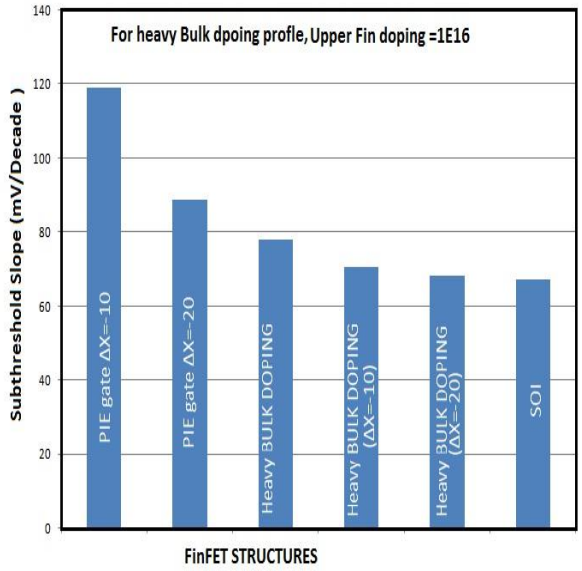


Fig 8: Subthreshold slope for different Bulk FinFET Structures

Simulated transfer characteristics are shown in Fig 9 (a) for SOI FinFET and bulk FinFET with source/drain junction depths extended underneath the gate by ΔXj = 0 nm (gate-bottom aligned to the junction depth) and ΔXj = 20 nm. SOI FinFET has drain-induced barrier lowering (DIBL) of 51.3 mV/V and subthreshold swing of 79.2 mV/Decade, whereas bulk FinFET with junctions aligned to the bottom of the gate has DIBL of 62.8 mV/V and S of 91.2 mV/Decade. Higher value of subthreshold slope and DIBL of bulk FinFET can be can be attributed to higher dielectric constant of depleted silicon compared to SiO_2, which guides the drain electric field towards the source underneath the gate. The gate-induced drain leakage is responsible for the current increase in accumulation. An increase of the source/drain junction depths by ΔXj = 20 nm with respect to the bottom of the gate deteriorates bulk FinFET characteristics greatly; having DIBL of 173.6 mV/V and SS of 212 mV/ Decade, due to low gate controllability of the bottom of the channel.

Simulated output characteristics is shown in Fig 9 (b). The output characteristics are closely spaced with bulk FinFET output resistance decreasing as junction depth is increasing, due to DIBL effect. The bulk FinFET has good performance in saturation regardless of source/drain junction depth. All these results show the importance of process variation control when the alignment between the gate-bottom and junction depth is concerned. The idea of making the S/D-to-body junctions shallower so that the polysilicon gate electrode controls the whole channel and part of the Fin under the active area comes from the Pi-gate FinFET structures.

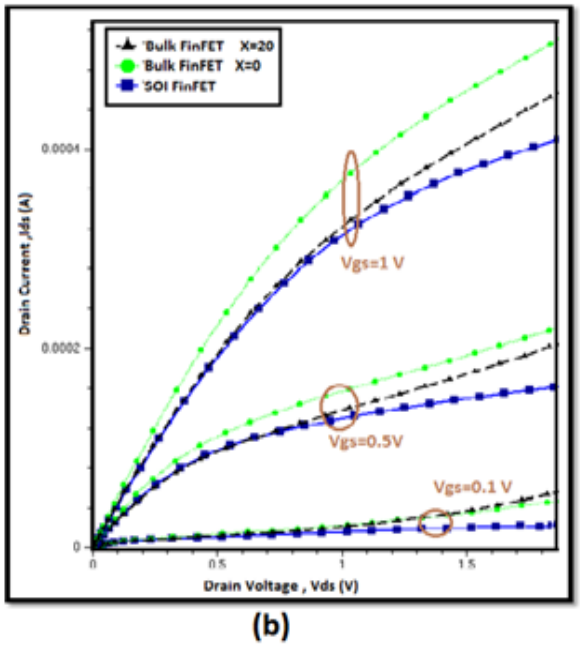
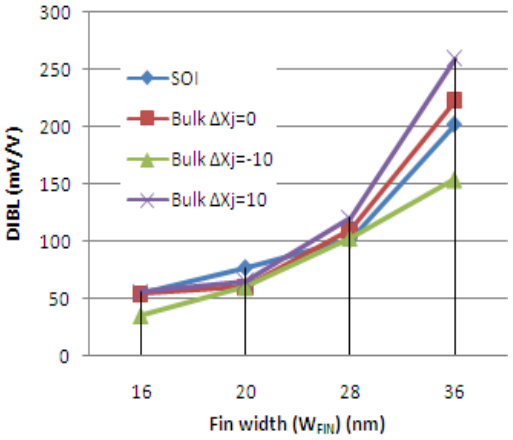
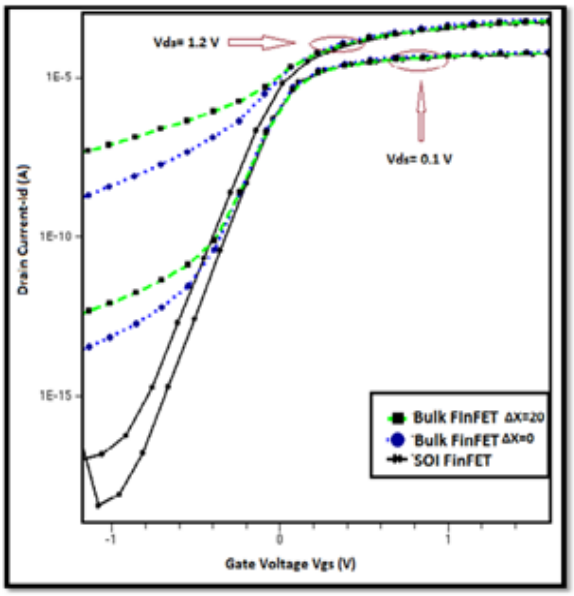


Fig 9 (a)) Transfer characteristics of different FinFET Structures (b) Output characteristics of different FinFET Structures

3.4 Effect of Fin Width (W_{Fin}) variations on Pie-gate FinFET Performance

The performance of FinFET is also depends on the Fin width. Low value of W_{FIN} leads to better control of gate over the channel, so value of W_{FIN} should be low to obtain better performance. Dependences of DIBL and SS on Fin width for different structures with a misalignment ΔXj as a parameter are shown in Fig 10(a),(b) respectively. An increase in SS and DIBL for all structures with increasing W_{FIN} is caused by the decreased gate control in wider Fins[15]. It can be noted that bulk FinFETs with wider fins are more sensitive to S/D junction depth; deeper junctions can deteriorate and shallower junctions can improve device characteristics substantially. Bulk FinFET with ΔXj = -10 nm (shallower junctions) has equal or even better subthreshold performance than the SOI Fin- FET, especially in the case of wider Fins, e.g. W_{FIN} = 36 nm.





(a)

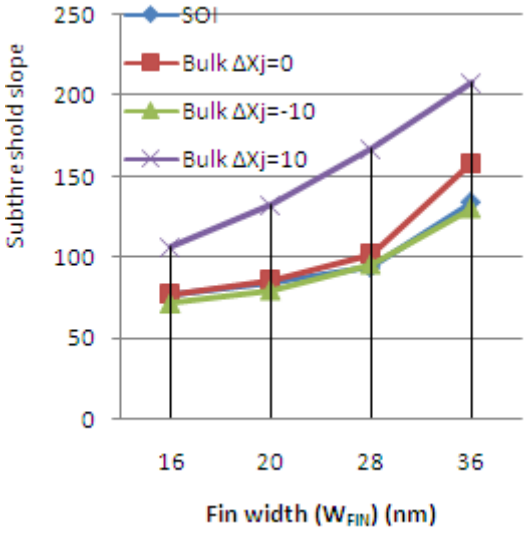


Fig 10 (a) DIBL versus fin width for SOI FinFET and for bulk FinFET with different S/D junction depths (b) Subthreshold swing versus Fin width for SOI FinFET and for bulk FinFET with different S/D junction depths

4. CONCLUSION

The performance of Bulk FinFET can be improved with non uniform channel doping using low channel doping in higher Fin and high doping in lower Fin as well as in body. Further, we can improve the performance with shallower source/drain junction than bottom of gate (i.e. negative value of ΔX). For pie gate FinFET, heavy body doping is used to improve subthreshold performance shown in table 4. It means that Pie gate Bulk FinFET structure for non uniform channel doping along with heavy body doping (i.e. Punchthrough stopper), is suitable candidate for approximately ideal subthreshold performance. Also, its performance is compared with SOI FinFET.

Table 4 Subthreshold performance of heavily doped pie-gate Bulk FinFET

Misalignment(nm)	SS(mV/decade)	DIBL(mV/V)
Δx=0	78.002	46.01
Δx=-10	70.62	27.87
Δx=-20	68.24	25.67

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