Quantum Cost Realization of Reversible Barrel Shifter

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ABSTRACT
This paper presents an efficient design of a reversible barrel shifter. It has also been shown that the new circuit outperforms the previously proposed one in terms of number of gates, number of garbage outputs, delay and quantum cost.

Keywords
Reversible Logic, Garbage output, Fredkin Gate, Feynman Gate, Quantum cost.

1. INTRODUCTION
Reversible system does not allow information to be erased. Thus the reversible gates have the same number of inputs and outputs which means that the input stage can always be retained from the output stage. For the reversible computer the heat dissipation is exactly $kT\ln 1$ which is logically zero. Thus reversible computation is a highly potential field for upcoming low power/high performance computing.
Designing reversible circuits using reversible gates have several constraints [3]:
a. The fan-out of every signal is equal to one.
b. Loops are not permitted in a strictly reversible system.

2. BASIC DEFINITIONS
In this, section we present some definitions on reversible logic gates and their quantum cost. A Reversible Gate is an n-input, n-output (denoted by n * n) circuit that uniquely maps the output vector Ov to the corresponding input vector I_v where $I_v = (I_0, I_1, I_2 \ldots I_{k-1}, I_k,)$ and $O_v = (O_0, O_1, O_2 \ldots O_{k-1}, O_k)$.

Definition 1. The input vector, Iv and output vector, O_v for 2*2 Feynman Gate (FE) is defined as follows: $I_v = (A, B)$ and $O_v = (P = A$ and $Q = A \oplus B)$. Fig 1 shows the block diagram of the reversible Feynman gate.
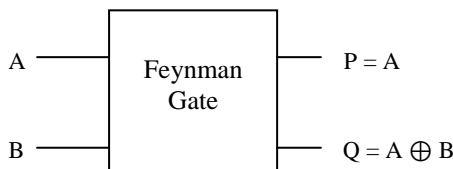

Fig 1: Feynman Gate

Definition 2. The input and output vector for 3*3 Fredkin gate (FR) are defined as follows: $I_v = (A, B, C)$ and $O_v = (P=A, Q= AB \oplus AC$ and $R = AC \oplus AB)$. Fig 2 shows the block diagram of a 3x3 Fredkin gate. The quantum cost of FR is also 5.
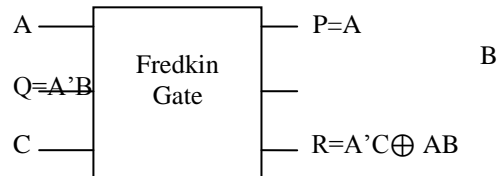

Fig 2: Fredkin Gate

Definition 3. To maintain the reversibility property of reversible logic gates several dummy output signals are needed to be produced in order to equal the number of input to that of output. These signals are commonly known as Garbage Outputs. The garbage output is denoted by P in Fig 1.

Definition 4. The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line.

3. BARREL SHIFTER
A barrel shifter is a combinational circuit which has n-input and n-output and m select lines that controls bit shift operation.

4. REVERSIBLE BARREL SHIFTER
In this section we will discuss about the reversible barrel shifter and then make comparative study between the existing and the proposed one. Shifter is a unidirectional logarithmic shifter consists of multiplexers. A 3x3 Fredkin Gate works as simple (2:1) multiplexers. Feynman gates are used for producing fan outs. The shifter with n-bit data value and k-bit shift value will require the following number of gates according to [4].

Number of Fredkin Gates $f = (2k-1) \times n$.
Number of Feynman Gates $g = n \times (2k-1)$.
Number of Garbage Outputs $GO = f + k = k + [(2k-1) \times n]$.
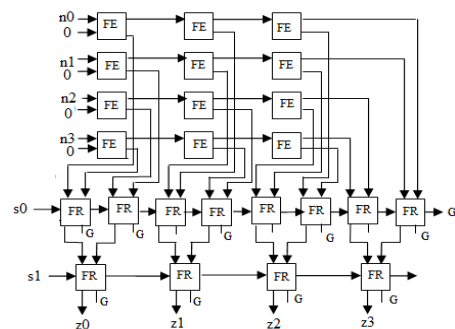The shifter with 4-bit data value and 2-bit shift value is shown in Fig 3.

Fig 3: Reversible (4, 2) Barrel shifter

This shifter is complex in design and requires large number of gates. As a result the total number of garbage outputs is high. Thus there is great room for improving the circuit complexity, total number of gates and garbage outputs, delay and quantum cost.

Algorithm: Shift/Rotate operation of an (n, k) Barrel shifter.

Input: Data Input Set I (io, i1 … in-1), n = total number of data input bit.
Control input Set S (s0, s1, … sk), k = log2 (n).
Output: Desired shift/rotate output set O (o1, o2,… oi).
begin
Step 1: for k <- 0 to log2(n)
Step 2: do if sk = 1
Step 3: then left shift /rotate I 2k times
Step 4: else I remains same
end.

5. LEFT SHIFT/ROTATE REVERSIBLE BARREL SHIFTER

For efficient designing of a reversible circuit several criteria:
a. Minimize the number of gates as possible.
b. Minimize the quantum cost of the circuit.
c. Total number of garbage outputs and usage of constant inputs should be minimized.

By maintaining the above parameters and observing the previous design, we have a novel logarithmic Reversible Barrel Shifter. The Existing Barrel shifter is a left rotating shifter which uses Fredkin gates for reversible (2:1) multiplexing and Feynman Gates for producing fan outs.

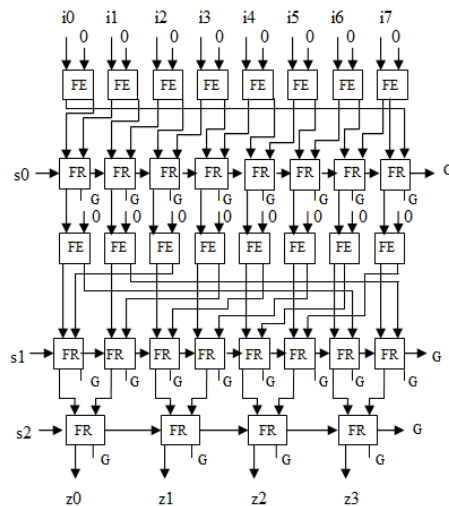Design of Existing (8, 3) Reversible shifter is as shown in fig 4.

Fig 4: Existing Reversible (8, 3) Barrel shifter

6. PROPERTIES OF THE EXISTING REVERSIBLE BARREL SHIFTER

From the above explanation and designing procedure we will now present several important properties of the Existing (n, k) reversible barrel shifter.

Theorem 1. A unidirectional reversible barrel shifter with n-bit data input and k-bit shift value can be realized with at least Fr number of Fredkin Gates for multiplexing where,

$$Fr = n (k-1) + n/2$$

Theorem 2. Let n be the total number of data input bits and k be the shift value bit of a unidirectional reversible shifter. Let Fe be the total number of Feynman Gates for producing fan outs, then

$$Fe = n (k-1)$$

Theorem 3. Let n be the total number of data input bit and k be the shift value of a unidirectional reversible barrel shifter. Let GO be the total number of garbage outputs of the proposed shifter, then

$$GO = n (k-1) + k$$

7. PROPOSED REVERSIBLE LOGICAL SHIFTER

In this section we designed the Reversible logical left shifter. Proposed (8, 3) Reversible Logical shifter is as shown in fig 5.
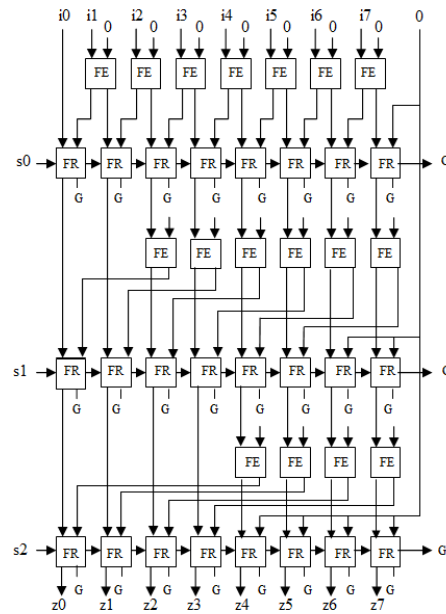

Fig 5: Proposed Reversible Logical(8, 3) Barrel shifter

8. PROPERTIES OF THE PROPOSED

Several important properties of the proposed (n, k) reversible Logical shifter is as discussed below.

Theorem 1. Unidirectional reversible Logical shifter with n-bit data input and k-bit shift value can be realized by Fredkin and Feynman Gates, which can be calculated as,

$$Fr = n (k-1) + n$$

Theorem 2. Let Fe be the total number of Feynman Gates for producing fan outs, then

$$Fe = n (k-1) +1$$

Theorem 3. Let GO be the total number of garbage outputs of the proposed Logical shifter, then

$$GO = n \, (k) + k$$

9. COMPARATIVE STUDY BETWEEN THE REVERSIBLE BARREL SHIFTERS

Comparing with the existing barrel shifter to the proposed, we observe the result shown in Table 1 and Table 2. From Table 1 we can see that the proposed circuit requires less number of gates, produce less garbage outputs. The delay costs (*D*). The quantum cost of the circuit, calculated according to the [9], is also shown in Table 2.

Table 1. Comparative study of the reversible barrel Shifters

(n, k)	Criteria	Barrel shifter	Existing Barrel shifter/ rotator	Proposed Logical Barrel shifter
(4, 2)	FR	12	6	8
	FE	12	4	5
	GO	14	6	10
	D	10	6	9
(8, 3)	FR	56	20	24
	FE	56	16	17
	GO	59	19	27
	D	35	14	12
(16, 4)	FR	240	56	64
	FE	240	48	49
	GO	244	52	68
	D	132	28	26

Table 2. Comparison of the quantum cost of the barrel shifters

(n, k)	Barrel Shifter	Existing Barrel shifter/rotator	Proposed Logical Barrel shifter
(4, 2)	72	34	45
(8, 3)	336	116	137
(16 ,4)	1440	328	369

10. CONCLUSION

The comparison table clearly shows that proposed Barrel shifter/ rotator requires less number of gates and also reduces in the delay and quantum cost of circuit. Therefore barrel shifters which are capable of performing n-bit shifting and rotating of data in a single cycle, are normally used in embedded processors such as: digital signal processors and high performance processors, high-speed/low-power Applications etc.

11. REFERENCES

[1] Rolf Landauer, "Irreversibility and Heat Generation in the Computing Process."

[2] C.H. Bennett, "Logical reversibility of computation".

[3] Gorgin, S.; Kaivani, A, "Reversible Barrel Shifters," Computer System and applications,

[4] E. Fredkin, T. Toffoli, Conservative logic.

[5] Edward Fredkin and Tommaso Toffoli, "Conservative Logic,"

[6] Wayne Wolf , Modern VLSI design.

[7] Paul Gigliotti, Implementing Barrel Shifters Using Multipliers, XAPP19.

[8] Pillmeier, Matthew R.;Schulte, Michael J.;Walters, Eugene G., "Design alternatives for barrel shifters, ".

[9] Hafiz Md. Hasan Babu, Md. Rafiqul Islam, Ahsan Raja Chowdhury and Syed Mostahed Ali Chowdhury, "Reversible Logic Synthesis for Minimization of Full-adder Circuit

[10] Ashis Kumer Biswas, Lafifa Jamal and Hafiz Md. Hasan Babu, "An Efficient Design of Parallel Loading Shift Register Using Reversible Flip-Flops".

[11] Ashis Kumer Biswas, Md. Mahmudul Hasan, Ahsan Raja Chowdhury, Hafiz Md. Hasan Babu, "Efficient approaches for designing reversible binary coded decimal adders".