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A Low Power 90nm Technology based CMOS Digital Gates with Dual Threshold Transistor Stacking Technique

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ABSTRACT

Scaling of transistor features sizes has improves performance, increase transistor density and reduces the power consumption. A chip's maximum power consumption depends on its technology as well as its implementation. As technology scales down and CMOS circuits are powered by lower supply voltages, leakage current becomes significant. static power is becoming the predominant source of energy waste. To create methodologies that support efficient designs, good performance, lower costs in the era of low power, is up to the design, EDA community . As the threshold voltage is reduced due to scaling, it leads to increase in sub threshold leakage current and hence increase in static power dissipation. This paper presents performance analysis of inverter using conventional CMOS, stack and dual threshold transistor stacking techniques. The performance analysis of inverter were analyzed in 90nm technology using Cadence virtuoso environment. The use of dual threshold voltages can significantly reduce static power dissipated in CMOS VLSI circuits.

General Terms:

Low Power Design

Keywords:

CMOS inverter, static power, threshold voltage, transistor stacking, ULSI.

1. INTRODUCTION

In early 1970's, providing high speed operation with minimum area were main aim of design. Many design tools are concentrated to achieve these goals. ITRS reported that leakage power consumption may come to dominate total chip power consumption as technology feature size shrinks [7,8]. As we can observed that static consumption tends to increase over the year as dynamic power consumption [8]. The increasing prominence of portable systems and the need to limit power consumption in very high density ULSI chips have lead to rapid and innovative development in low power design. Due to power sensitive portable devices, low power is very important requirement of all high performance application where power is one of the important design constraints. In today's era of VLSI,

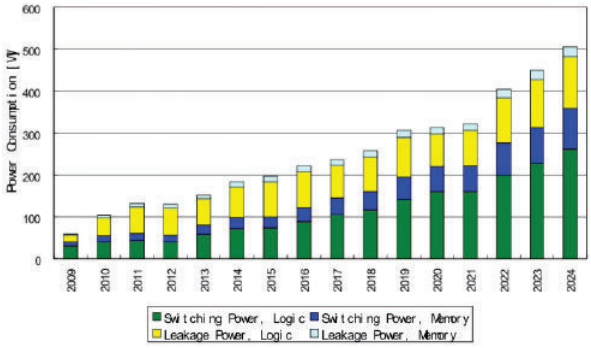


Fig. 1. **Power consumption prediction by the ITRS 2009[8].**

power consumption control and management has become a key challenge and critical issue in electronics industry. The advancement in VLSI technology allows integrating a complete system on chip (SoC) providing facility to develop a portable system. Power dissipation is a critical parameter in battery operated portable device. The limited battery Lifetime typically imposed very strict demands on the overall power consumption of the portable systems. Power consumption is one of the important factors of VLSI circuit design for CMOS is the primary technology. The power consumption has become a fundamental problem in VLSI circuit design. Therefore, reducing the power consumption of integrated circuits through design improvement is a major challenge in portable system design. To solve the power consumption problem, many different techniques from circuit level to device level and above have been proposed by researchers. However, there is no straight forward ways to meet the tradeoff between power, delay and area. The designers are required to choose appropriate techniques that satisfy the application and product needs [2]. Reducing power dissipation varies from application to application. The key objective in reducing power consumption is to reduce the overall cost of the product. One of the most challenging problem is to find out new and effective circuit design technique to reduce the overall power dissipation without compromising the performance of the device. Scaling advanced CMOS technology improves high performance and high transistor density. The power dissipation of a chip depend

not only on its technology but also on its implementation i.e on size, circuit style, operating frequency and so on. Because of this technology trends transistor leakage power has increased exponentially supply voltage scaling increases sub-threshold leakage current, increases leakage power and pose numerous leakage in the VLSI design. Therefore static power has become a significant portion of the total power consumption. There are several VLSI techniques to reduce leakage power. Different techniques provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each techniques. In this paper an efficient subthreshold leakage current reduction and optimization methods are presented and result are given for 90nm generic process design kit technology using virtuoso schematic editor.

2. REVIEW OF PREVIOUS WORK

2.1 Conventional CMOS technique

Fig.2. shows the block diagram of digital circuit using conventional CMOS techniques. In this technique, a fully complementary CMOS circuit has an nMOS pull down network to connect the output to '0' (GND) and pMOS pull up network to connect the output to '1' (VDD).

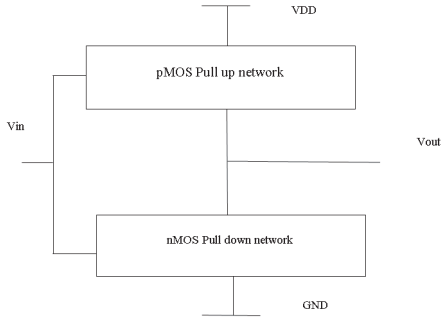


Fig. 2. **Base case (conventional CMOS) circuit structure.**

2.2 Forced Transistor Stacking Technique

This technique is based on the fact that natural stacking of MOSFET helps in achieving leakage current. The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect [4]. An effective way to reduce leakage power in active mode is stacking of transistor [1].

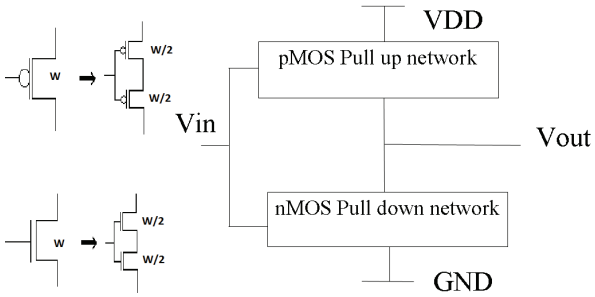


Fig. 3. **Forced Stack Technique circuit structure.**

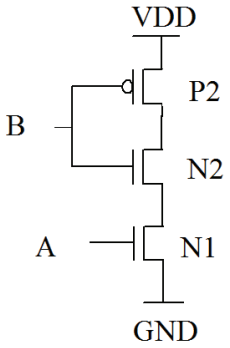


Fig. 4. **Circuit Schematic of Forced Stack Technique[6]**

The subthreshold leakage is exponentially related to the threshold voltage of the device and threshold voltage changes due to body effect. The source of the nMOS device N1 is connected to ground. Transistor N2 source is connected to drain of N1. The source of N2 is not grounded and it can acquire voltages close to Vdd while its substrate is connected to ground. Therefore the condition Vsb=0 will not hold in bias cases for transistor N2. The device N1 will experience higher Vth due to the difference in the voltage between the source and body. The voltage between drain and source also decreased since the intermediate node has a voltage above the ground resulting reduction in DIBL affect and hence effective saving of leakage power. For turned off the single transistor,leakage current Isub0 can be expressed as follows[3,11]:

$$I_{sub0} = Ae^{\frac{1}{nV\theta}(V_{gso}-V_{tho}-\gamma V_{sbo}+\eta V_{dso})}(1-e^{\frac{V_{dso}}{V_\theta}}) \quad (1)$$

$$= Ae^{\frac{1}{nV_\theta}(-V_{tho}+\eta V_{dd})} \quad (2)$$

$$A = \mu_0 C_{ox}(W/L_{eff})V_\theta^2 e^{1.8} \quad (3)$$

n=sub-threshold coefficient V=thermal voltage Vgs0, Vth0, Vbs0 and Vds0 are the gate-to-source voltage, the zero-bias threshold voltage, the base -to-source voltage and the drain-to-source voltage respectively. γ is the body-bias effect coefficient, and η is the Drain Induced Barrier Lowering (DIBL) coefficient. μiszero-bias mobility, Cox is the gate-oxide capacitance, W is the width of the transistor, and Leff is the effective channel length.
Two transistor are turned off together (M1=M2). So,

$$I_{sub1} = Ae^{\frac{1}{nV_\theta}}(V_{gs1}-V_{tho}-\gamma V_{sb1}+\eta V_{ds1})(1-e^{\frac{v_{ds1}}{V_\theta}}) \quad (4)$$

$$= Ae^{\frac{1}{\eta V_\theta}}(-V_x-V_{tho}-\gamma V_x+\eta(V_{dd}-V_x)) \quad (5)$$

$$I_{sub2} = Ae^{\frac{1}{nV_\theta}}(V_{gs2}-V_{tho}-\gamma V_{sb2}+\eta V_{ds2})(1-e^{\frac{V_{ds2}}{V_\theta}}) \quad (6)$$

$$= Ae^{\frac{1}{nv_\theta}(-V_tho+\gamma V_x)}(1-e^{-V_x/V_\theta}) \quad (7)$$

Where Vx is the voltage at the node between M1 and M2. Now consider X is the factor of Isub0 and Isub1 (==Isub2)

$$X = \frac{I_{sub0}}{I_sub1} = \frac{Ae^{\frac{1}{nV\theta}(-V_{tho}+\eta V_{dd})}}{Ae^{\frac{1}{nV_\theta}(-V_x-V_{tho}-\gamma V_x+\eta(V_{dd}-V_x))}} = e^{\frac{V_x}{\eta V_\theta}(1+\gamma+\eta)} \quad (8)$$

If Isub1=Isub2 then from equation (4.8) we can write,

$$1 = e^{\frac{1}{nV_\theta}(\eta V_{dd} - V_x(1+2\eta+\gamma))} + e^{\frac{-V_x}{V_\theta}} \quad (9)$$

Threshold voltage can be controlled by body bias effect.

$$V_{th} = V_{t0} + \gamma(\sqrt{V_{sb}}) \quad (10)$$

Changing the substrate voltage causes the threshold voltage to change. So the different kind of effect is arises for changing the substrate voltage like Zero-Body Bias, Reverse-Body Bias and Forward-Body Bias. This Phenomenon is frequently used for controlling the threshold voltage. γ constant dependent on the transistor parameter and the technology feature size. By controlling body biasing effect with changing the constant term we can easily control the leakage power[3,10].

2.3 Sleep Transistor Technique

This technique uses the sleep transistor between both VDD and the pull up network and between GND and pull down network [3]. The sleep transistor turn off the circuit by cutting off the power rails in idle mode thus can reduce leakage power effectively.

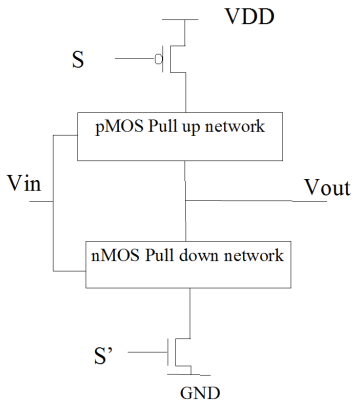


Fig. 5. **Sleep Transistor Technique Structure.**

In this technique we have floating values and thus will lose state during sleep mode. The Wakeup time and energy of the sleep technique have significant impact [3]. The technique in which high Vth sleep transistor are used called Multi-threshold voltage CMOS (MTCMOS) proposed by Motoh et al. [3].

2.4 Dual Threshold Transistor Stacking Technique

This new technique called dual threshold transistor stacking hybrid version of stack and MTCMOS. It takes the advantage of both above techniques i.e. sleep transistor are redesigned with stack effect. The size of sleep transistor is reduced. The sleep transistors are designed as a high threshold voltage [1]. Fig.6 shows the circuit schematic of Dual threshold transistor stacking technique.

3. SIMULATION RESULTS

Simulations have been performed using virtuoso in 90nm gpdk CMOS technology with supply voltage 1.2V to estimate the power consumption. The Inverter and two input NAND circuit are chosen to compare the different techniques. The propagation delay is measured at 1kHz frequency. The resulting schematic diagram and output waveforms are shown from fig. 7 to fig. 10.

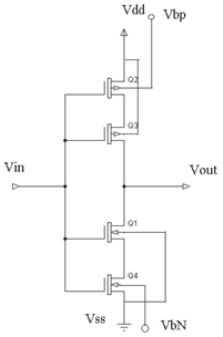


Fig. 6. **Dual Threshold Transistor Stacking Technique.**

Table 1 :Physical aspects of MOS transistor using CMOS techniques

Physical Aspects	nMOS Transistor	pMOS transistor
Channel width (μm)	0.3	0.6
Channel length (μm)	0.1	0.1
Aspect Ratio	3	6

Table 2 : Physical aspects of MOS transistor using stack techniques

Physical Aspects	nMOS Transistor	pMOS transistor
Channel width (μm)	0.15	0.3
Channel length (μm)	0.1	0.1
Aspect Ratio	1.5	3

Table 3: Physical aspects of MOS transistor using DTTS techniques

Physical Aspects	nMOS Transistor	pMOS transistor
Channel width (μm)	0.15	0.3
Channel length (μm)	0.1	0.1
Aspect Ratio	1.5	3

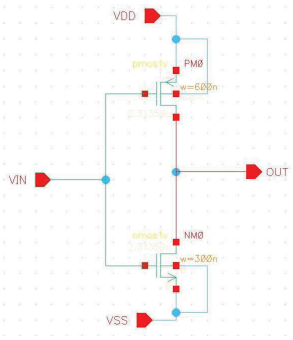


Fig. 7. **Inverter with Conventional technique.**

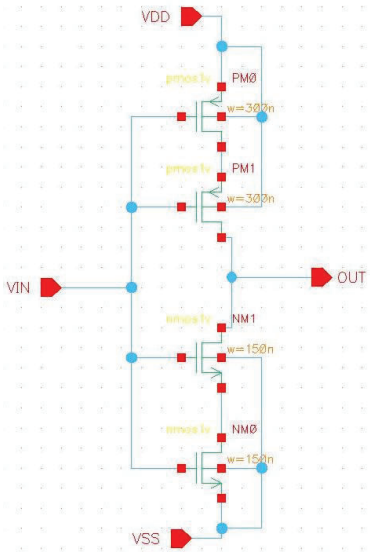


Fig. 8. **Inverter with Forced Stack technique.**

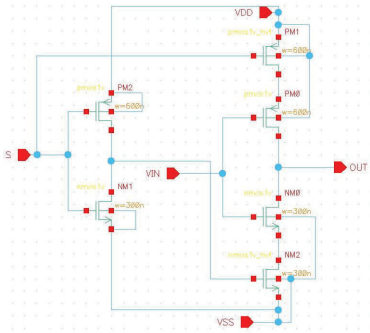


Fig. 9. **Inverter with Sleep Transistor technique.**

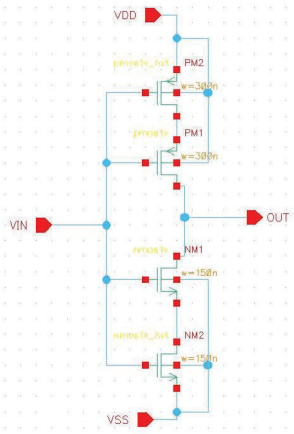


Fig. 10. **Inverter with Dual Threshold stack transistor technique.**

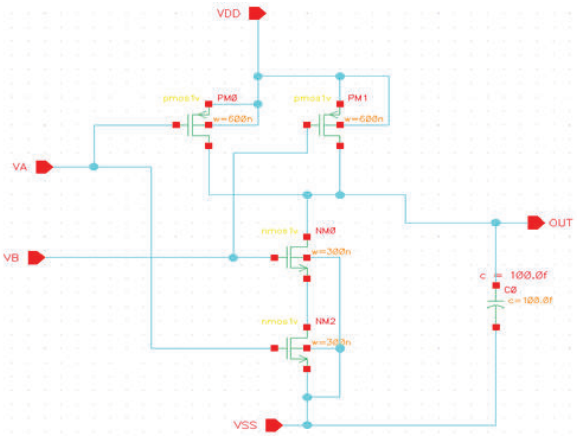


Fig. 11. **NAND with Conventional technique.**

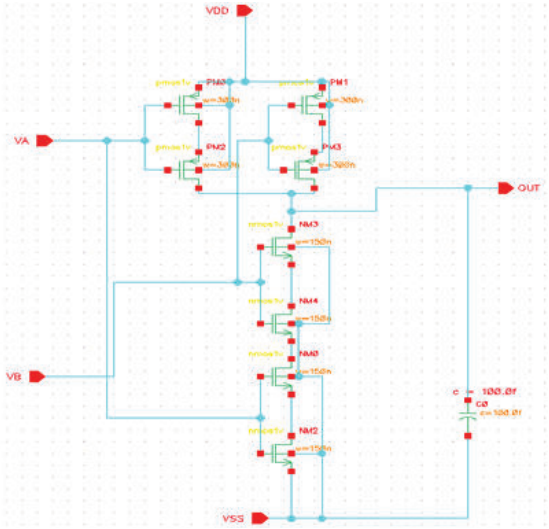


Fig. 12. **NAND with Forced Stack technique.**

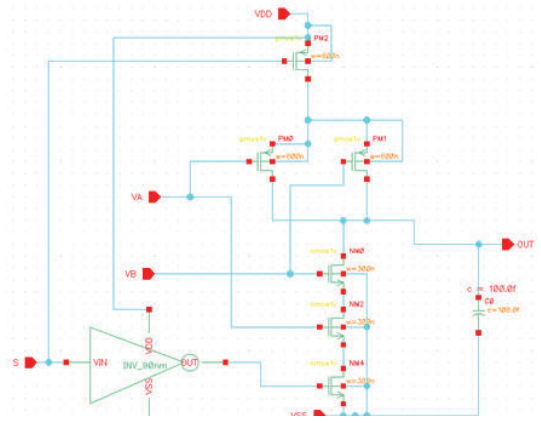
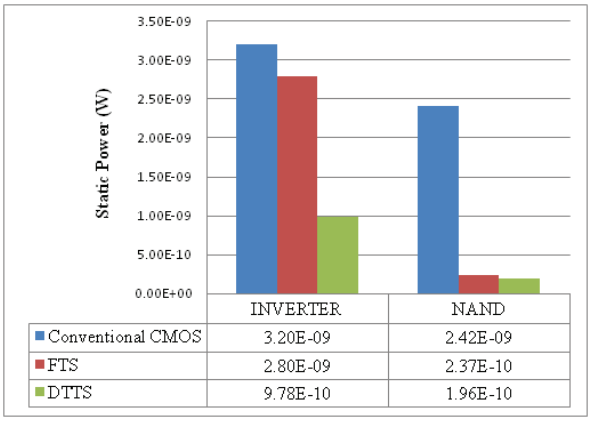
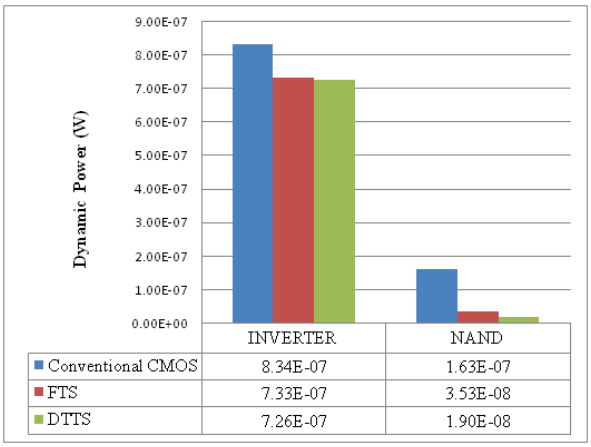


Fig. 13. **NAND with Sleep Transistor technique.**



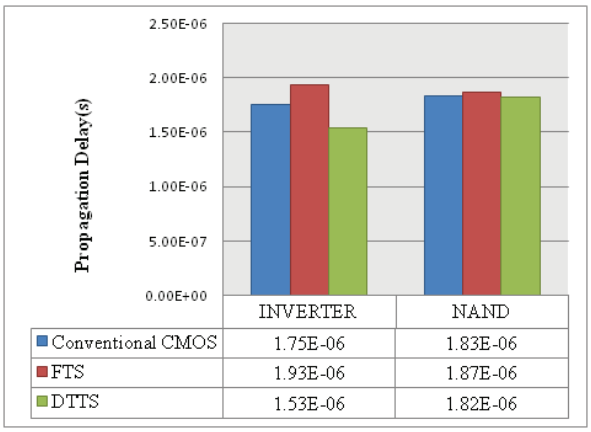
	INVERTER	NAND
Conventional CMOS	3.20E-09	2.42E-09
FTS	2.80E-09	2.37E-10
DTTS	9.78E-10	1.96E-10

Fig. 14. **Static Power Comparison chart.**



	INVERTER	NAND
Conventional CMOS	8.34E-07	1.63E-07
FTS	7.33E-07	3.53E-08
DTTS	7.26E-07	1.90E-08

Fig. 15. **Dynamic Power Comparison chart.**



	INVERTER	NAND
Conventional CMOS	1.75E-06	1.83E-06
FTS	1.93E-06	1.87E-06
DTTS	1.53E-06	1.82E-06

Fig. 16. **Propagation Delay Comparison chart.**

4. CONCLUSION

The CMOS inverter is most important and used in all digital as well as analog applications. The optimization of the inverter becomes very important. The leakage power is of great concern for designs in nanometer technologies. As the technology scaling goes below 90nm, the standby leakage power dissipation has become a critical issue. To reduce the standby leakage power, this paper has presented a novel design technique. The results show the proposed technique is a viable solution for high energy reduction in CMOS circuits. In proposed technique no area penalty demand compared to force stack technique. The DTTS technique may be considered as an alternate for FTS technique. Power reduction varies with different techniques. The optimization of leakage power subjects to performance metrics and active area increase constraints. This technique mentioned in this paper can be implemented in low power VLSI circuit and reduce the power consumption of the chip which will increase battery life. For our Future work,we plan to calculate the area of the various approaches using layout and design of various combinational and sequentially circuits using proposed method.

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