VLSI Implementation of 4-bit 50Gbps High Speed Pipelined ADC Architecture for I-UWB Receiver

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ABSTRACT
In this work, a 4-bit pipelined ADC that provides the high speed conversion needed in UWB applications with sampling frequency of the order 50 Gbps is proposed. The pipelined ADC designed uses a high speed 1-bit comparator, wide band amplifier, sampling circuit and a high speed buffer. The individual blocks are designed using 130nm CMOS low power library cells. The individual blocks are designed to operate at a frequency greater than 50 Gbps sampling rate. In order to operate increase the operating frequency of the pipelined ADC, Specific new design techniques/algorithms such as power-efficient, capacitor ratio-independent conversion scheme, a pipeline stage-scaling algorithm, a nested CMOS gain-boosting technique, an amplifier and comparator sharing technique, and the use of minimum channel-length, thin oxide transistors with clock bootstrapping and in-line switch techniques are adopted.

General Terms

Keywords
I-UWB receiver, pipelined ADC, high speed, CMOS gain boosting, clock boot strapping

1. INTRODUCTION
UWB based applications use 3.1GHz to 10.6 GHz band for operation. The advantages of UWB communications are that they provide high data rate of 100Mbps – several Gbps (1-50 meters) [1], [2] and an effective isotropic radiated power (EIRP) of −41.3 dBm/MHz. UWB communication applications are ground/wall penetrating radar, through wall imaging, medical imaging, wireless sensor networks and surveillance applications. It is desirable to build applications on single chip solutions that can have both analog and digital processing. The bottleneck in existing SoC based design is the output power capability of RF receivers as they are band limited by the active devices used in the RF section [3]. SiGe and GaAs technology were adopted for RF receivers due to their high power requirements. For applications mentioned it is required to consume low power, thus RF transreceivers with impulse based UWB need to consume very low power, hence CMOS technology is found to be most preferred for implementation. CMOS also offers the possibility of a complete UWB application on System-on-Chip (SOC). There are two major challenges for the implementation of CMOS digital UWB radios. The first is building RF and analog circuitry covering wide bandwidth over several GHz [4]. The second is sampling and digitizing high frequency signals in the UWB frequency range of 3 GHz to 10 GHz, which is not feasible for existing CMOS analog-to digital converters. Analog I-UWB receivers correlate the incoming signal from the LNA with a template signal for pulse matching. The template matched pulse is used for synchronization and demodulation. As template matching has to be synchronized, it is difficult for an analog UWB receiver to accurately control the timing of the signal reception, which degrades the performance [5]. Several methods to sample UWB signals were reported in (Gangyaokung 1995 [6], Donnell 2002 [7] and Namgoong 2003 [8]). The method reported in (Feng 2002 [9]) relies on a time-interleaving technique for multiple ADCs, in which each ADC samples the signal by equally time-spaced clock triggering. This method is highly sensitive to the timing jitter, so the time resolution capability of multiple clock signal generation dominates the sampling speed. Also, since each ADC has to sample a wideband signal, design of the front-end circuitry remains difficult. The alternative methods reported in (Gangyaokung 1995 [6] and Namgoong 2003 [8]) utilize a channelization technique. One problem with the channelization method lies in the use of non-ideal band pass filters, which lead to overlapping of transition bands to cause the aliasing problem. Therefore, high performance band pass filters are necessary for the channelization technique. To address the shortcomings of existing methods frequency domain sampling methods are adopted. In (Hyung-Jin Lee 2006 [10]), two different architectures for frequency domain I-UWB receiver with 1-bit ADCs and frequency channelized ADC using low pass filters is proposed and implemented. For low power applications, I-UWB with 1-bit ADCs is recommended however, it degrades the performance of the receiver by about 3 dB at BER of 10^{-1} compared to ideal ADCs and has very low data rates [11]. In this work, design of pipelined ADC architecture that can be used in I-UWB receiver is carried out.

This paper is organized as follows. Section II discusses the theoretical background of I-UWB receiver. Section III discusses the design specifications of ADCs for I-UWB receiver and design of high speed ADCs. The performance results and discussions are presented in Section IV. Finally, conclusions are drawn in Section V.

2. Background Theory

In February 2002, the Federal Communications Commission (FCC) opened the spectrum from 3.1 GHz to 10.6 GHz for unlicensed use of UWB technology (FCC 2003). The FCC ruling has generated considerable interest in developing UWB communication systems, and it has created several new opportunities for innovation and development. The great potential of UWB lies in the facts that it can co-exist with the users of already licensed spectrum and that it opens a wide range of applications. Such applications include high-speed wireless personal area networks (WPANs) and wireless USB (Scholtz 1997 [12]).

2.1 Ultra Wideband Signaling
UWB systems must be able to transmit and receive an extremely short duration burst of radio frequency (RF) energy

– typically from a few tens of picoseconds to a few nanoseconds in duration. These bursts may be formed by one or a few cycles of an RF carrier wave. Therefore the waveform is extremely broadband, and it is often difficult to determine the real RF center frequency, and thus, the term "carrier-free". There are basically two types of UWB communication: (i) impulse-based UWB (I-UWB) that is based on very short pulses and (ii) multicarrier UWB (MC-UWB) that is based on multiple simultaneous carrier signals (Fontana 2002 [13]).

2.2 Impulse-based UWB

Unlike classical communication systems, impulse-based UWB (I-UWB) does not use a carrier to convey information. The information is transmitted in a series of baseband pulses. Since the pulse durations are in the nanosecond range, the signal bandwidth is in the range of gigahertz. Due to their short time duration, UWB pulses have some unique properties. In communications, UWB pulses can be used to achieve extremely high data rate in multiuser network applications. For radar applications, short pulses can provide very fine time resolution and precision for the measurement of distance and/or positioning. Short pulses are relatively immune to multipath cancellation effects due to mobile and in-building environments. Multipath cancellation occurs when the direct path signal and an out of phase reflected wave simultaneously arrive at the receiver, thus causing a reduced amplitude response in the receiver. With very short pulses at short range, the reflected signal will arrive at the receiver after the direct signal is gone, and there is no cancellation. Therefore, I-UWB systems are well suited for high-speed, mobile wireless applications. Since the bandwidth is large, the UWB energy density (power per Hertz) can be quite low. Low energy density translates into a low probability of detection which is of particular interest for military applications such as stealth communications and radar. At the same time, a low probability of detection also represents minimal interference to other systems and minimal RF health hazards. Figure 1 shows the spectrum of impulse UWB system (Fullerton 2000 [14]).

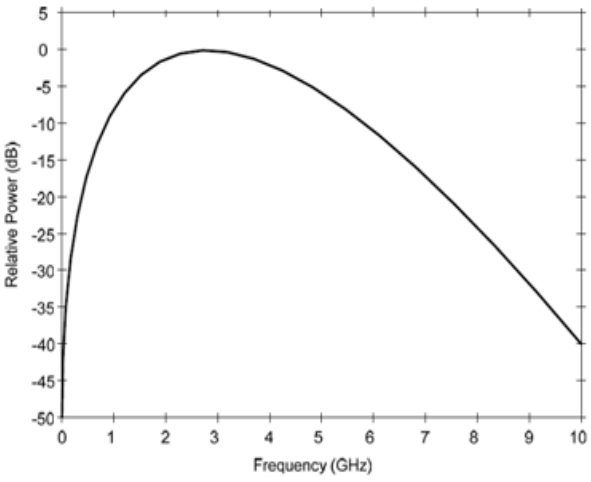

Figure 1 Spectrum of Impulse UWB system

Figure 2 shows the top level block diagram of I-UWB receiver [15]. I-UWB receiver consists of an ultra wideband LNA, a frequency domain sampler, an energy harvester block, and a decision block. LNA must exhibit a low return loss, a low noise figure, and a high gain across the entire frequency band of interest. These characteristics are mainly supported by the input matching skills of the circuit.

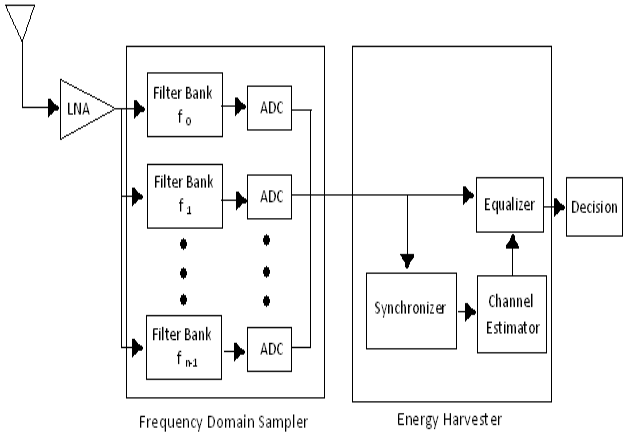

Figure 2 Top level block diagram of I-UWB receiver [16]

The ADC samples the filtered signal and is digitized for further processing. In order to reduce complexity time-interleaved ADC is employed. A time-interleaved ADC consists of parallel ADCs driven by multiple clocks with small difference in time. This reduces the required speed of the ADC by the number of parallel ADCs. For example, two ADCs in parallel reduce the required ADC speed by half. The energy harvester block collects the energy dispersed on multipath, and its function is identical to the RAKE function used for narrowband communications systems (Yang 2003 [17]). The communication channel is estimated after achieving synchronization, and the equalizer performs inter-symbol interference cancellation to recover an ideally interference-free representation of the desired symbol. A major challenge in digital I-UWB receiver design is due to the I-UWB channel, the narrow pulse shape, and narrowband interference. First, the I-UWB channel inherently suffers a relatively large delay spread as compared to the pulse width. The delay spread is normally at least tens of nanoseconds (Foerster 2003 [18]) compared to typical pulse widths of hundreds of picoseconds. During the large delay spread it is possible that hundreds of multipath reflections may be seen by the receiver. Thus, for a standard RAKE receiver, many correlates are necessary to exploit available multipath diversity. Such a large number of RAKE fingers are not practical for an analog correlate because it adds excessive complexity in hardware and control operations. Figure 3 shows the top level architecture of digital I-UWB receiver. The incoming signal is filtered and is sampled to convert analog data to digital data and is passed through DSP for further processing.

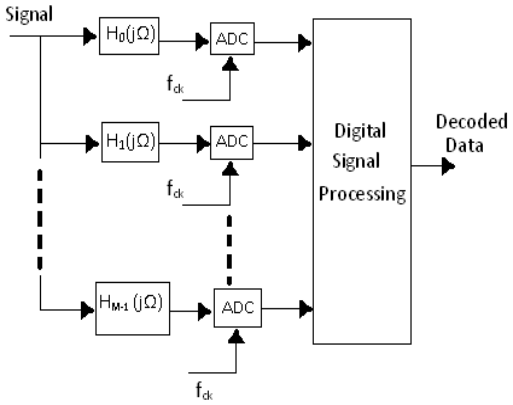

Figure 3 Top level module of Digital I-UWB receiver [18]

The ADC architecture designed in this paper can be used for high speed I-UWB receiver.

3. Design and analysis of ADC architectures

The high-speed low resolution analog-to-digital converters (ADCs) become more and more important in high-speed analog interface applications such as hard disk read channel, radar, digital receiver, IEEE 802.15.3a wireless personal area network (WPAN) [1] receiver and so on. Based on IEEE 802.15.3a WPAN UWB applications, the signals using multi-band orthogonal frequency division multiplexing (MB-OFDM) occupy a bandwidth of 528MHz for every band. It requires the conversion rate at least higher than 1.06GSample/sec with 4-bit resolution [19]. The flash ADCs published in recent years achieve from l.1GSample/sec [20]-[22] up to 40GSample/sec [23]. These high-speed ADCs usually require the relatively high supply voltage and power consumption. However, due to the rapid advances in CMOS technology, the channel length of MOS transistor is reducing. To use the MOS transistors with the low breakdown voltage and prolong the battery operating time, it is highly desirable to reduce both the supply voltage and power consumption. The pipelined ADC and sigma delta ADC have number of pipeline stages and thus can be used to operate in low power mode by switching on and off the required stage at any point of time. Thus in this section discussion on two different ADC architectures that are suitable for high speed I-UWB applications, the pipelined ADC and the Sigma Delta Modulator ADC are presented.

3.1 Low power Pipelined ADC

The pipeline ADC is the extension of the two-step structure. The conversion is divided into several stages with each stage generating a certain number of digital bits. The general block diagram is shown in Fig. 4. There are 4 stages and the i^{th} stage generates mi digits. If no redundancy is used, the sum of mi equals to 4, the resolution of ADC. The stages perform the following functions: the sample-hold circuits sample the output from the previous stage; the sub-ADC converts the analog signal into mi digital bits; the sub-DAC generates the estimated analog input signal; the subtraction and multiplication circuits generate the error signal between the input and the estimated signal and multiply it into the full scale.

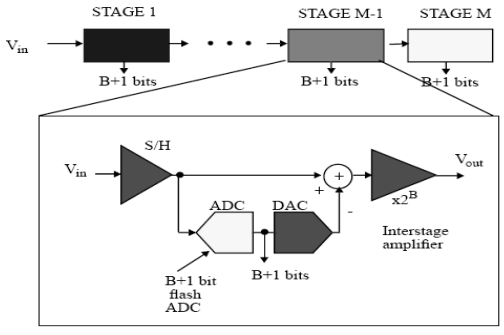

Figure 4 Pipelined ADC

This residue signal goes to the next stage. All stages operate concurrently. When a stage works on the current sample, the next stage processes the previous one. The nature of concurrence makes the throughput of the converter independent of its resolution, and the same as for a flash ADC.

3.1.1 1-Bit Single Stage of Pipelined Architecture

This stage consists of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. The analog signal is sampled and fed to the comparator which acts as the 1-bit ADC that would produce 1-bit digital output. The sample signal is DC shifted by 0.9V before being processed by the comparator, to ensure that comparator can compare the value to the threshold voltage and give the output. The digital output from the comparator is converted back to analog using the 1-bit DAC. This converted analog signal is subtracted from actual sampled signal, and the error is captured using a difference circuit. The error output of difference signal is called as residue signal. This residue signal is again scaled by a factor of 2 using an open loop amplifier. The subtractor and the multiplier are designed to operate at 50 GS/s with an input range of range of +/-300mV.

3.1.2 Sample & Hold Circuit

In this work sampled and hold circuits are implemented by the transmission gates and capacitors. The switched capacitor technique has been implemented to reduce the power. The input to the sample and hold circuit is sine wave having bandwidth of 1 GHz and the sampled signal frequency is 50 GHz. The delay between input and output is found to be 0.7ns. Figure 5 shows the circuit schematic of sample and hold circuit and its simulation results.

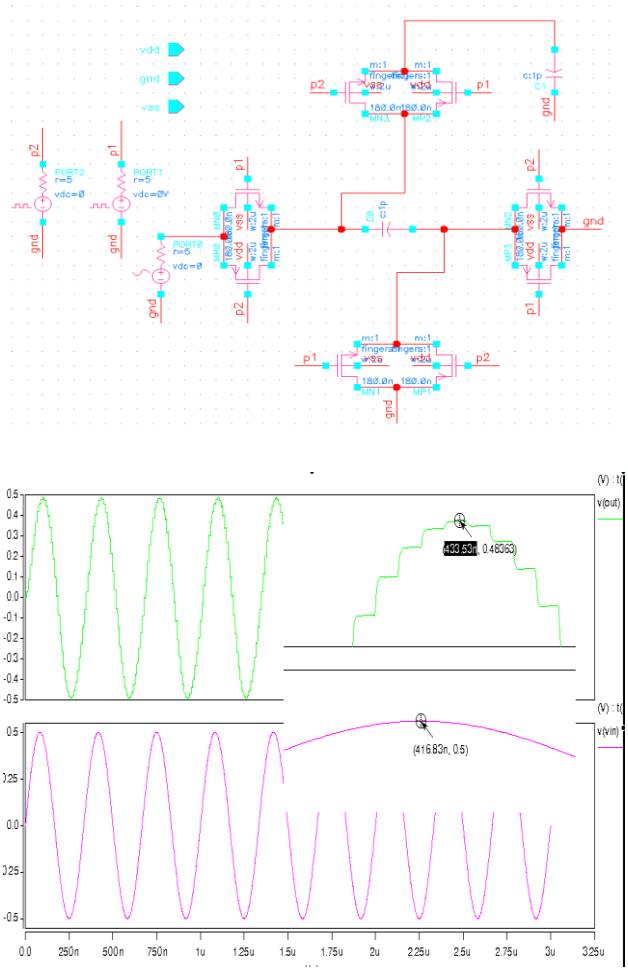

Figure 5 Schematic diagram and output results of the sample and hold circuit

3.1.3 Wideband Operational Amplifier Design

The subtraction and multiplier circuits are designed using the wideband Opamp. The specifications of the wideband amplifier are derived based on the top level simulation of 4-bit pipelined ADC. The achieved parameters from the operational amplifier simulation are given in Table 1.

Table 1 Design specifications of Wide band Operational Amplifier

DC Gain = 75dB
Unity Gain Freq = 75 GHz
Slew Rate = 14 e6 V/Sec
Phase Margin=49°
Input swing= +/-0.35mV
Output swing=+/- 1.05V

The schematic is modeled using Virtuoso and simulated using Cadence Spectre, the layout has developed using Virtuoso. The simulated transient and AC analysis waveforms are shown in the figure 6. The area occupied by the amplifier layout is 15 um* 16 um. To implement layout fingering and interdigitized technique are used.

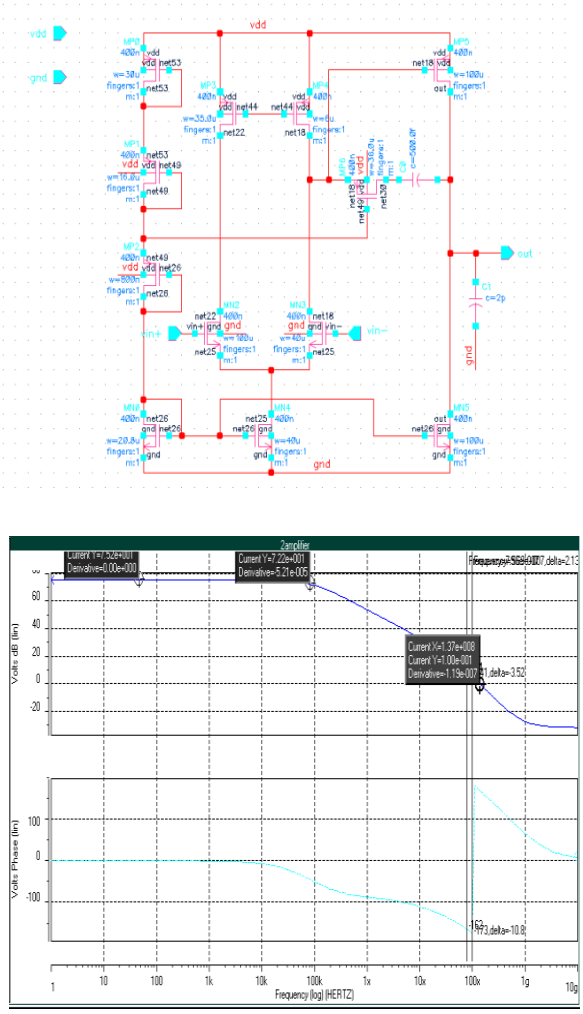

Figure 6 Wideband Opamp schematic diagram and AC analysis

3.1.4 1-Bit ADC design using CMOS Inverter

In this paper, however, a new approach, the Threshold Inverter Quantizer (TIQ), based on systematic transistor sizing of a CMOS inverter in a full-flash scheme, eliminates the resistor array implementation of conventional comparator array flash designs. Therefore no static power consumption is required for quantizing the analog input signal, making the proposed circuit very attractive for battery-powered applications. The safe analog input range can be estimated as follows: *Analog range = Vdd - (VTN + | VTP|)*, where *VTN* and *VTP* are the threshold voltages for large NMOS and PMOS devices, namely the VTHO value from the model parameter data set used during the entire design process. Figure 7 shows the schematic and the transfer characteristics of 1-bit ADC.

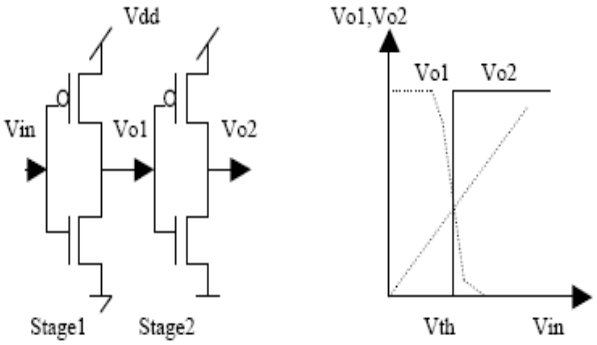

Figure 7 Schematic diagram of 1-bit ADC

4. Results and Discussion:

In this section, the simulation result of top model of 1-bit pipelined ADC is discussed. The pipelined ADC is design to operate as a 4-bit pipelined ADC with cascading of four pipelined ADCs. The results of the same are compared with reference design.

4.1 1-Bit Single stage of Pipelined Architecture

This stage is consist of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. Figure 8 shows the top level schematic of pipelined ADC architecture.

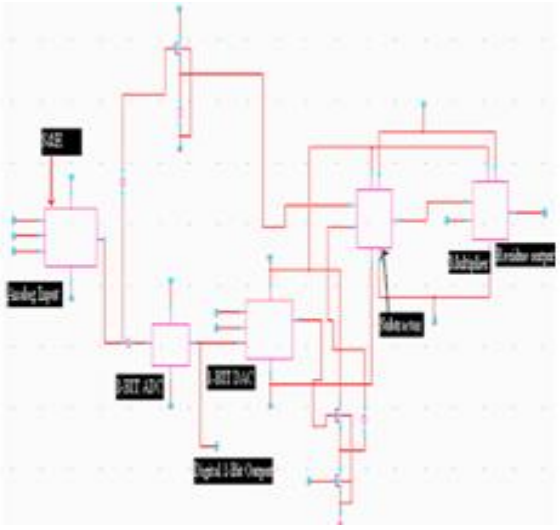

Figure 8 Schematic Diagram of 1-Bit Conversion Stage

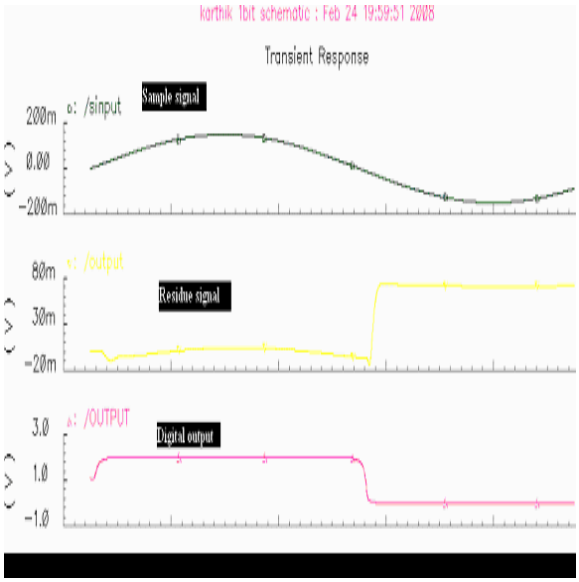

Figure 9 Output Wave Form Of The 1-Bit Conversion stage

Figure 9 presents the input sine wave having voltage rage of +/- 200mV, which is sampled and is digitized to 1-bit output. The intermediate signal is the residue output signal which is going to input of the next stage of the pipelined ADC. Since this residue signal is being affected by the loads at different stages, the signal should be amplified before given to the next stage. Figure 10 shows the top level schematic of 4-bit pipelined ADC architecture. The sub systems that were designed have been integrated together to form the top level schematic captured using Virtuoso and is simulated in Spectre. The design is carried out using 0.13 micron CMOS technology and the results obtained are discussed.

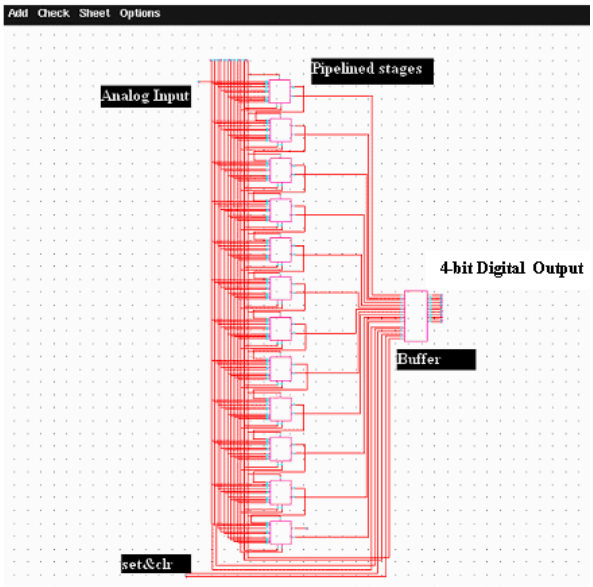

Figure 10 Top level schematic of 4-bit pipelined ADC

The power consumption at a clock frequency of 50 GHz was 36 mW from a 1.2 V supply. Below Table summarizes the measured results.

Table 2: Results Comparison

Parameters	Previous work [24,25]	Present Work
Technology	CMOS 0.35um	CMOS 0.13um
Power Supply	3V	± 1.2V
Input Signal Freq.	200KHz	up to 1 GHz
Input voltage range	---	+/-250 mV
Power dissipation	290 mW	180 mW
Area	7.9 mm^2	3.2 mm^2
Sampling freq.	75 MHz	50GHz

5. Conclusion

The goals of this work are to design a high speed ADC that can be used in I-UWB receiver. First, ADC architectures were analyzed to determine the optimal topology for the given performance specifications with minimum power consumption. Second, the exact implementation of the chosen architecture was investigated in an effort to use the minimum amount of power. Due to some limitations the SNR of the designed 4-bit ADC cannot able to be measured. After a complete analysis, the block was simulated for functionality verification. Once confirmation of correct operation was achieved, a complete layout has been designed. This project involved designing an integrated CMOS Analog-to-Digital converter for communication and video applications. The performance specifications were 4-bits, power dissipation less than 200 mW, area should be less than 0.5mm^2 and static performance parameters such as INL and DNL should be less than 1 LSB and 0.5 LSB in order to make a monotonic ADC. This pipelined ADC has been met the performance requirements. The ADC was designed in 0.18um technology at an operating voltage of ±1.2 V. Sample and hold circuit is designed by the switched-capacitor implementation. Development of low-voltage Opamp design techniques. Low-voltage design techniques for the switched-capacitor building blocks have been demonstrated enabling the implementation of larger applications such as sample-and-holds, filters, and data converters. In particular, a 1.2 V, 4-bit, 50 GS/s, 200 mW pipelined analog – to - digital converter was implemented in a 0.6m CMOS technology. The analysis presented here has also been used to identify mechanisms other than quantization noise that may limit the performance of delta-sigma modulators regardless of the over sampling ratio. It has been proven that TG switches are more immune to imperfections like charge-injection and clock feed through due to the complementary pair connected in parallel which cancels out the effect of each other. The designed 4-bit pipelined ADC has +/-300mV input voltage range. This input voltage range is limited by the input voltage swing of the Opamp and the voltage follower circuits which are commonly used, to avoid the loading effect.

6. ACKNOWLEDGMENTS

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