Study and Design of Low Power Quasi Adiabatic Cross Coupled Inverter

Samik Samanta
Neotia Institute Of Technology, Management & Science
West Bengal ,Pin-743368,India

ABSTRACT

Power dissipation has been a highly concerned issue in low power VLSI design. The classical approaches of reducing energy dissipation in conventional CMOS circuits include reducing the supply voltages, node capacitances and switching activities. Adiabatic switching technique based on energy recovery principle is one of the techniques to achieve low power VLSI design. In this paper the power dissipation of various adiabatic circuits is calculated using SPICE simulation tool. From the calculated results it has also been found that positive feedback adiabatic logic (PFAL) inverter exhibits minimum power dissipation among all the cross coupled adiabatic inverters. A new adiabatic family has been proposed by swapping NMOS and PMOS transistor of pull up network and pull down network and it has been shown that the new PFAL inverter has 33% less power dissipation than conventional PFAL inverter.

Keywords

VLSI, PFAL, SPICE , adiabatic

1. INTRODUCTION

Power dissipation has been considered as one of the very critical issues in the performance of the high speed VLSI circuits because of rapid growth of portable wireless applications and battery powered devices [2]. There are several methods to achieve low power dissipation such as reducing the supply voltage, the voltage swing, the load capacitance and switching activity [2]. Although these methods try to minimize the power dissipation, still all the energy down from the dc power supply is completely dissipated in the circuit [4]. Alternatively, adiabatic logic can reduce power dissipation to further extent by utilizing ac power supplies to recycle the energy stored in the load capacitance instead of being dissipated as heat in the circuit [4]. The word adiabatic comes from a greek word which is used to describe a thermal process without any gain or loss of heat [2,4]. In this paper we have calculated the power dissipation of various adiabatic circuits using SPICE simulation tool. From the calculated results it has also been found that positive feedback adiabatic logic (PFAL) inverter exhibits minimum power dissipation among all the cross coupled adiabatic inverters. A new adiabatic family has been proposed by. swapping NMOS and PMOS transistor of PUN and PDN and it has been shown that the new PFAL inverter has 33% less power dissipation than conventional PFAL inverter. We have also shown the mechanism to generate the trapezoidal clock needed for adiabatic circuits.

In standard CMOS circuit changes are fed from the power supply steered through MOS devices and then dumped into the load capacitor. In adiabatic logic load capacitance is charged by a constant current source instead of constant-voltage source as in the conventional COMS circuits [2,6]. A constant charging current corresponds to a linear ramp. Let us take the following circuit with constant current source, resistor and capacitor.

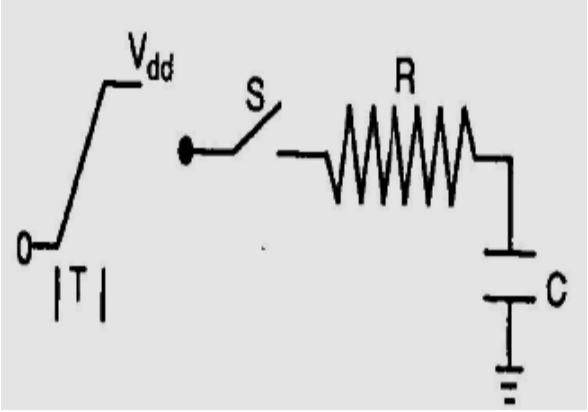

Fig 1.Principle of adiabatic circuit

R is the resistance of PMOS network. Assuming initial capacitor voltage Vc is zero. Voltage across the resistor =IR

Power in the resistor $P(r)= I^2R$

Energy during charge = $I^2RxT = I^2RT$

We know I = CV/T, T = CV/I

$E = I^2RT = (CV/T)^2 \times RT = C^2V^2/T^2 \times RT = C^2V^2R/T$

$E = E_{diss} = 1/2\ CV^2 \times (2CR/T)$

Dissipated energy is smaller than the conventional case if T is larger than 2RC, that is dissipated energy can be made arbitrary small by increasing the charging time [2,7].The dissipated energy is proportional to resistor R, as opposed to the dissipation depends on the capacitance and voltage swing. Thus reducing the ON resistance of the PMOS network will reduce energy dissipation.

To convert a conventional CMOS logic gate in to an adiabatic gate the pull up network and pull down network, must be replaced with complementary transmission gate networks[4].

The transmission gate network implementing the PUN is used to drive the true output of the adiabatic gate while the T-gate network implementing the PDN drives the complementary output node. All inputs should be available in complementary form. For adiabatic operation, the dc voltage source of the original circuit must be replaced by a pulsed power supply [2,4].

The energy CV_{PP}^2 which is consumed in the conventional CMOS circuit is unavoidable since the charge is transferred

from the supply and returned to the ground. The current drawn from the supply during a 0-1 transition is relatively large because of the large drain – source voltage. If however the supply voltage can be varied in a manner that would reduce the drain current, the energy will be significantly reduced. This can be achieved by using adiabatic circuits.

2. ADIABATIC GATES

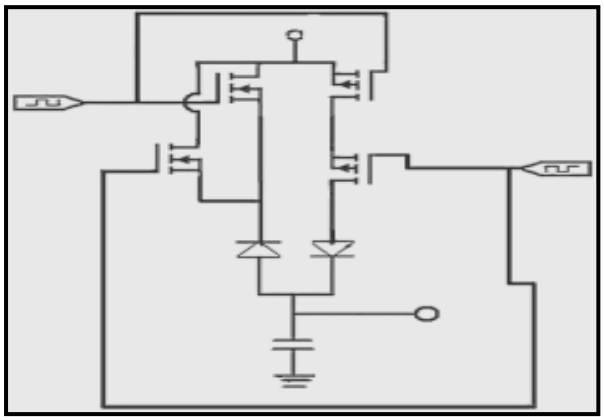

Fig1: Adiabatic NOR gate

The first branch consists of two P-channel MOSFETS and a diode in series. The second branch consists of two N-channel MOSFETS in parallel, connected in series with a diode. The two parallel branches are connected in series with the load capacitance.

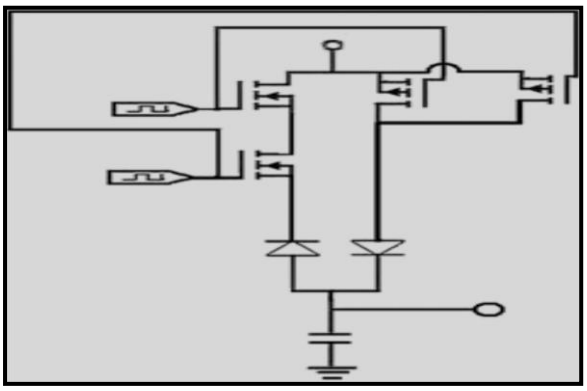

Fig2: Adiabatic NAND gate

Fig 2 shows the circuit diagram of adiabatic NAND gate. This circuit consists of two branches in parallel. The first branch consists of two P-channel MOSFETS in parallel and a diode in series. The second branch consists of two N-channel MOSFETS and a diode in series. The two parallel branches are connected in series with the load capacitance. The power dissipation of various gates and inverters are shown in the table.

Table 1. Comparison of power dissipation of various adiabatic and non adiabatic gates

Gates	Frequency		
	25MHz	50MHz	100MHz
Conventional NOR gate	34 µW	45 µW	56 µW
Conventional NAND gate	26 µW	36 µW	61 µW
Adiabatic NOR gate	15 µW	22 µW	28 µW
Adiabatic NAND gate	11 µW	14 µW	21 µW

We have simulated the conventional gates, conventional CMOS inverter and compare with the simulation results of adiabatic gates and inverters. The simulation is done using SPICE simulator and cadence simulation tools. We have used 75nm technology.

Table2: Comparison of CMOS and PFAL inverter

Inverters	Frequency		
	50MHz	100MHz	200MHz
	Power dissipation(µW)		
Conventional CMOS inverter	2.47	5.89	10.54
PFAL inverter	0.28	1.42	5.12

3. ADIABATIC INVERTER

In this paper positive feed back adiabatic inverter(PFAL) and modified positive feed back inverter(MPFAL) are shown. The heart of all the PFAL logic is composed of a latch made by the two PMOS transistors M1-M2 and two NMOS transistors M3-M4.

The conventional logic gates and conventional CMOS inverter are also simulated. The simulation is done using SPICE simulation tool.

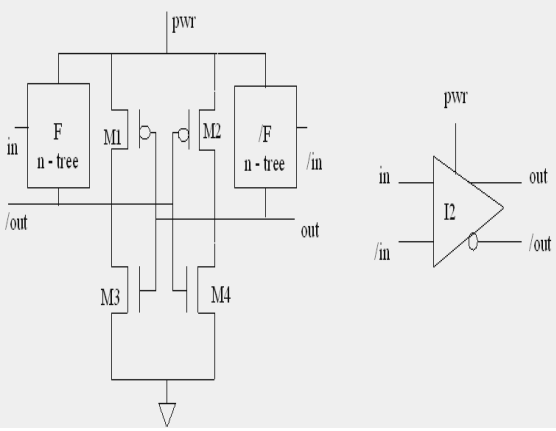

Fig3: PFAL inverter

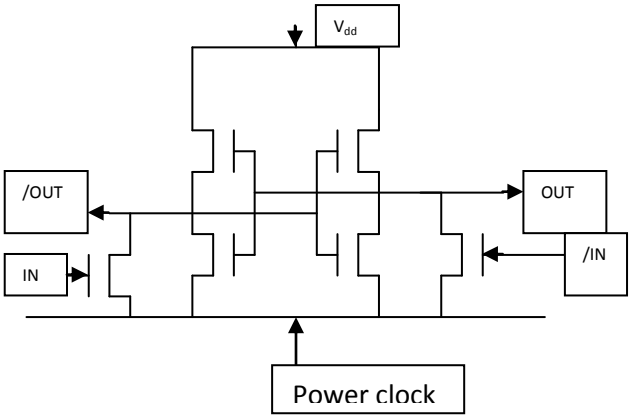

Fig4. Modified PFAL inverter

4. SIMULATION RESULTS

In modified PFAL we have interchanged the NMOS and PMOS of pull up and pull down network. We connect power supply VDD instead of power clock.

Table3: Comparison of power dissipation of PFAL and modified PFAL inverter.

Inverter	Power dissipation at 100MHz
PFAL	5.89
modified PFAL	0.482

Table 4: Comparison of power dissipation of PFAL

Circuit	Power dissipation at 100MHz
PFAL adder	2.42 µW
modified PFAL adder	0.907 µW

adder and modified PFAL adder

5. CLOCK GENERATION

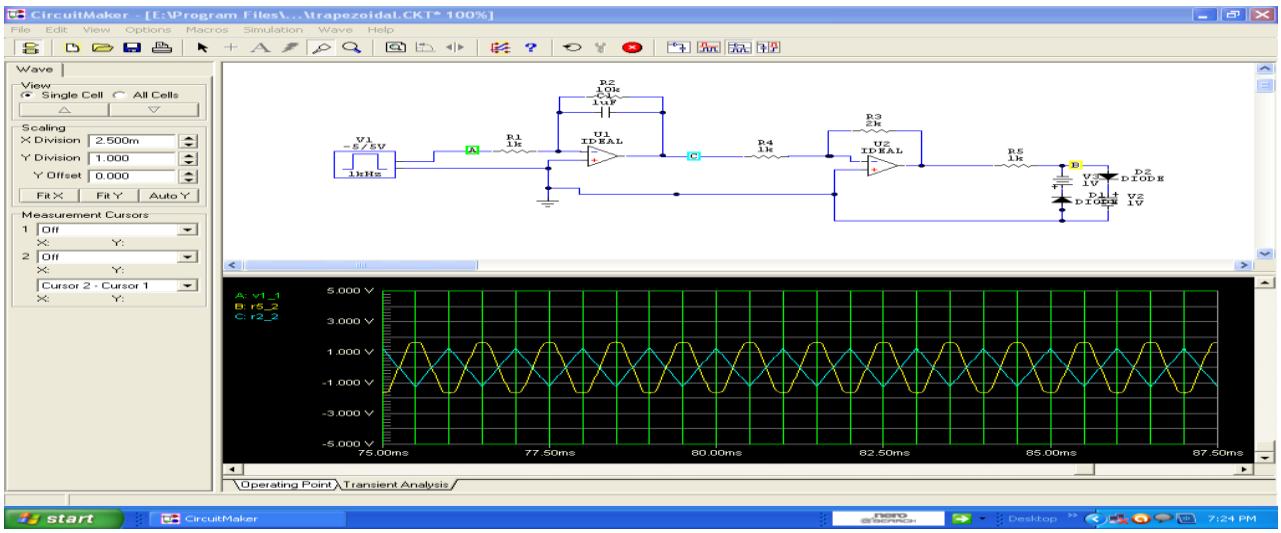

Fig 5.adiabatic clock generation

It is actually a triangular waveform generator. A square wave is integrated to get the triangular wave. The output is then amplified and clipped in both directions by a two-sided clipper circuit. We can vary the positive and negative clipping levels by varying the value of the voltage sources.

By varying the time-constant 'R_1C_1' of the integrator and by varying the amplification factor of the amplifier, we can change the rising and falling rates.

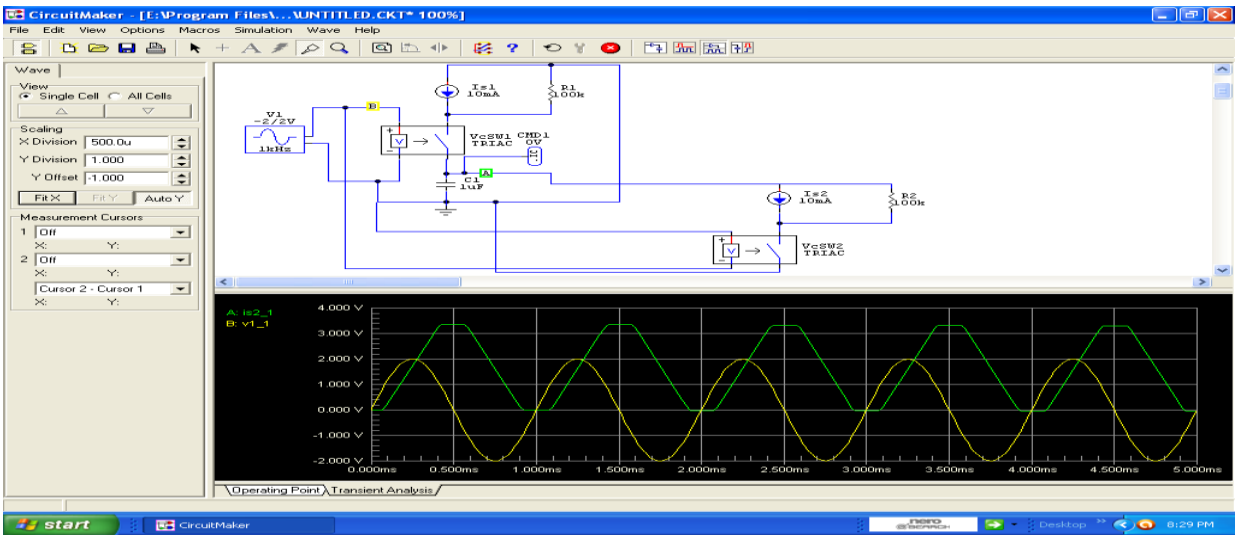

Fig 6.adiabatic clock generation

Here the main principle is to charge a capacitor by two different current sources in opposite directions, one for getting positive slope and the other for the negative slope. Let the capacitor in rest holding its voltage for some time to get a fixed level. Current source 'IS_1' charges positively and 'IS_2' charges negatively. Charging and discharging are controlled independently by two Voltage-controlled-switches. The time for which both the switches remain off = 2 x (the threshold voltage of the switches).The slopes and the levels can be varied by changing the values of constant currents (both need to have the same values).

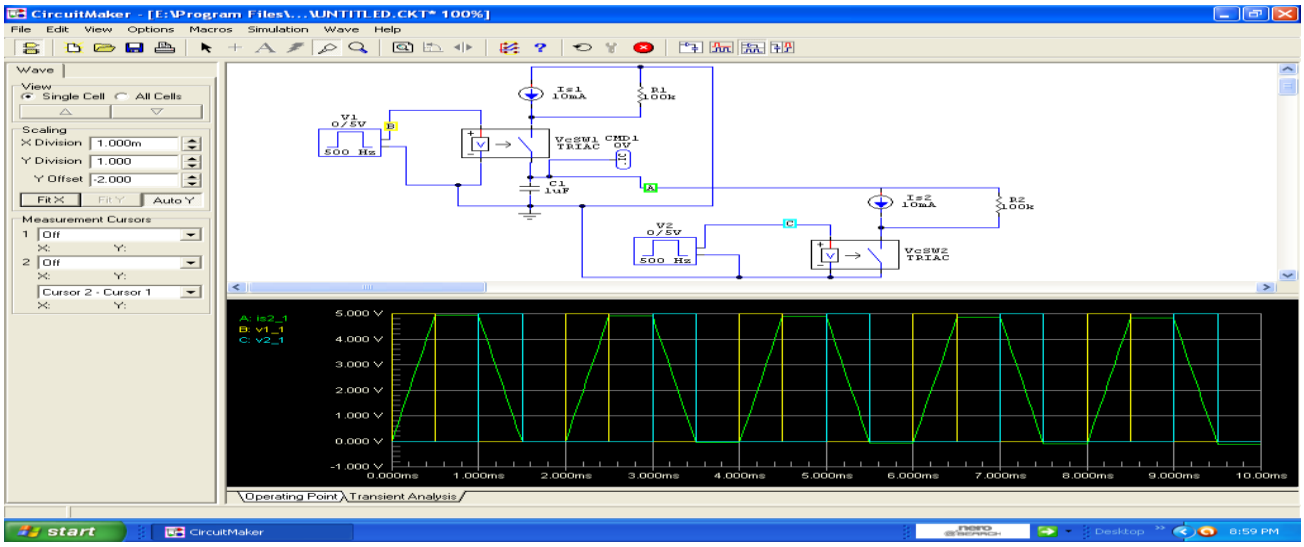

Fig 7.adiabatic clock generation

6. ACKNOWLEDGEMENT

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