# Impact of CNT's Diameter Variation on the Performance of CNFET Dual-X CCII

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## ABSTRACT
CNFET is generally considered to be one of the most appealing next generation transistors because of its high current carrying capacity and ballistic transport property. This paper investigates the performance analysis of Dual-X Current Conveyor with the CNFET technology, by varying the CNT diameter at 32nm technology node. Current Bandwidth, Input and Output Port resistances of the device along with the average power dissipated are chosen as the parameters of reference for carrying out the analysis. The impact of scaled power supply voltage, on the parameters of interest has also been explored. HSPICE simulator has been used to carry out the extensive simulations at a reduced power supply of ±0.9V.

## General Terms
Technologies beyond CMOS, Nanoelectronics,

## Keywords
Dual-X CCII, Carbon Nanotubes, Carbon Nanotube field effect transistor, Diameter of CNT, Inter-CNT Pitch

## 1. INTRODUCTION
Silicon based CMOS has been the dominant IC technology for the last 40 years and it's been one of the most primitive reasons for the mega success of the micro electronics industry. In fact, it has played an instrumental role in driving the world economics and scaling down of the feature length has been the fundamental strategy for improving the performance of the device. However, as we continue to scale down, towards the nanometer regime, its I-V characteristics tend to differ substantially .Various factors like line edge roughness, tunneling effects, randon dopant fluctuations, short channel effects etc tends to effect it's functioning and thereupon, it's become of acute essence to investigate other alternative materials that could help extend the saturating Moore's Law. In the recent past, various novel materials and devices have been investigated, amongst which Carbon Nanotubes (CNT) are generally considered as the most promising, owing to their nano scale size as well as due to it's unique electronic, mechanical and thermal properties.CNT based FET's i.e. Carbon Nanotube Field Effect Transistors (CNFET's) have been successfully fabricated and reportedly show superior performance as compared to the state of the art Silicon CMOS transistors at the same technological node. As a result, it's of imperative interest to evaluate the performance of various widely used digital and analog building blocks with the emerging CNFET technology.

As a matter of fact, various basic building blocks of digital domain like adders, multiplexers, inverters etc have already been designed using CNFET's and that's why it is of pivotal importance that the performance of analog building blocks are also explored with the same emerging technology. In this work, design and performance issues of Dual-X Current Conveyor (Dual-X CCII), a relatively new but widely used current mode device has been investigated using CNFET's. The concept of current mode devices & current mode analog signal processing has grabbed numerous eyeballs in the past decade. In current mode operation, circuit's response is described in terms of current, which is chosen as the primary parameter rather than the voltage. Current mode design offers numerous advantages over its voltage mode counterpart like high frequency response, simpler architecture, better dynamic ranges, improved linearity and being operable at lower power supply voltages. Though the performance of this building block has already been evaluated using the Silicon CMOS platform, however, designing it in deep submicron node, with the emerging CNFET technology still remains an unexplored area and that's what motivated this work

Paper is organized as follows: After a brief introduction, CNFET based design of Dual-X CCII along with its performance analysis is discussed in Section II & III respectively. Section IV explores the effects of scaled power supply voltages on the performance parameters. Finally the paper is concluded in Section IV. All the simulation measurements have been obtained after extensive simulation on HSPICE (High-performance simulation program with integrated circuit emphasis) environment using PTM parameters.

## 2. CNFET BASED DESIGN OF DUAL-X CCII
Dual-X Current Conveyor is a relatively new but versatile current mode building block, widely used in the realization of multifunctional filters, quadrature

oscillators, integrators etc to name a few. It utilizes the combined features of second generation current conveyor and inverting second generation current conveyor. The module utilizes two input X terminals i.e. Xp( non-inverting X terminal) and Xn (inverting X terminal ).Currents at both of these terminals Xp and Xn are reflected to their counterpart Z terminals i.e. Zp and Zn. The transistor level implementations of the widely used DXCCII module are shown in Figure 1.Using standard notation, terminal characteristics of Dual-X CCII shown in Figure 1 can be given as

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP} \\ I_{ZN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \end{bmatrix}$$

Though various transistor level implementations of the intended module, exists in literature, the one shown in Figure 1 has been chosen for the performance analysis using CNFET technology, because of its superior high frequency response.

Carbon Nanotube Field Effect Transistor's (CNFET) were first reported way back in 1998 and tends to overcome most of the traditional fundamental problems associated with CMOS like extreme short channel effects, leakage currents, high field effects, lithographic limits and quantum confinement effects. CNFET can be scaled down to 10 nm channel length and 4 nm channel width, thus enhancing throughput in terms of speed. Its principle of operation shares the same space with conventional CMOS technology. The semiconducting carbon nanotubes acting as the conducting channel of the device, bridges the contact between drain and source and could be turned on or off electrostatically via the gate. The number of semiconducting CNTs employed in the channel region depends on the current drive requirement. CNFET's exploits the basic inherent properties associated with 1-D structure of Carbon Nanotubes (CNT), as a result of which the device is operable in ballistic mode, thus achieving superior performance. A CNFET is generally identified in terms of three different structure parameters namely number

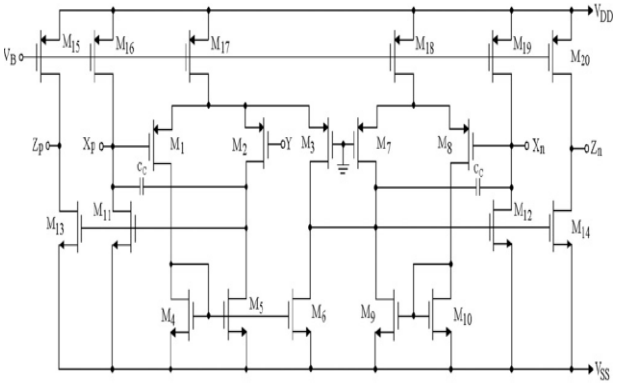


**Figure 1: Transistor level implementation of Dual-X CCII**

of CNT's in the channel (N), inter-CNT space known as Pitch(S) and the diameter of the CNT's ($D_{CNT}$). The design equations relating the diameter of the CNT ($D_{CNT}$), number of CNTs in the channel (N) , inter-CNT pitch (S) ,its threshold voltage ($V_{TH}$) and the energy gap ($\sum_g$ ) are given as follows:

$$D_{CNT} = a( n_1^2 + n_2^2 + n_1 n_2)^{1/2} / \pi$$

$$V_{th} = (aV_\pi) / \sqrt{3}\, qD_{CNT}$$

$$\sum_g = 0.84eV / D_{CNT}$$

where q = electronic charge, a = 2.49 Å is the lattice constant and $V_\pi$ =3.033 eV is the carbon π to π bond energy.

A typical layout of MOSFET like CNFET is shown in Figure 2. MOSFET-like CNFET has been chosen over Schottky barrier controlled FET (SB-CNFET) as the reference for carrying out the analysis because of its ease of fabrication and superior performance. Jie Deng's Predictive Technology model (PTM) of CNFET has been taken into consideration since it accounts for the acoustical/optical phonon scattering in the channel region, screening effect by parallel CNT's for CNFET's with multiple CNT's as well as quantum confinement on both the circumferential and the axial directions. Moreover it is also valid for a wide range of values of chiralities and diameters, thus assisting in studying the effects of diameter variation on the performance parameters of Dual-X CCII. Intrinsic device capacitance (~2-5 aF/nanotube), overlap and fringe capacitances (~0.1 fF/nanotube) along with a capacitive load of 1fF are considered for a 32 nm CNFET device. Variation of the drive current i.e. $I_{ds}$ with the variation in power supply, for different values of Oxide thickness ($T_{OX}$) is illustrated in Fig. 3. The values of various parameters used in the design are elaborated in Table 1 given below.

## 3. PERFORMANCE ANALYSIS OF CNFET DUAL-X CCII

Dual-X Current Conveyor, is a well known analog building block commonly used in the realization of filters, oscillators, integrators etc. Current Bandwidth, Input Port Resistance (Port X and Port Y), Output Port Resistance (Port Z) along with average power consumed have been chosen as the parameters for accessing the performance of the building block.

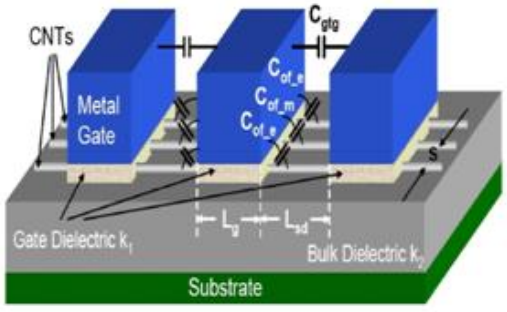


**Figure 2 : 3D view of CNFET**

TABLE I: Fixed Design Parameters of CNFET

| FIXED PARAMETERS | |
|---|---|
| Oxide Thickness ($T_{OX}$) | 3 nm |
| Power Supply | ±0.9V |
| Gate Dielectric | $HfO_2$ |
| Dielectric Constant (Kgate) | 16 |
| Threshold Voltage ($V_{TH}$) | 0.44V |
| Csub(The coupling capacitance between the channel region and the substrate ) | 30.0e-12 |
| Efi(The Fermi level of the doped S/D tube) | 0.6eV |
| Flatband voltage for n-CNFET | 0.0 eV |
| Flatband voltage for p-CNFET | 0.0 eV |
| Mean free path: Intrinsic CNT | 200nm |
| Lss (The length of doped CNT source-side extension region) | 32nm |
| Ldd(The length of doped CNT drain-side extension region) | 32nm |
| Number of CNT's in the channel | 12 |
| Inter- CNT Pitch | 14 nm |

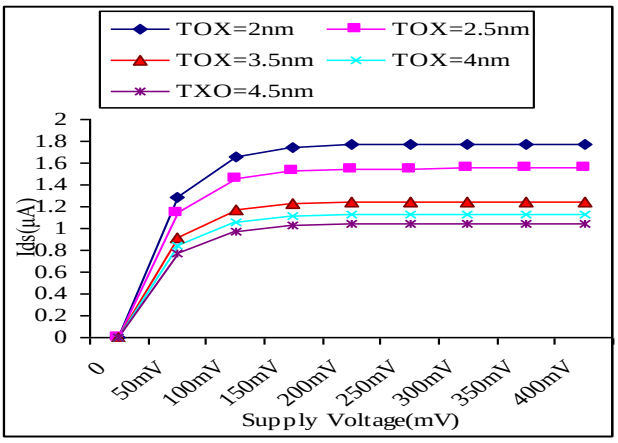


**Figure 3: Variation of $I_{ds}$ versus supply voltage**

Number of CNT's and Inter-CNT pitch for the optimized CNFET transistors used have been kept at 12 and 14nm respectively as specified in Table 1. The diameter of a SWCNT is a measure of its electronic properties and is in fact one of the most important design parameters because it not only affect the source/drain series resistance but also the threshold voltage of the device.. Here in this work, an attempt has been made to study the performance of Dual-X CCII by varying the diameter of the CNT's being used in the CNFET. For carrying out the analysis at 32nm technology node, HSPICE circuit simulator has been used and the supply voltage has been kept constant at ±0.9V.

Figure 3. indicates that the 3- dB bandwidth of the circuit increases almost parabolically with the increase in the diameter of CNT. Static current gain close to unity was obtained in addition to cut off frequencies higher than 20GHz for diameter's greater than 1.8nm. The trend could be well justified because on increasing the diameter, the gate to channel capacitance along with the fringe capacitance decrease appreciably on account of enhanced screening between the adjacent CNT channels Resistances at the input (X and Y) and output

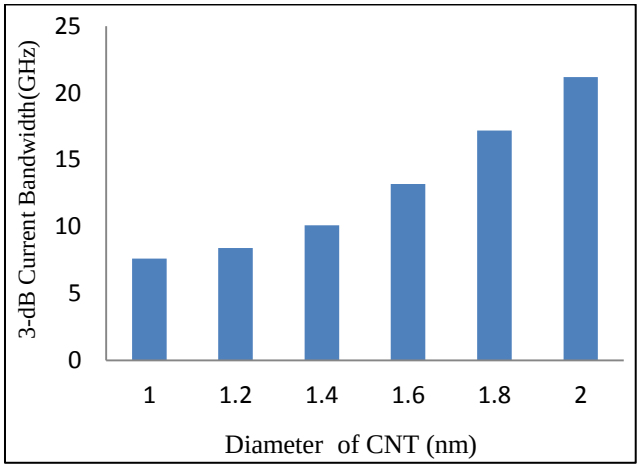


**Figure 4. Variation of 3-dB BW with the Diameter of CNT**

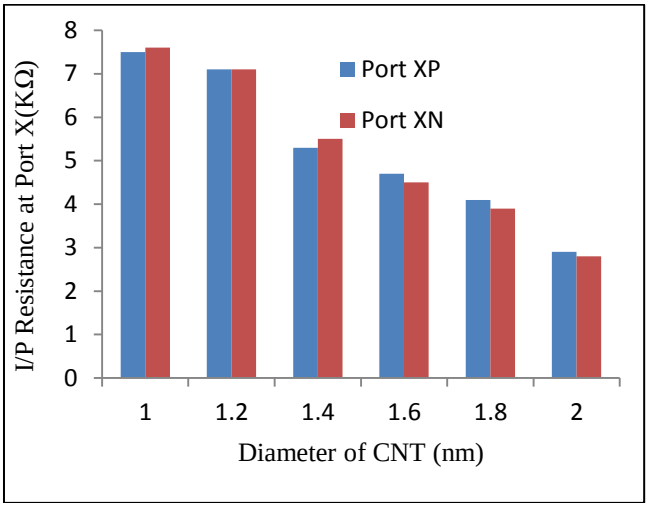


**Figure 5. Variation of Input Resistance at Port X with Diameter of CNT**

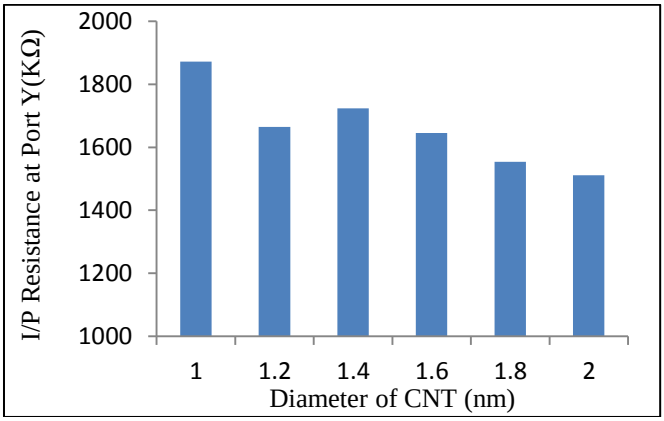


**Figure 6. Variation of Input Resistance at Port Y with Diameter of CNT**

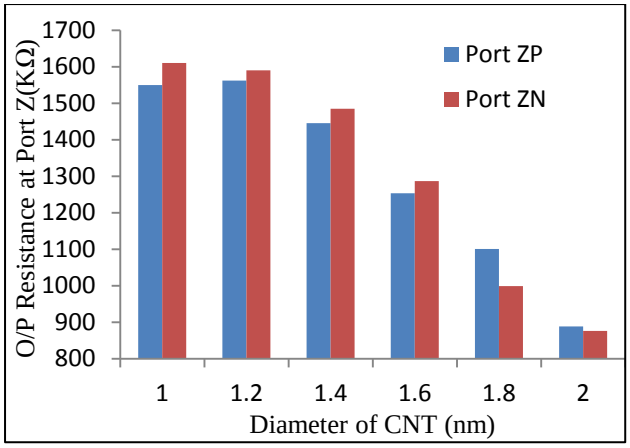


**Figure 7. Variation of Output Resistance at Port Z with diameter of CNT**

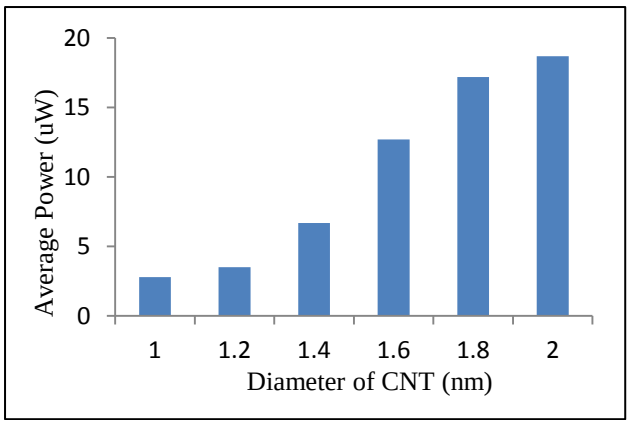


**Figure 8. Variation of Average power with the Diameter of CNT (nm)**

(Z) Port's are evaluated next. For maintaining proper signal transfer ratio's it's very important that these are kept as close as possible to their ideal value. Variation of Input Port resistances i.e. Port X and Port Y with the CNT's diameter are shown in Figures 4 and 5 respectively. On performing the small signal analysis , the output resistance of Port Z is given as :

$$R_{Zn} = ( r_{ds14} // r_{ds20} )$$

It is observed that at Output port Z, resistance of more than 1500K is obtained for smaller values of diameter and reduces down as the diameter is enhanced. Moreover the effect of power consumed has also been studied and it has been noticed that the power increases almost exponentially with the increase in the CNT diameter, for the designed analog building block. Henceforth we conclude that depending upon the application, the CNT diameter in a CNFET could be varied for a large range. For the requirements of circuit being operable in ultra wide band range of frequencies, large values of diameter are preferable but at the expense of higher power dissipation. Similarly moderate bandwidth, low power dissipation along with excellent Port Y and Z resistances are obtained ,provided smaller values of CNT diameter are taken into consideration. Therefore, opting for a suitable value of diameter is extremely difficult; rather a compromise between conflicting requirements. The optimum diameter value is hence chosen to be 1.8 nm Table II compares the results of optimized CNFET Dual-X CCII with its CMOS counterpart designed at the same node.

**TABLE II. COMPARATIVE PERFORMANCE OF CMOS & CNFET DUAL-X CCII**

| PARAMETER | CMOS DXCCII | CNFET DXCCII |
|---|---|---|
| 3-dB Current BW (GHz) | 9.45 | 17.2 |
| 3-dB Voltage BW (GHz) | 6.70 | 12.3 |
| Parasitic elememt at $X_p$ terminal (KΩ) | 5.62 | 4.12 |
| Parasitic elememt at $X_n$ terminal (KΩ) | 5.74 | 3.98 |
| Parasitic element at Y terminal | 655 | 1546 |
| Parasitic element at $Z_p$ terminal(KΩ) | 828 | 1100 |
| Parasitic element at $Z_n$ terminal(KΩ) | 845 | 1010 |

## 3. VARIATIONS IN POWER SUPPLY VOLTAGE

One of the biggest advantages associated with the CNFET is that it can be operated with much lower power supply voltages as compared to conventional Si CMOS transistors. Keeping the obtained optimized values of the number of CNTs, diameter of CNT and inter-CNT pitch, the effect of scaled power supply voltages on the performance of the designed Dual-X CCII is explored in this section. Figure 8 indicates that with the decrease in supply voltage from 0.9V to 0.3V, there is a rapid deterioration as far as the bandwidth of the circuit is concerned, because of the pronounced effect of parasitics which play a more dominant role at lower supply voltages. Furthermore, with the fast scaling of supply voltage, current drive reduces appreciably and the device operation shifts to the sub are concerned, as depicted in Fig. 10-12. Though the

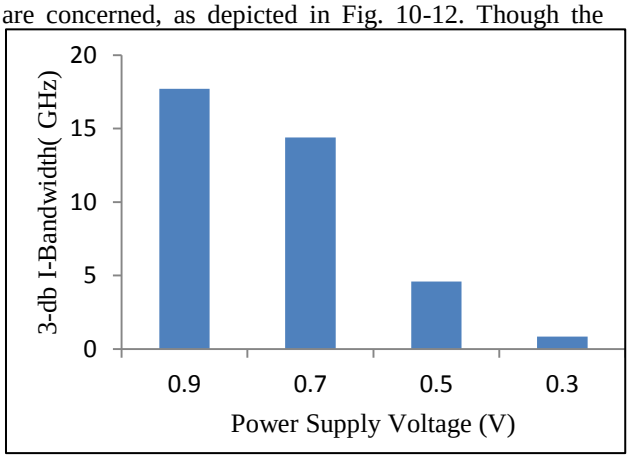


**Figure 9: Variation of the Bandwidth with the power supply**

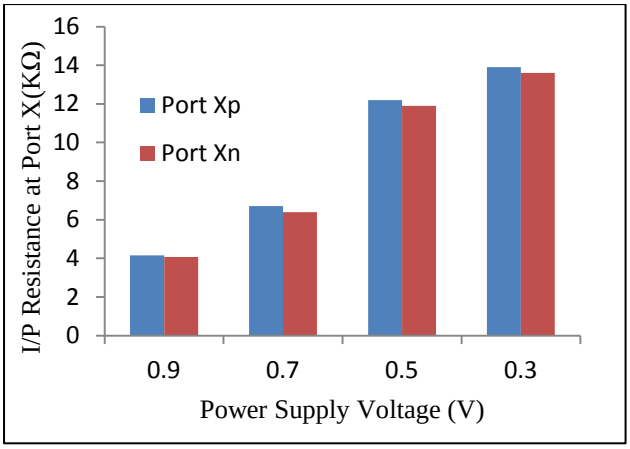


**Figure 10: Variation of Port X resistance with power supply**

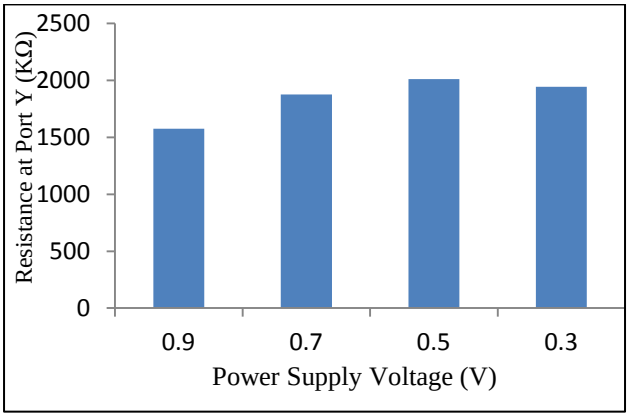


**Figure 11: Variation of Port Y resistance with power supply**

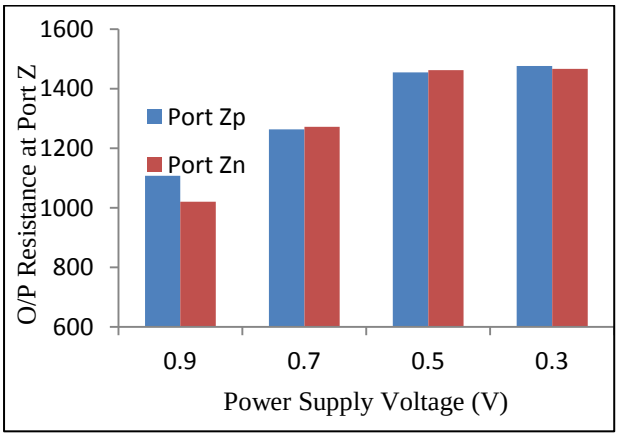


**Figure 12 : Variation of Port Z resistance with power supply**

threshold region. As a result there's a significant increase as far as the port resistances i.e. $R_X$ ,$R_Y$ and $R_Z$ lowering of supply voltage decreases the power consumption due to the proportional scaling but the robustness of the circuit deteriorates. Hence ,by studying the effect of parameter variations with supply voltage i.e.$V_{DD}$ as depicted by fig 9-13, it was found that for best performance, the supply voltage must be set around 0.9V.However a slight shift could be observed when opting for optimizing one parameter over the other such as supply voltage of ±0.7V is best

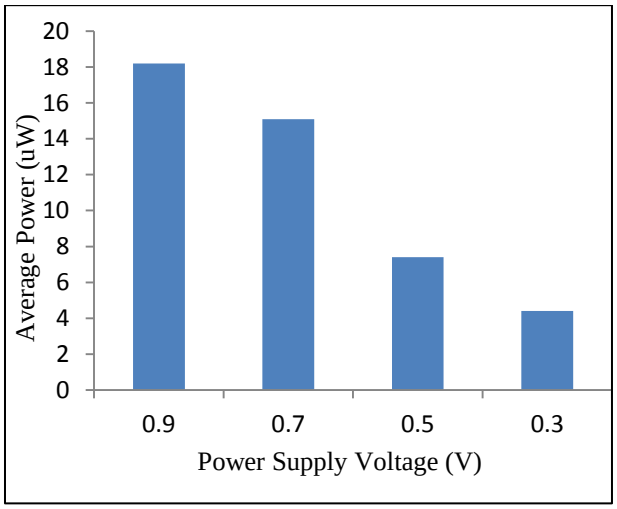


**Figure 13: Variation of Average power with power supply**

for moderate bandwidth, low power and moderate port resistance applications

## 4. CONCLUSION

This paper explores the scopes and possibilities of investigating analog circuits utilizing CNFET technology. In this paper, an attempt was made to study the performance of Dual-X CCII by varying the diameter of the CNT's being used in the CNFET. The proposed module provides excellent current bandwidths, making it suitable to be operated at microwave range of frequencies. The analysis showed that CNFET nano electronics can achieve significantly greater performances, thus making it a prospective alternative to the existing CMOS technology.

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