

Design and Optimization of n-bit Reversible Binary Comparator

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ABSTRACT

Reversible logic has attracted significance attention in recent years, leading to different approaches such as synthesis, optimization, simulation and verification. In this paper, we propose the design and optimization of n-bit reversible binary comparator. The circuit for MSB and one-bit comparator cell using NOT, PG and CNOT gates are designed. The n-bit reversible binary comparator is designed using circuit for MSB as first stage to compare MSBs and one-bit comparator cell as second stage and so on to compare lesser significant bit positions. The power consumption, delay, garbage outputs and constant inputs are computed. It is observed that the quantum cost and garbage output values are less in the proposed technique compared to the existing approaches.

KEYWORDS

Reversible Binary Comparator, Quantum Cost, Reversible Logic, Garbage Output, Constant Input.

1. INTRODUCTION

Power dissipation, silicon area and delay are major issues in VLSI design. The more number of devices are fabricated in a small silicon area to reduce size of equipment used in the real time applications. The power dissipation increases since the heat developed by more number of devices in the system. The disadvantages of real time application equipment's are (i) Increase the cost of cooling and packaging, (ii) performance of the circuit deteriorates and (iii) spoils the environment by global warming. Power consumption in CMOS design is of three types: static, short-circuit and dynamic power. Static power consumption is due to transistor leakage current, is the sum of leakage and all biased currents. Short-circuit power is related to supply voltage and threshold voltage of transistor, is determined by the process. Dynamic power is the power consumed during switching events in the core or input/output of the design. Switching activity is function of voltage, frequency and capacitance.

The dynamic power is the charging and discharging of parasitic gate capacitance and metal layers, which is dominant among the overall power consumption of the chip. Hence most of the designer's effort goes on reducing dynamic power, which includes the reduction of capacitance, operating voltage, frequency and switching. With advancement in technologies, ASIC and FPGAs have increased in logic capacity and performance. Power consumption is receiving greater attention at the component selection phase of ASIC and FPGA-based designs. Due to exponential growth, physical boundaries will be reached in the near future hence traditional technologies like CMOS will reach their limits. To overcome this, an alternative computation technologies are required that encourages research in reversible logic.

Reversible computing has become a strongly studied research area. As reversible circuits are subjected to certain restrictions like fan-out and feedback, synthesis aspects are of interesting. According to Landauer [1], every bit of information lost consumes $KT\ln 2$ joules of energy, where K is Boltzmann's constant and T is the absolute temperature at which the operation performed. Charles Bennett [2] showed that if the computation is carried out in reversible logic, the energy loss can be reduced or even eliminated and also proved that circuits built from reversible gates have zero power dissipation.

The recycling of real life entities like bottles, cans, paper etc., were impossible decades back, but they are quite prominent today. The same applies to the computing world also. Today's computers consume huge amount of energy, as millions of bits are manipulated billion times in every second. The irreversible logic devices are used in computers been recognized as energy inefficient for several decades. The reversible computing, which does not compute bits that are no longer needed, that allows their energy to be recovered and recycled for use in later operations. The demand for energy efficient becomes more prominent hence reversible computing will become popular. Before the computer industry reaches the fundamental brick wall of performance and energy constraints of computing devices, reversible computing needs to be fully developed.

A circuit is reversible if it has one-to-one mapping between the input and output values. Quantum technology is inherently reversible and is one of the most computing technologies for future computing systems [3]. In Quantum Computation, problem solving is much more efficient compared to classical computing. A reversible logic should be designed to use minimum number of gates, constant inputs, garbage outputs and Quantum cost [4]. The comparison of binary numbers is one of the important operations in many computing systems. It finds wide applications in General Purpose Processors, Communications Systems, Medical Electronics, Web Designing, Data Mining, Biometrics etc. The binary comparators are designed using traditional logic such as NMOS and CMOS, which results in little more power consumption. The reversible binary comparators are designed using reversible gates to optimize power consumption.

Contribution: In this work, design and optimization of reversible binary comparator is proposed. The design is based on the reversible gates such as NOT, Feynman (CNOT) and Peres (PG). The PG gate is very useful in designing binary comparator for optimizing quantum cost, delay, constant inputs and garbage outputs. The proposed reversible binary comparator design for 8-bit, 16-bit, 32-bit, 64-bit and n-bit numbers is illustrated.

Organization: The paper is organized into the following sections. Section 2 is an overview of basic reversible gates. The literature survey is described in section 3. Section 4 is the proposed comparator design, result analysis of the proposed design is presented in section 5 and conclusions are contained in section 6.

2. BASIC REVERSIBLE GATES

The simplest reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 reversible gates such as Fredkin (F), Toffoli (TG), Peres (PG) and TR gate. The quantum cost of 1*1 Reversible gates is zero, and quantum cost of 2*2 reversible gates is one. Any reversible gate is realized by using 1*1 NOT gates and 2*2 reversible gates, such as V, V⁺ (V is square root of NOT gate and V⁺ is its hermitian) and Feynman gate which is also known as CNOT gate. The V and V⁺ quantum gates have the property given in the Equations 1, 2 and 3.

$$V * V = \text{NOT} \dots\dots\dots (1)$$

$$V * V^+ = V^+ * V = I \dots\dots\dots (2)$$

$$V^+ * V^+ = \text{NOT} \dots\dots\dots (3)$$

The quantum cost of a reversible gate is calculated by counting the number of V, V⁺ and CNOT gates.

2.1 NOT Gate

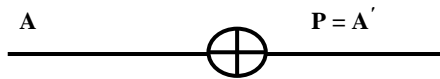


Figure 1. NOT Gate.

The reversible 1*1 gate is NOT gate with zero quantum cost is as shown in the Figure 1.

2.2 Feynman / CNOT Gate

The reversible 2*2 gate with quantum cost of one having mapping input (A, B) to output (P = A, Q = A ⊕ B) is as shown in the Figure 2.

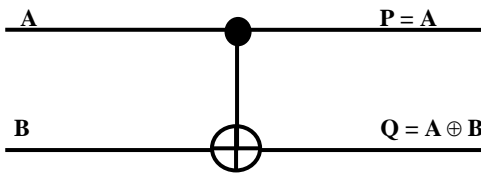


Figure 2. Feynman / CNOT Gate.

2.3 Peres Gate

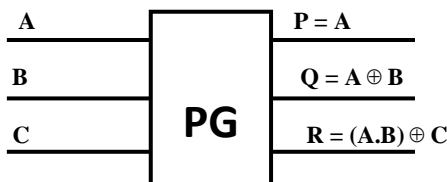


Figure 3. Peres Gate

The three inputs and three outputs i.e., 3*3 reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = A ⊕ B, R = (A.B) ⊕ C). Since it requires two V⁺, one V and one CNOT gate, it has the quantum cost of four. The Peres gate

[7] and its quantum implementation are as shown in the Figure 3 and 4 respectively.

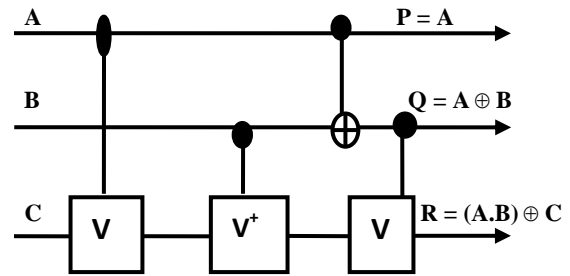


Figure 4. Quantum implementation of Peres Gate

3. LITERATURE SURVEY

Zeljko Zilic et al., [8] presented a methodology for realizing the networks of reversible gates results in synthesizing complex reversible circuits by mapping the original irreversible circuit specification into a library of reversible cells. Mozammel Khan [9] explained the design of quantum ternary equality, less-than and greater-than comparator using one-qutrit and two-qutrit Muthukrishnan-stroud gates, which are multi-valued quantum gates. Zichu Qi et al., [10] presented a floating-point Fused multiply-add unit with low-cost and low-power techniques. To reduce area for supporting two single precision operations in parallel, the multiplier, shifter and adder are reused. Leland Chang et al., [11] explored about the limitations of power dissipation due to advancement in silicon microelectronics and the importance of trade-off between power and performance and also shown that area is the constraint in improving power efficiency.

Fuming Sun et al., [12] analyzed the sources of power consumption, design consideration, technologies and analysis tools in FPGA. A general view of power consumption, various forms of power consumption and design characteristics to minimize power consumption are discussed. Michael Miller and Zahra Sasanian [13] explained cost saving with the goal of reducing the number of quantum gates required, based on novel line labeling and gate moving procedures. Maii Emam and Layle Elsayed [14] presented two novel designs of adder/subtractor using reversible gates. First design uses two's complement adder/subtractor suitable for signed/unsigned numbers. Other one is a novel reversible gate that can work singly as reversible full adder/subtractor unit. The design is extended for reversible four-bit ripple adder/subtractor. Madhusmita Mahapatro et al., [15] developed a reversible counterpart of all the irreversible basic logic gates and full custom layout of all these gates with reversibility using 0.25 μm technology. The reversible full adder, half adder, four-bit binary parallel adder and 4x4 multiplier circuits are designed using reversible logic. Lihui Ni et al., [16] proposed a general approach to construct the reversible full-adder with two reversible gates and two garbage outputs. The reversible full adder can be used to construct the large-scale reversible systems and can reduce the cost of the circuits.

Mathias Soeken et al., [17] introduced Revkit, a toolkit that helps to make recent developments in reversible circuit design accessible to others. A modular and extendable framework is provided which enables the addition of new methods and tools. Stefan Frehse et al., [18] presented an automatic debugging approach for reversible logic, based on simulation with pattern matching. In many cases this leads to significant

reductions of the number of errors. Applying this leads to run time improvements up to five orders of magnitude. Rangaraju et al., [19] proposed three designs of reversible parallel binary adder/subtractor which is used for low-power applications and is efficient in terms of quantum cost, number of gates used, garbage inputs/outputs. Praveen et al., [20] presented a 4x4 reversible adder/subtractor circuit which performs half/full adder and subtractor function with minimum garbage count and critical path.

4. PROPOSED COMPARATOR DESIGN

4.1 Circuit for MSB

The circuit for MSB is to binary comparator using reversible logic is shown in Figure 5. This circuit consists of three inputs A_n , B_n and logical low i.e., 0 and the outputs A Equal to B (AEB), A Greater than B (AGB) and A Less than B (ALB). The reversible circuit for MSB is designed using one PG, two CNOT and one NOT gates. The circuit for MSB alone can function as one-bit comparator and has one garbage output, two constant inputs and the quantum cost of six as PG gate costs four and each CNOT gate costs one. This circuit for MSB is connected at the first stage of the serial design of n-bit reversible binary comparator.

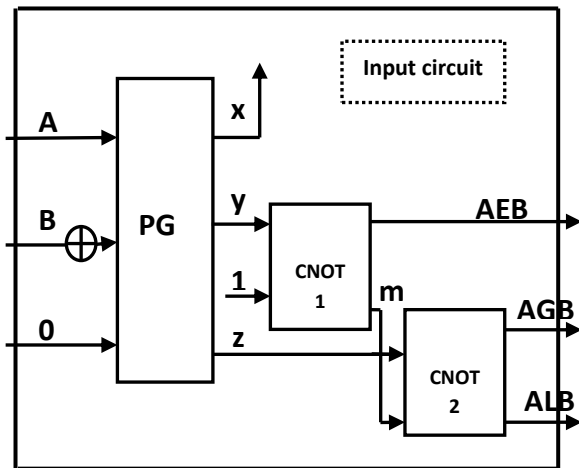


Figure 5. The circuit for MSB of the reversible binary comparator

The input B_n is connected to the NOT gate to get B_n' at the output of the NOT gate and the inputs A_n , B_n' and logical Low are connected to PG gate. The output x is garbage output represented as $g1$ and output y of the PG gate is $(A \oplus B)$ is connected to input of CNOT1 gate, another input to CNOT1 gate is Logical High i.e., 1. The output z of the PG gate is AB' and output m of CNOT1 is $(A \oplus B)$ are connected to inputs of the CNOT2 gate. The final outputs of the circuit for MSB are given in Equation 4, 5 and 6.

$$AEB = (A \oplus B)' \dots\dots\dots (4)$$

$$AGB = AB' \dots\dots\dots (5)$$

$$ALB = A'B \dots\dots\dots (6)$$

4.2 One-bit Reversible Binary Comparator

Block A is shown in Figure 6 is used in the one-bit comparator cell, which consists of two NOT, one PG and one CNOT gate. The output i of PG is garbage output and output j of the PG gate is $(A \oplus B)'$ is connected to NOT gate and then to input of the CNOT gate. The output k of the PG gate is

connected to input of CNOT gate which results in C_1 i.e., AB' and C_2 i.e., $A'B$.

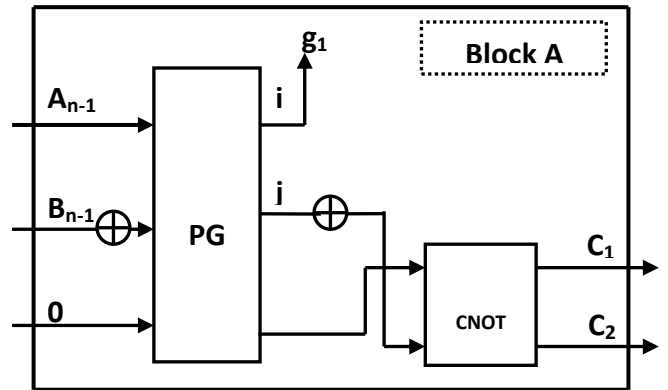


Figure 6. Block diagram of block A

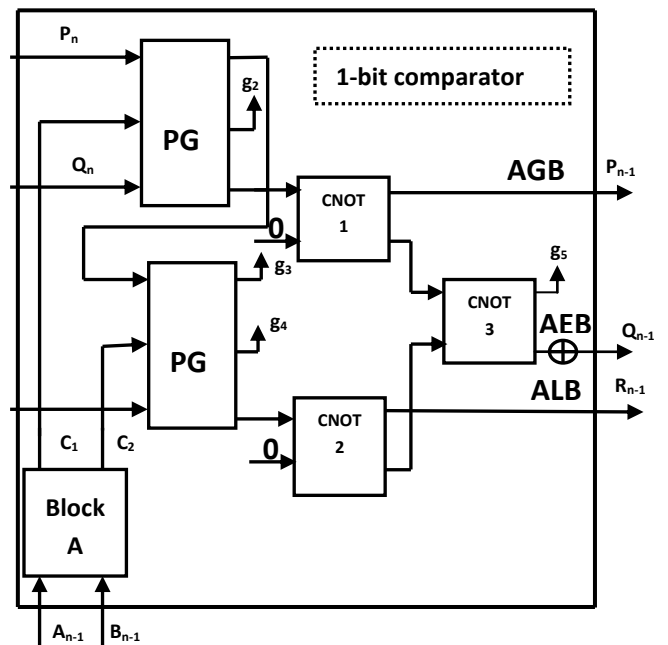


Figure 7. One-bit reversible binary comparator

Table 1. One-bit reversible binary comparator

Inputs		Outputs		
A	B	ALB	AEB	AGB
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

One-bit reversible binary comparator consists of three PG and four CNOT gates. It has five inputs viz., P_n (AEB), Q_n (AGB), R_n (ALB), A_{n-1} and B_{n-1} and three outputs Q_{n-1} i.e., AGB, P_{n-1} i.e., AEB and R_{n-1} i.e., ALB as shown in the Figure 7. In this PG gates are used to generate the product functions like AB' and $A'B$ and connecting these to three CNOT gates and one

NOT gate to get the final outputs of one-bit comparator. This circuit designed to be fit at lesser significant bit positions in n-bit binary comparator. This design has a quantum cost of sixteen as three PG gates costs twelve and four CNOT gates costs four, constant inputs of three denoted as logical *Low* and five garbage outputs represented as *g1* to *g5*. The corresponding input and output combinations are shown in the Table 1.

4.3 Two-bit Reversible Binary Comparator

Two-bit reversible binary comparator is shown in Figure 8. It has two stages: circuit for MSB stage and one-bit comparator cell stage. The two Most Significant Bits (MSBs) A_2, B_2 are applied to circuit for MSB, gives one-bit comparison outputs P_2, Q_2 and R_2 . These outputs are connected to one-bit comparator cell which compares two Least Significant Bits (LSBs) A_1, B_1 with P_2, Q_2 and R_2 . The outputs AEB, AGB and ALB, are final outputs of the two-bit comparator. This design has the quantum cost of twenty two as circuit for MSB costs six and one-bit comparator cell costs sixteen. The constant inputs i.e., inputs connected to Logical *low* or Logical *high* are five numbers and six garbage outputs i.e., unused outputs. Outputs for different input combinations are shown in the Table 2.

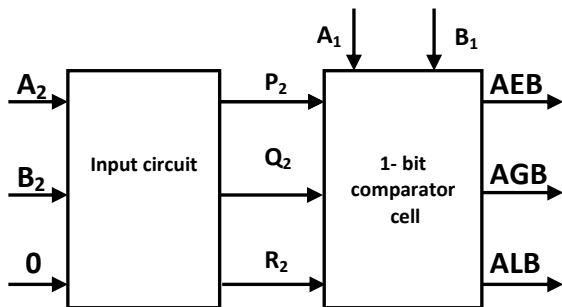


Figure 8. Two-bit reversible binary comparator

Table 2. Two-bit reversible binary comparator

Inputs				Outputs		
A		B		ALB	AEB	AGB
A2	A1	B2	B1			
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

In the table A_2, A_1 and B_2, B_1 are two-bit numbers A and B and depending on the magnitude of these bits any one of the outputs i.e., ALB, AEB and AGB will be Logical *high*. For example consider the tenth row in the table i.e., $A_2=1, A_1=0$ and $B_2=0, B_1=1$, here since A_2 is the MSB bit of A which is Logical *high* and B_2 is the MSB bit of B which is Logical *low* irrespective of other input bits the result will be AGB.

4.4 Three-bit Reversible Binary Comparator

Three stages of three-bit reversible binary comparator is shown in Figure 9. First stage is circuit for MSB stage functions as one-bit comparator compares the MSB bits A_3, B_3 of the two numbers. Second stage is one-bit comparator cell compares the result of the first stage i.e., P_3, Q_3, R_3 and the input bits A_2 and B_2 . Third stage is also one-bit comparator cell compares the outputs P_2, Q_2 and R_2 of the second stage and the LSB bits A_1, B_1 of the two numbers results in the final outputs AEB, AGB and ALB of the three-bit comparator.

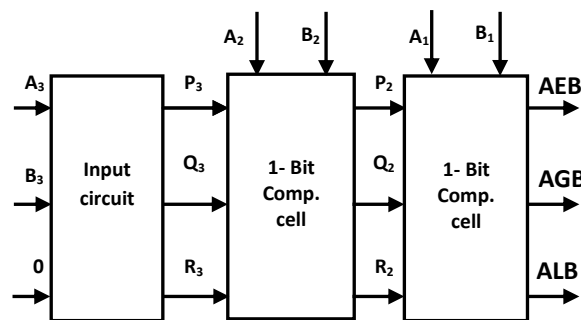


Figure 9. Three-bit reversible binary comparator

The Quantum Cost (QC) of three-bit reversible binary comparator is given in an Equation:

$$QC = QC \text{ of circuit for MSB} + (2 * QC \text{ of one-bit Comparator cell}) \dots\dots\dots (7)$$

$$QC = 6 + 2 \times 16 = 38.$$

The number of Constant Inputs (CIs) of three-bit reversible binary comparator is given in an Equation:

$$CIs = CIs \text{ of circuit for MSB} + (2 * CIs \text{ of one-bit Comparator cell}) \dots\dots\dots (8)$$

$$CIs = 2 + 2 \times 3 = 8.$$

The Garbage Outputs (GOs) of three-bit reversible binary comparator is given in an Equation:

$$GOs = GOs \text{ of circuit for MSB} + (2 * GOs \text{ of one-bit comparator cell}) \dots\dots\dots (9)$$

$$GOs = 1 + 2 \times 5 = 11.$$

4.5 Four-bit Reversible Binary Comparator

Four stages of four-bit reversible binary comparator are shown in Figure 10. First stage is circuit for MSB stage compares the MSB bits of the two numbers. Second stage is one-bit comparator cell compares the result of the first stage and the input bits A_2, B_2 . Third stage is also one-bit comparator cell compares the output of the second stage and the input bits A_1, B_1 . Fourth stage compares the result of third stage and the LSB bits A_0, B_0 of the two numbers resulting the final output of the four-bit numbers A and B.

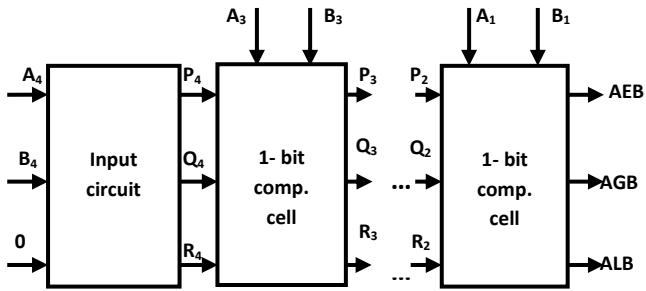


Figure 10. Four-bit reversible binary comparator

The QC of four-bit reversible binary comparator is given in an Equation:

$$QC = QC \text{ of circuit for MSB} + (3 * QC \text{ of one-bit Comparator cell}) \dots\dots\dots (10)$$

$$QC = 6 + 3 \times 3 = 15.$$

The number of CIs of four-bit reversible binary comparator is given in an Equation:

$$CIs = CIs \text{ of circuit for MSB} + (3 * CIs \text{ of one-bit Comparator cell}) \dots\dots\dots (11)$$

$$CIs = 2 + 3 \times 3 = 11.$$

The GOs of four-bit reversible binary comparator is given in an Equation:

$$GOs = GOs \text{ of circuit for MSB} + (3 * GOs \text{ of one-bit comparator cell}) \dots\dots\dots (12)$$

$$GOs = 1 + 3 \times 5 = 16.$$

4.6 Eight-bit Reversible Binary Comparator

Eight-bit reversible binary comparator is shown in Figure 11. First stage is circuit for MSB stage compares the MSB bits of the two numbers A_8, B_8 . Second stage is one-bit comparator cell compares the result of the first stage and the input bits A_7, B_7 . Third stage is also one-bit comparator cell compares the output of the second stage and the input bits A_6, B_6 . Fourth stage compares the result of third stage and the input bits A_5, B_5 of the two numbers and so on. The final stage compares the output of the seventh stage and the LSB bits A_1, B_1 resulting the final output of the eight-bit numbers A and B.

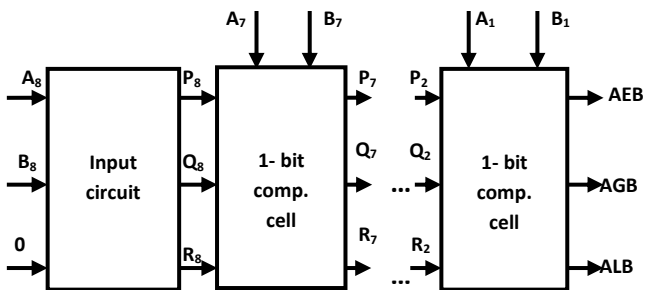


Figure 11. Eight-bit reversible binary comparator

The QC of eight-bit reversible binary comparator is given in an Equation:

$$QC = QC \text{ of circuit for MSB} + (7 * QC \text{ of one-bit Comparator cell}) \dots\dots\dots (13)$$

$$QC = 6 + 7 \times 3 = 27.$$

The number of CIs of eight-bit reversible binary comparator is given in an Equation:

$$CIs = CIs \text{ of circuit for MSB} + (7 * CIs \text{ of one-bit Comparator cell}) \dots\dots\dots (14)$$

$$CIs = 2 + 7 \times 3 = 23.$$

The GOs of eight-bit reversible binary comparator is given in an Equation:

$$GOs = GOs \text{ of circuit for MSB} + (7 * GOs \text{ of one-bit comparator cell}) \dots\dots\dots (15)$$

$$GOs = 1 + 7 \times 5 = 36.$$

4.7 Sixteen-bit Reversible Binary Comparator

Sixteen stages of sixteen-bit reversible binary comparator are shown in Figure 12. First stage compares the MSB bits of the two numbers A_{16}, B_{16} . Second stage is one-bit comparator cell compares the result of the first stage and the input bits A_{15}, B_{15} . Third stage is also one-bit comparator cell compares the output of the second stage and the input bits A_{14}, B_{14} . Fourth stage compares the result of third stage and the input bits A_{13}, B_{13} of the two numbers and so on. The final stage compares the output of the fifteenth stage and the LSB bits A_1, B_1 resulting the final output of the eight-bit numbers A and B.

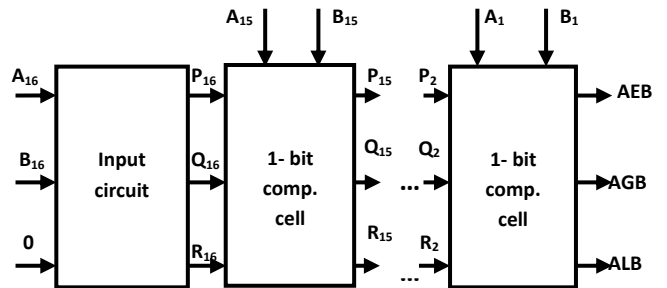


Figure 12. Sixteen-bit reversible binary comparator

The QC of sixteen-bit reversible binary comparator is given in an Equation:

$$QC = QC \text{ of circuit for MSB} + (15 * QC \text{ of one-bit Comparator cell}) \dots\dots\dots (16)$$

$$QC = 6 + 15 \times 3 = 54.$$

The number of CIs of sixteen-bit reversible binary comparator is given in an Equation:

$$CIs = CIs \text{ of circuit for MSB} + (15 * CIs \text{ of one-bit Comparator cell}) \dots\dots\dots (17)$$

$$CIs = 2 + 15 \times 3 = 47.$$

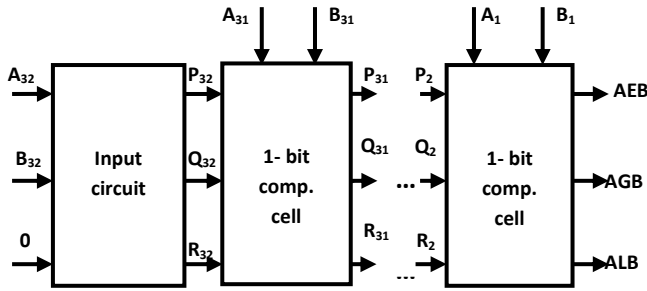
The GOs of sixteen-bit reversible binary comparator is given in an Equation:

$$GOs = GOs \text{ of circuit for MSB} + (15 * GOs \text{ of one-bit comparator cell}) \dots\dots\dots (18)$$

$$GOs = 1 + 15 \times 5 = 76.$$

4.8 Thirty-Two-bit Reversible Binary Comparator

Thirty-two-bit reversible binary comparator are shown in Figure 13. First stage is circuit for MSB stage works as one-bit comparator compares the MSB bits of the two numbers A_{32}, B_{32} . Second stage is one-bit comparator cell compares the result of the first stage and the input bits A_{31}, B_{31} . Third stage is also one-bit comparator cell compares the output of the second stage and the input bits A_{30}, B_{30} . Fourth stage compares the result of third stage and the input bits A_{29}, B_{29} of the two numbers and so on. The final stage compares the output of the thirty-first stage and the LSB bits A_1, B_1 resulting the final output of the thirty-two-bit numbers A and B.



Thirty-two-bit reversible binary comparator

The QC of Thirty-two-bit reversible binary comparator is given in an Equation:

$$QC = QC \text{ of circuit for MSB} + (31 * QC \text{ of one-bit Comparator cell}) \dots\dots\dots (19)$$

$$QC = 6 + 31 \times 16 = 502.$$

The number of CIs of Thirty-two-bit reversible binary comparator is given in an Equation:

$$CIs = CIs \text{ of circuit for MSB} + (31 * CIs \text{ of one-bit Comparator cell}) \dots\dots\dots (20)$$

$$CIs = 2 + 31 \times 3 = 95.$$

The GOs of Thirty-two-bit reversible binary comparator is given in an Equation:

$$GOs = GOs \text{ of circuit for MSB} + (31 * GOs \text{ of one-bit comparator cell}) \dots\dots\dots (21)$$

$$GOs = 1 + 31 \times 5 = 156.$$

4.9 Sixty-Four-bit Reversible Binary Comparator

Sixty-four-bit reversible binary comparator is shown in Figure 14. First stage is circuit for MSB stage works as one-bit comparator compares the MSB bits of the two numbers A_{64} , B_{64} . Second stage is one-bit comparator cell compares the result of the first stage and the input bits A_{63} , B_{63} . Third stage is also one-bit comparator cell compares the output of the second stage and the input bits A_{62} , B_{62} . Fourth stage compares the result of third stage and the input bits A_{61} , B_{61} of the two numbers and so on. The final stage compares the output of the sixty-third stage and the LSB bits A_1 , B_1 resulting the final output of the sixty-four-bit numbers A and B.

The QC of Sixty-four-bit reversible binary comparator is given in an Equation:

$$QC = QC \text{ of circuit for MSB} + (63 * QC \text{ of one-bit Comparator cell}) \dots\dots\dots (22)$$

$$QC = 6 + 63 \times 16 = 1014.$$

The number of CIs of Sixty-four-bit reversible binary comparator is given in an Equation:

$$CIs = CIs \text{ of circuit for MSB} + (63 * CIs \text{ of one-bit Comparator cell}) \dots\dots\dots (23)$$

$$CIs = 2 + 63 \times 3 = 191.$$

The GOs of Sixty-four-bit reversible binary comparator is given in an Equation:

$$GOs = GOs \text{ of circuit for MSB} + (63 * GOs \text{ of one-bit comparator cell}) \dots\dots\dots (24)$$

$$GOs = 1 + 63 \times 5 = 316.$$

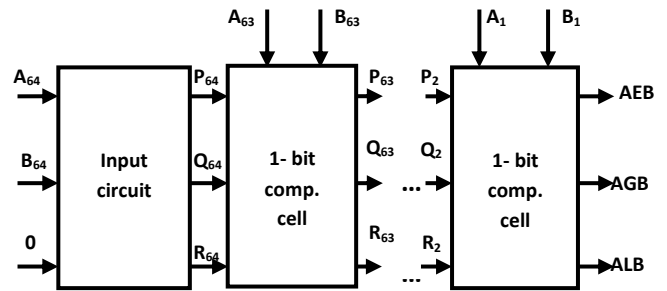


Figure 14. Sixty-Four-bit reversible binary comparator

4.10 n-bit Reversible Binary Comparator

In n-bit reversible binary comparator first stage is circuit for MSB stage works as one-bit comparator to compares the MSB bits of the two numbers A_n , B_n . Second stage is one-bit comparator cell compares the result of the first stage and the input bits A_{n-1} , B_{n-1} . Third stage is also one-bit comparator cell compares the output of the second stage and the input bits A_{n-2} , B_{n-2} . Fourth stage compares the result of third stage and the input bits A_{n-3} , B_{n-3} of the two numbers and so on. The final stage compares the output of the $(n-1)^{th}$ stage and the LSB bits A_1 , B_1 resulting the final output of the n-bit numbers A and B. The QC of n-bit reversible binary comparator is given in an Equation:

$$QC = QC \text{ of circuit for MSB} + ((n-1) * QC \text{ of one-bit Comparator cell}) \dots\dots\dots (25)$$

The number of CIs of n-bit reversible binary comparator is given in an Equation:

$$CIs = CIs \text{ of circuit for MSB} + ((n-1) * CIs \text{ of one-bit Comparator cell}) \dots\dots\dots (26)$$

The GOs of n-bit reversible binary comparator is given in an Equation:

$$GOs = GOs \text{ of circuit for MSB} + ((n-1) * GOs \text{ of one-bit comparator cell}) \dots\dots\dots (27)$$

5. RESULT ANALYSIS

5.1 Simulation Results

The simulation is carried out using Cadence Tool and S18 (180nm-Analog Process) Technology. The typical gate delay for the process is given ~ 0.2 pf/gate. The one-bit, two-bit, three-bit and four-bit reversible binary comparators are designed and the schematics are simulated to check the functionality of the design, power consumption and delay. The simulation results of one-bit, two-bit, three-bit and four-bit reversible binary comparator are shown in Figure 15, 16, 17 and 18 respectively.

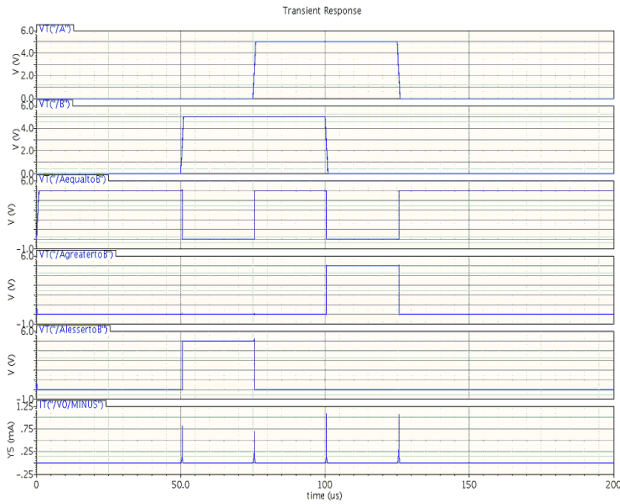


Figure 15. Simulation result of one-bit reversible comparator

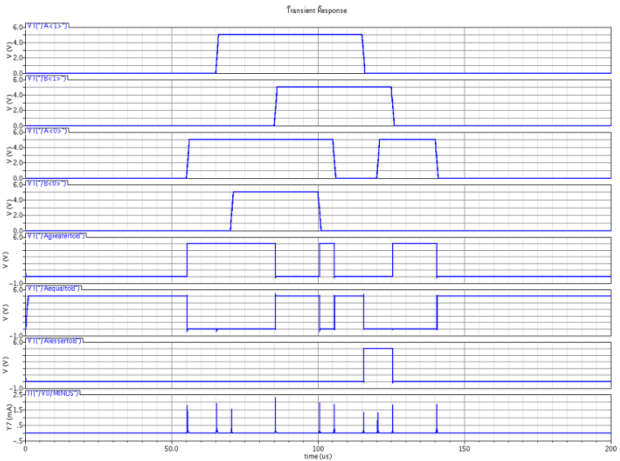


Figure 16. Simulation result of two-bit reversible comparator

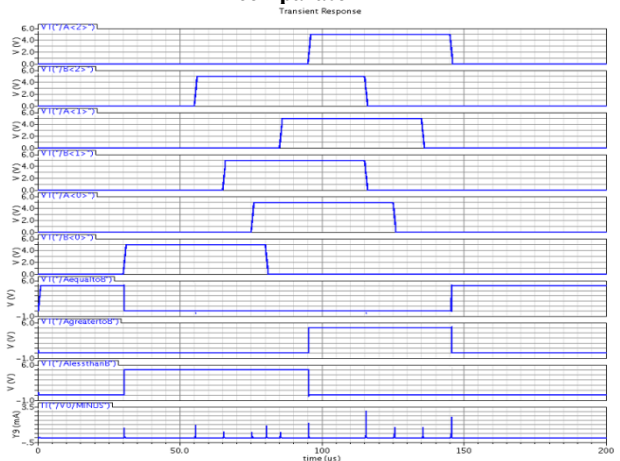


Figure 17. Simulation result of three-bit reversible comparator

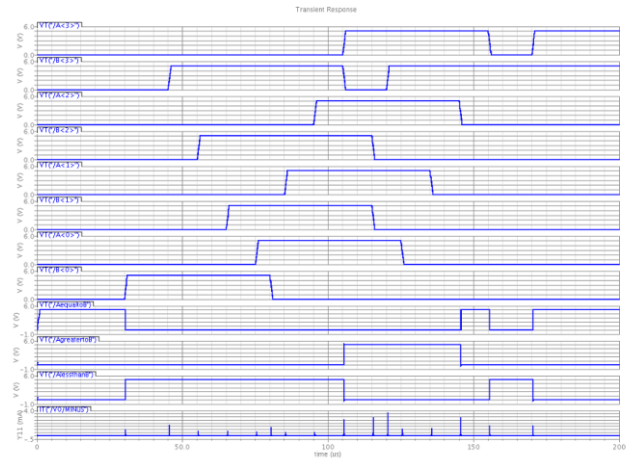


Figure 18. Simulation result of four-bit reversible comparator

5.2 Performance analysis

The performance of 8, 16, 32 and 64-bit binary comparator design is shown in the table 5. The quantum cost is 118 in case of 8-bit comparator and 246, 502 and 1014 in case of 16, 32 and 64-bit comparator respectively. The number of constant inputs are 23, 47, 95 and 191 in case of 8, 16, 32 and 64-bit comparator respectively. The numbers of garbage outputs are 36 in 8-bit design, 76 in the case of 16-bit, 156 and 316 in the case of 32-bit and 64-bit design respectively.

Table 5. Performance of 8, 16, 32, 64-bit reversible binary comparator

Parameter	8-bit	16-bit	32-bit	64-bit
Quantum cost	118	246	502	1014
Constant inputs	23	47	95	191
Garbage outputs	36	76	156	316
Delay (nS)	57.6	120	244.8	494.4
Power (μ w)	45.31	79.31	147.31	283.31

A comparison of the proposed serial design of 8 and 64-bit reversible binary comparator with the existing approaches [5] and [6] is given in table 6. From the table it is evident that the proposed design has an improvement of 12.59% and 63.23% in QC, 14.28% and 43.75% in GOs in the case of 8-Bit. The improvement of 11.28% and 59.52% in QC, 16.40% and 38.28% in GOs in the case of 64-bit comparator w. r. t. the existing techniques [5] and [6] respectively. Figure 25 shows the graphical representation of the existing and proposed reversible binary comparators compared in terms of quantum cost and number of garbage outputs. Therefore proposed design has better performance compared to the existing techniques.

Table 6. Comparison of existing and proposed 8-bit and 64-bit reversible binary comparators

	8-bit		64-bit	
	QC	GOs	QC	GOs
Thapliyal et al., [5]	135	42	1143	378
Al-Rabadi [6]	321	64	2505	512
Proposed design	118	36	1014	316
Improvement in % w.r.t [5]	12.59	14.28	11.28	16.40
Improvement in % w.r.t [6]	63.23	43.75	59.52	38.28

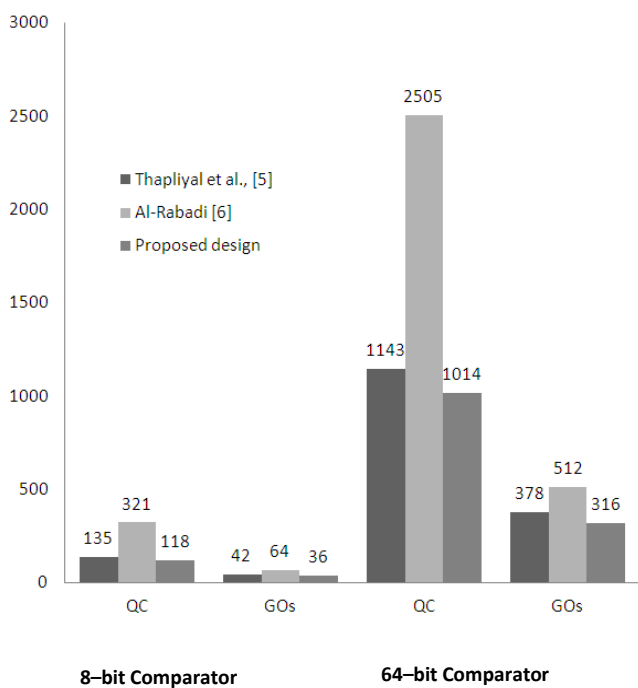


Figure 25. Comparison of existing and proposed reversible binary comparators

6. CONCLUSIONS

In this paper design and optimization of n-bit reversible binary comparator is presented. The design is based on the useful properties of PG gate suitable for comparator. The n-bit reversible binary comparator are designed using circuit for MSB as first stage to compare MSBs and one-bit comparator cell as second stage and so on to compare lesser significant bits. The power consumption, delay, garbage outputs and constant inputs are computed. It is seen that the quantum cost and garbage output values are less in the proposed technique compared to the existing approaches. The design is useful in realizing hardware implementation of the quantum algorithms.

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