Detection and Diagnosis of Faults in the Routing Resources of a SRAM based FPGAs

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ABSTRACT
Field programmable gate arrays (FPGAs) are the reconfigurable logic devices which are widely used in many applications like system prototyping, complex computing systems, automotive electronics and mobile devices. FPGAs have become very popular at present because of their features like high logic capacity, reconfigurability and regular structure with less area cost. However, increase in density and complexity also has resulted in more probability of defects. FPGAs are prone to different types of faults similar to other complicated integrated circuit chips. Faults may occur due to many reasons like environmental conditions or aging of the device. The rate of occurrence of permanent faults can be quite high in emerging technologies, and hence there is a need for periodic testing of such FPGAs. To effectively deal with the increased defect density, we need efficient methods for fault detection and correction.

Here, we present an approach for testing FPGA interconnect that exploits the reprogramability of an FPGA to create built-in self test (BIST) logic by configuring it only during off-line testing. In this way, testability is achieved without any area overhead, since the BIST logic "disappears" when the circuit is reconfigured for its normal system operation. We have used XILINX ISE12.1 for simulation and synthesis.

Keywords: *BIST, CLB, CUT, LUT, TPG, ORA*

1. Introduction

An FPGA is a programmable logic device consisting of an array of logic blocks (CLB) connected to one another through programmable interconnect or the routing resources. Both CLBs and interconnect are programmed according to the data present in the configuration memory. Static RAM (SRAM) based FPGAs mainly consists of two types of interconnect. They are the global interconnect and local interconnect. Global interconnect links one CLB to another through horizontal and vertical routing channels. Local interconnects are associated with CLBs input and output pins. Local interconnect has most programmable SRAM cells compared to any other part of the routing resources. In order to test the local interconnect, CLBs are very much necessary [1].Testing an FPGA interconnect is a challenging task for the test engineers as it occupies 80% of the device area. [2]. Test methodologies for detecting faults in interconnect mainly concentrate on generating numerous configurations for programmable SRAM cells which connect different wire segments.

Testing can be prohibitively expensive for fast and complex systems since the testing equipment must supply test patterns to the FPGA and collect the output responses faster than the speed of the FPGA itself. Instead of external test equipment, if we create a testing circuit on the Integrated Circuits it is called as Built in self test (BIST). It would achieve maximal stuck-at fault coverage and would be executed at speed to provide high fault coverage for a variety of fault models in the FPGA. The first BIST for the configurable logic in FPGAs was proposed in [3]. With growing complexity of integrated circuits and systems, the cost of testing has become ever more significant. BIST is increasingly being applied as an effective means to reduce the cost of testing [4].The main components of a BIST scheme are Test Pattern Generator (TPG), which produces the test patterns for the circuit under test (CUT), and output response analyzer (ORA), which compacts the response of the CUT.

In this paper section II presents overview of FPGA interconnect and previous techniques. Section III explains types of faults and fault models. Section IV gives the fault detection technique and simulation results and concludes with section V.

2. General SRAM based FPGA interconnect structure

Figure1 shows a detailed structure of interconnect. It has basically connection block and the switch block (switch matrix). A logic block input pin connects to channel wire segments through switches in an input connection block. The logic block output pins are connected to channel wire segments via an output connection block. A switch block makes connections between wire segments at every intersection of a horizontal and vertical channel. Each switch matrix contains a set of switches which allow input wire segments to connect to wire segments in adjacent channels.

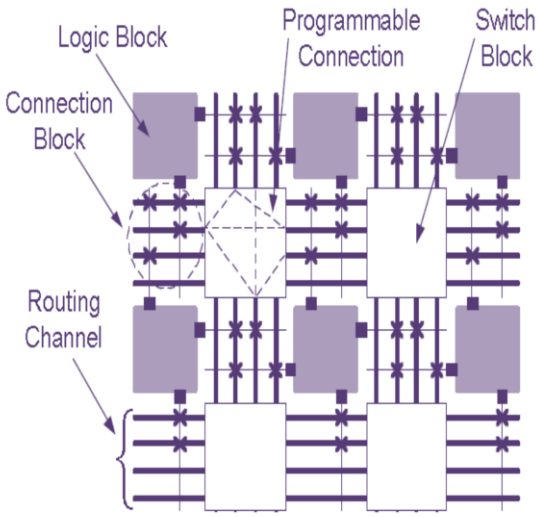


Figure 1. Structure of Interconnect

The connecting blocks and wire segments associated with CLBs are also called as local interconnects. A connecting block mainly consists of programmable-interconnect-point PSs (PIP-PSs) and multiplexer PSs (MUX-PSs) to bring

signals into and out of CLBs. On the other hand, wire segments and programmable cross-point PSs (PCP-PSs) within the switch matrix (SM) in global interconnects form horizontal and vertical routing channels that connect signals between CLBs. The input–output signals can be transmitted into or out of the FPGA using the input–output blocks (IOBs).

Previous work:

Many researchers have developed techniques for detecting the faults across the local and global interconnect using fault models and applying multiple configurations. [6]–[11],[12]–[17], external testers are used for testing the internal components via I/O blocks in [6]–[11], where as 12]–[17] have used BIST technique and JTAG port of the device. These methods require minimum control from the outside. In [7]–[9], and [11] interconnect issues are considered, where as [7]–[9], [11], [12], [13], [16], and [17] focus on global, local, and global and local interconnects, respectively. In [4], global interconnects are programmed to form "global busses" and are tested using classical bus testing vectors externally applied to the device. Testing for local interconnects can only be performed by passing test signals through the CLBs. In [8] and [11], one-dimensional CLB arrays, each containing CLBs, are used for an FPGA. Multiple fault detection is not guaranteed in [11] due to the use of XOR trees and D flip-flop (DFF) chains to propagate the test outputs. The first BIST proposal for testing interconnects resources is a comparison-based approach by Stroud *et al.* [10]. They configure a subset of wire segments and PSs to form two groups of *wires under test* (WUTs). The two WUTs receive identical test patterns from a group of CLBs configured as *test pattern generators* (TPGs), and are compared by a group of CLBs configured as an *output response analyzer* (ORA). This approach has good fault coverage for shorts/opens on wire segments and stuck-on/off faults in PSs. However, the ORAs fail to detect multiple faults that have identical faulty behavior in the two WUTs groups. In [6], a parity-based error control coding technique is proposed for global interconnect testing. It supports superior multi fault coverage.

3. Types of Faults and Fault models

In general, FPGAs are prone to different types of faults, they may be **transient** or **permanent** faults which appear during the lifetime. These types of faults are briefly explained below.

Transient Faults: Transient faults also called as soft errors are mainly due to environmental conditions. These faults occur because of energetic nuclear particle or an electrical source [18]. The nuclear particles which cause errors are either cosmic ray which bombards the earth constantly from space radiations. Power supply noise or electromagnetic interference (EMI) may also induce the errors.

Permanent faults: Permanent faults may occur because of electro migration or with the aging of the device, small manufacturing imperfections that are not detected by production testing may become effective during the lifetime. Design errors can also cause a device to stop functioning in response to rare sequences of input [19].These faults are modeled as, open/short, stuck-on/off and stuck-at-0/1. The stuck–on/off faults appear in the pass transistor of PIP-PS or MUX-PS in local interconnect. Figure2 shows the case of stuck-on/off faults in local interconnects.

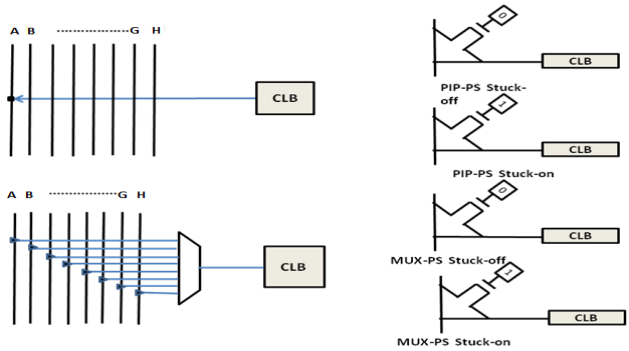


Figure 2 : stuck-on/off in the local interconnect

The open/ short faults occur in the PCP-PS or wire segments of global interconnect, as shown in Figure 3. An open fault in the global interconnect is a disconnection of any wires, while short fault indicates a bridging between two wires.

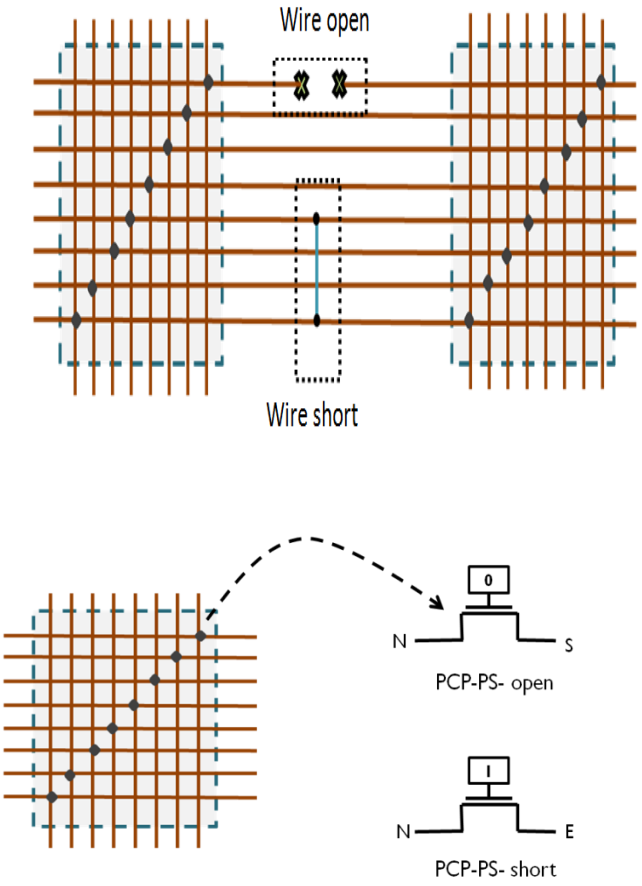


Figure 3. Open/Short faults in global interconnect

4. Fault detection and diagnosis strategy:

Our basic idea is to use BIST concept for detection and diagnosis of faults which occur across local interconnect and the global interconnect. For realizing this we have considered the interconnect structure of XILINX 4000 FPGA. Main functional blocks such as TPG and the ORA are configured on the CLBs of the FPGA. Output of the TPG is connected to the local interconnect fault model and then to the global interconnect fault model. After identifying fault, localization or diagnosis of the fault is done. BIST for CLB and interconnect has three main functional logic blocks. They are TPG, BUT and the ORA.

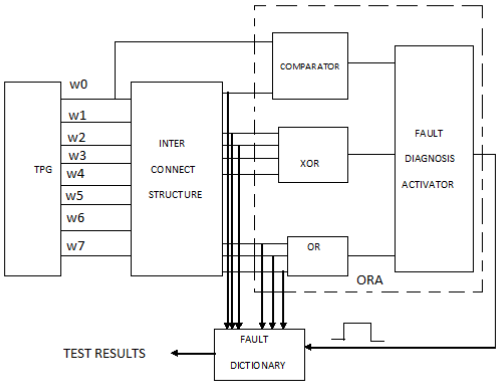


Figure 4. Local/ global interconnect BIST

TPG: Test pattern generator – this block should generate test vectors for finding the faults in BUT. After identifying faulty block for locating faults (diagnosis) also we need test patterns. Whenever we are selecting a TPG we should consider the time factor and its coverage. Time required for generating vectors should be less and the number of vectors for detecting all the faults (100%) should be minimum. Keeping this in mind, for testing CLBs and interconnect resources we have selected an algorithmic test generation method as given in [21]. Test vectors are as shown in table . TPG block is configured on the CLBs. Test vectors are stored in the LUTs of the CLBs. These are subsequently applied to the BUT which may be either CLBs or the interconnect resources. Test vectors are so chosen that we can activate stuck-at faults in the LUTs, wire-open faults, stuck-on/off and bridging faults in interconnect. Output from the BUT is sent to the ORA (output response analyzer) for checking the presence of faults.

ORA: It basic function is to compare the obtained outputs from the BUT with that of the actual value. We have used a simple two input XOR as the comparator for checking wire-open fault in global interconnect as in figure 4. Logic high output indicates presence of fault. A 4bit XOR is used as a parity checker to determine faults in the LUTs and local interconnect. A fault dictionary is used after detecting the faults. This will be activated by the fault dictionary activator.

Table .Test Vectors

Input	Output of LUTs							
	C1	C2	C3	C4	C5	C6	C7	C8
0000	0	1	0	1	0	1	0	1
0001	0	1	0	1	0	1	1	0
0010	0	1	0	1	1	0	0	1
0011	0	1	0	1	1	0	1	0
0100	0	1	1	0	0	1	0	1
0101	0	1	1	0	0	1	1	0
0110	0	1	1	0	1	0	0	1
0111	0	1	1	0	1	0	1	0
1000	1	0	0	1	0	1	0	1
1001	1	0	0	1	0	1	1	0
1010	1	0	0	1	1	0	0	1
1011	1	0	0	1	1	0	1	0
1100	1	0	1	0	0	1	0	1
1101	1	0	1	0	0	1	1	0
1110	1	0	1	0	1	0	0	1
1111	1	0	1	0	1	0	1	0

BUT: Block under test or circuit under test is nothing but the CLBs (configurable logic block) and interconnects of the FPGA. In order to detect multiple faults we have configured 4 CLBs as BUTs as in figure 6. For testing purpose we have considered 4 input LUT of a CLB. Interconnect is having 8 wire segments. W1 is configured as global interconnect. W2-W5 considered as local interconnect are used for testing stuck at faults. W6-W8 are used for testing short faults between the wires.

For testing global interconnects, test patterns should be applied to the horizontal and vertical wires through PCP-PSs in SMs. We have considered the fault model as shown in figure3 and the TPG output is connected to it. Corresponding outputs are verified with the help of ORA. For testing global interconnect we have not used any CLBs as we have taken horizontal and vertical bus for finding the faults. For testing PCP-PSs in SMs completely, it has to be configured in three different directions [20], [1]. Orthogonal(OR), left diagonal(LD) and right diagonal (RD). Orthogonal direction has all W–E and N–S PIP-PSs of a PCP-PS in SMs programmed closed, and the remainder is left open, connecting intersecting horizontal and vertical wires. LD and RD are similarly configured, testing the N–W and S–E and the S–W and N–E PIP-PSs of a PCP-PS, respectively.

Fault diagnosis

Fault diagnosis is a process of identifying the exact location of the fault in the structure. This can be done by comparing the obtained faulty values with the values stored in fault dictionary. We have created a fault dictionary for storing all possible faulty values. Initially we have diagnosed the faulty blocks and then type of fault. We have introduced faults at various points between four functional blocks F1-F4 and then outputs are compared with the fault dictionary values.

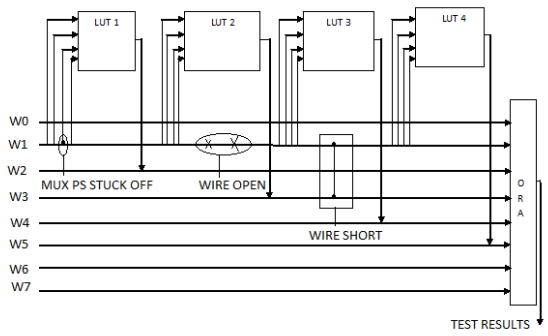
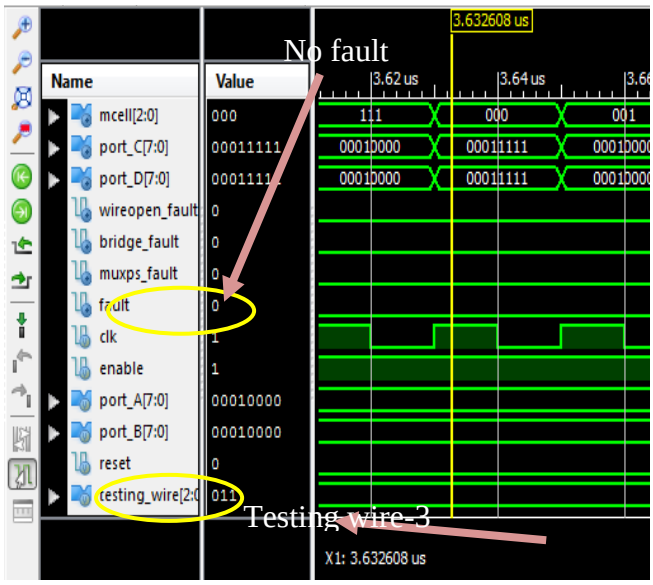


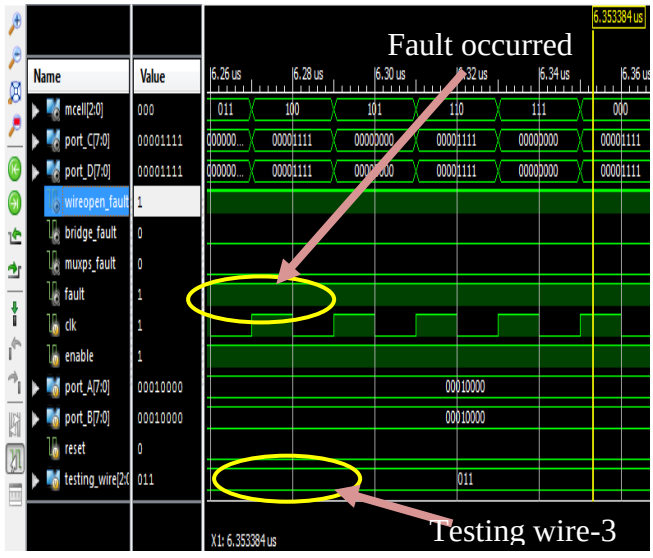
Figure 6. Multiple fault detection in interconnect

Simulation Results:

1. Testing Wire 3: Fault free

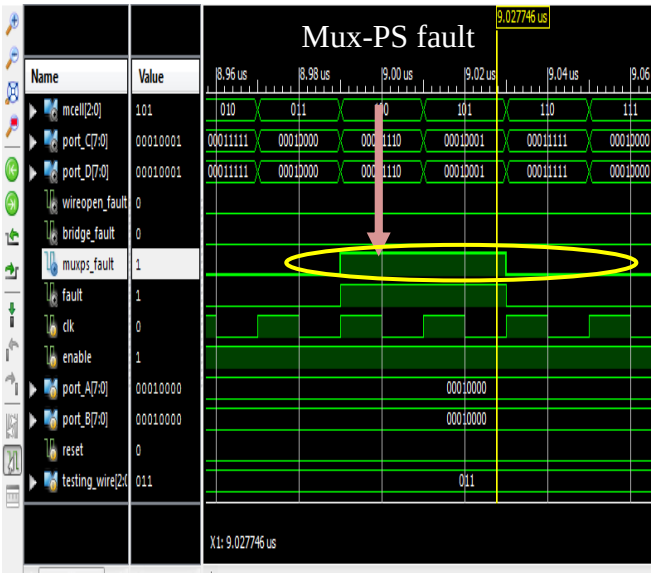


2. Testing wire 3: Wire open Fault (Fault introduced at F4 location)



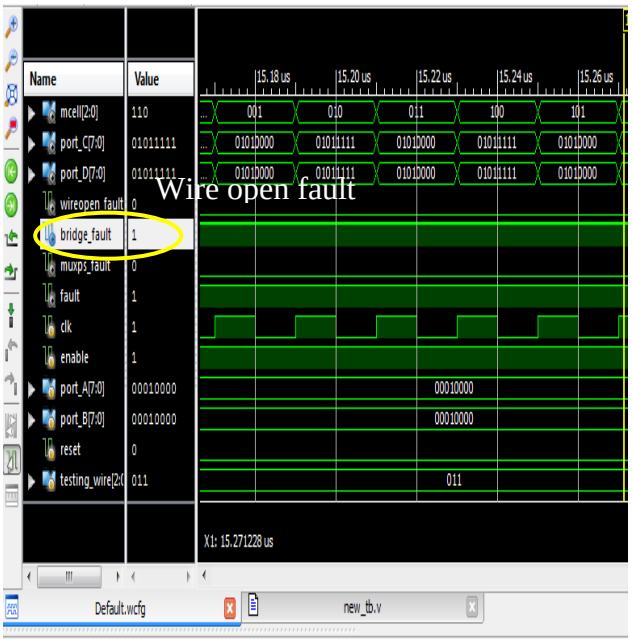
The simulation result of Fig shows a wire open fault during the testing of wire-3. A fault signal indicates the occurrence of fault. The location of fault can be obtained by diagnosing the BUT. The fault was introduced at F4 location.

3. Testing Wire 3: Mux stuck off fault (Fault introduced at F4 location)



In this simulation result of Fig fault was introduced at third input of Mux-ps at F4 location. The fault data is "00011110" and "00010001" when C5 & C6 are loaded into LUTs respectively.

4. Testing wire 3: wire short fault (Wire 3-wire 1 fault introduced at F3 location)



The simulation result of Fig shows a wire short between wire 3 and wire1. The fault was introduced at F3 location.

5. Conclusion:

In this paper we have presented a BIST technique for detecting and diagnosing faults in interconnect of an FPGA. We used eight test vectors for testing a single structure. In order to test the entire FPGA we need to configure BIST structure 12 times. With this method we can detect and diagnose all the faults in interconnect. As we can test and diagnose all the faults, this method can be used in providing fault tolerance of FPGAs. Simulation and synthesis is done using XILINX ISE 12.1.

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